1967-68

INTEGRATED CIRCUITS CATALOG

TEXAS INSTRUMENTS
INCORPORATED

Notes on This First Edition

This first edition of TI's Integrated Circuits catalog contains currently published data sheets covering SOLID CIRCUIT® semiconductor networks. As new data sheets are published, they will be distributed for insertion in the appropriate sections of this basic Tightleaf® catalog.

This catalog replaces collections of loose integrated circuits data sheets. Many of the data sheets in this book have been revised, and therefore cancel and supersede earlier editions.

Please give your present collection to a co-worker who can make use of it; the largest part of the old data is still current.

Note that certain large blocks of page numbers have intentionally been omitted, to permit simplified numbering of insert pages.

To insert pages: Turn to colored page, Page 1251.

TEXAS INSTRUMENTS

1967-8

INTEGRATED CIRCUITS CATALOG

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TEXAS INSTRUMENTS
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SEMICONDUCTOR-COMPONENTS DIVISION
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HOW TO USE THE INDEXES

If you know only the **category of device,**
look in the **Table of Data Sheet Contents,** page **3.**

If you know only the **device number,**
look in the **Numeric Index,** page **6.**

The first page of a data sheet is always a right-hand page.

INTEGRATED CIRCUIT SELECTION GUIDES

For assistance in selecting devices to meet your requirements,
use the **Selection Guides,** pages **4** and **5.**

SPECIAL INFORMATION

TABLE OF DATA SHEET CONTENTS

(Updated with each mailing of new data sheets)

Full Military Temperature Range Digital Circuits

Transistor-Transistor-Logic (TTL) –55°C to 125°C

Modified Diode-Transistor Logic (Modified DTL) –55°C to 125°C

Diode-Transistor Logic (DTL) –55°C to 125°C

*Operating free-air temperature range of –55°C to 70°C and operating case temperature range of –55°C to 100°C

†Operating free-air temperature range of –55°C to 100°C and operating case temperature range of –55°C to 125°C

Full Military Temperature Range Linear Circuits

Industrial Temperature Range Digital Circuits

Transistor-Transistor Logic (TTL) 0°C to 70°C

Modified Diode-Transistor Logic (Modified DTL) 0°C to 70°C

DIGITAL INTEGRATED CIRCUITS SELECTION GUIDE

TYPICAL CHARACTERISTICS						
PROPAGATION DELAY TIME	POWER DISSIPATION (each gate)	NOISE IMMUNITY	TEMPERATURE RANGE	TYPE OF LOGIC	LOGIC FAMILY	CATALOG PAGE
HIGH SPEED — HIGH A-C AND D-C NOISE MARGINS						
13 ns	10 mW	1000 mV	–55°C to 125°C	TTL	Series 54	1001
13 ns	10 mW	1000 mV	–55°C to 125°C	TTL	Series 54 930	1501
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74	5001
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74 930	5501
MEDIUM SPEED — HIGH D-C NOISE MARGIN						
25 ns	8 mW	750 mV	–55°C to 125°C	DTL	Series 15 930	3001
25 ns	8 mW	750 mV	0°C to 75°C	DTL	Series 15 830	7001
ECONOMICAL PLUG-IN PACKAGE						
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74N	6001
25 ns	8 mW	750 mV	0°C to 75°C	DTL	Series 15 830N	7501
MODIFIED DTL						
30 ns	10 mW	300 mV	–55°C to 125°C	Modified DTL	Series 53	2001
30 ns	10 mW	300 mV	0°C to 70°C	Modified DTL	Series 73	6501

LINEAR INTEGRATED CIRCUITS SELECTION GUIDE

DIFFERENTIAL/OPERATIONAL AMPLIFIERS

PARAMETER		TYPE SN521A	SN522A	SN523A SN5231L	SN524A SN524AL	SN525	SN526	SN5510 SN5510L	SN723 SN7231L	SN724 SN724L	UNIT
A_{vs}	Open-loop voltage gain	62	62	72	63	90	66	40	69	61	dB
BW	Bandwidth (–3 dB)	50	50	180	140	45	120	40,000	150	140	kHz
Z_{in}	Input impedance	—	—	15	1,000	140	1,000	6	10	800	kΩ
C_{in}	Input capacitance	—	—	55	60	250	50	7	55	60	pF
V_{DI}	Differential-input offset voltage	1	1	2.2	12	1	3	3	4	15	mV
I_{DI}	Differential-input offset current	0.2	0.2	0.5	0.02	0.016	0.006	3	1	0.044	μA
α_{VDI}	Differential-input offset voltage temperature coefficient	8	8	9	25	5	10	10	10	30	μV/deg
V_{CMIM}	Maximum common-mode input voltage range	±3	±3	±5	±5	±7	±7	±1	±5	±5	V
V_{CMO}	Common-mode output offset voltage	0.5	0.5	0.5	—	0.25	0.22	3.1	0.6	—	V
Z_{out}	Output impedance	10,000	160	200	200	10,000	—	35	250	300	Ω
V_{OM}	Maximum peak-to-peak output voltage	8.2	5.4	24	15	18	11.7	4.0	20	12	V
CMRR	Common-mode rejection ratio	60	60	90	55	100	77	85	80	55	dB
P_T	Total power dissipation	28	72	100	120	100	132	165	100	120	mW
I_{in}	Input current	2	2	5	0.08	0.45	0.05	40	6.5	0.11	μA
	CATALOG PAGE	4001	4001	4005 4009	4013	4017	4023	4505	8001 8005	8009	

SENSE AMPLIFIERS

PARAMETER		TYPE SN5500	SN7500	SN7501	SN7502	UNIT
V_T	Differential-input threshold voltage	17	17	17	21	mV
V_{CMF}	Common-mode input firing voltage	2	2	2	2.5	V
$V_{out(1)}$	Logical 1 output voltage	3.2	3.2	3.2	3.2	V
$V_{out(0)}$	Logical 0 output voltage	0.2	0.2	0.2	0.2	V
$I_{in(1)}$	Logical 1 level input current (strobe or reset)	1.2	1.2	—	—	mA
$I_{in(0)}$	Logical 0 level input current (strobe or reset)	—	—	–1.1	–1.1	mA
$Z_{in}D$	Differential-input impedance	0.2	0.2	5	5	kΩ
I_{CC1}	V_{CC1} supply current	15	15	18	15	mA
I_{CC2}	V_{CC2} supply current	–10	–10	–10	–8	mA
I_{ref}	V_{ref} supply current	—	—	2.5	2.5	mA
$t_{cyc(min)}$	Minimum cycle time	1.5	1.5	0.7	1.5	μs
	CATALOG PAGE	4501	8504	8506	8508	

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NUMERIC INDEX

(Updated with each mailing of new data sheets)

This index is presented for the user who is not familiar with the "series system" of designating integrated circuits. It is therefore arranged in strict ascending numerical order, disregarding letter prefixes and series relationships.

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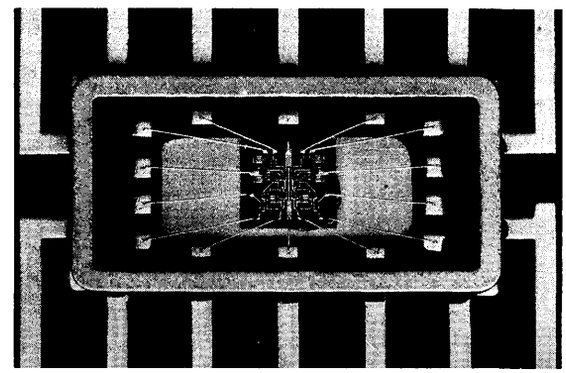
SERIES 54
BULLETIN NO. DL-S 669179, DECEMBER 1966
REPLACES BULLETINS NO. DL-S 657921, AUGUST 1965
AND DL-S 668579, NOVEMBER 1966

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

Series 54 integrated circuits have been designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. Definitive specifications are provided for operating characteristics over the full military temperature range of –55°C to 125°C. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems.



TYPE SN5400 PRIOR TO CAPPING

features

LOW SYSTEM COST

- **maximum number of circuits per package through use of 14-lead package**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay time of 13 ns**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **full fan-out of 10**

CONTENTS

†Patented by Texas Instruments.

design characteristics

Series 54 digital integrated circuits effect an optimization between saturated logic circuitry and monolithic semiconductor technology yielding high perfotmance at lowest cost. In discrete-component circuitry maximum use is made of lower cost components (diodes and resistors) instead of the higher priced transistors. However, in monolithic circuitry it costs no more to build transistors than diodes or resistors. Therefore, in Series 54, transistors are used to buffer the fluctuations in currents that occur as resistor values change. Also, the Series 54 multiple-emitter transistor can easily be built in a monolithic bar to eliminate the need for conventional input diodes.

circuit operation

The transistor-transistor logic (TTL) used in Series 54 is analogous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode D_3. If inputs A and B are raised to a high voltage, drive current will then pass through diode D_3.

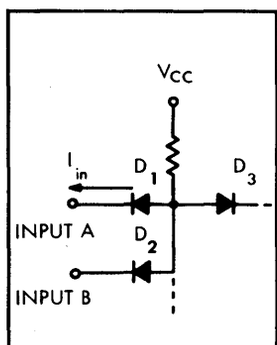


Figure A
Diode AND Logic

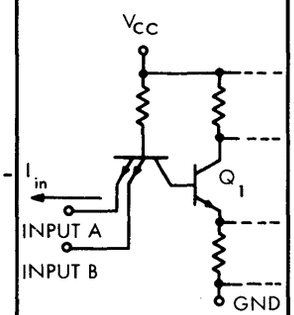


Figure B
Series 54 AND Logic

In Series 54 TTL circuitry, the multiple-emitter transistor performs the same function as the diodes in DTL (see figure B). However, the transistor action of the multiple-emitter transistor causes transistor Q_1 to turn-off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

Although one-volt d-c noise margins are typical for Series 54 circuits, an absolute guarantee of 400 millivolts is assured for every unit. This is accomplished by testing each output and input as shown in figures C and D.

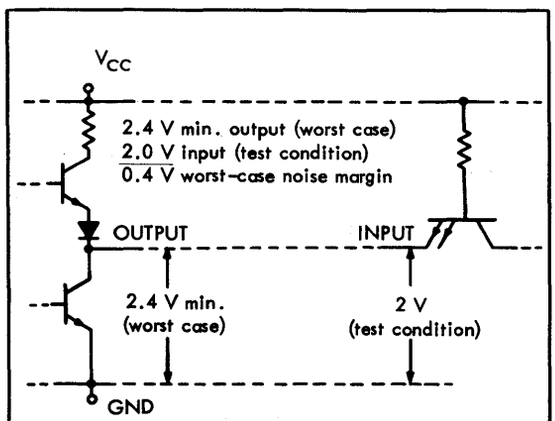


Figure C — Logical 1 Noise Margin

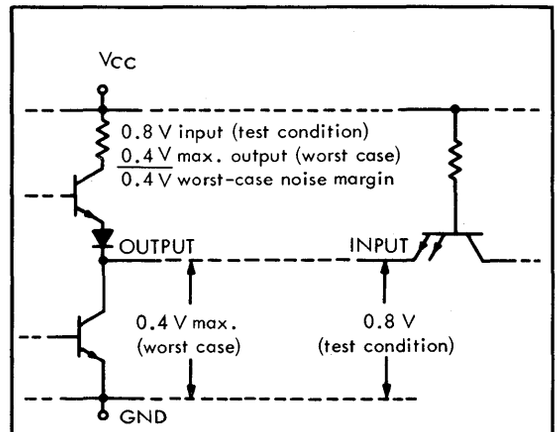


Figure D — Logical 0 Noise Margin

Each output is tested to ensure that the logical 1 output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest V_{CC}, and 0.8 volt on the input — 400 mV more than the logical 0 maximum.

Each output is tested to ensure that the logical 0 output voltage will not exceed 0.4 volt. This is done with full fan-out, lowest V_{CC}, and 2 volts on the input — 400 mV less than the logical 1 minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition, the threshold voltage of the Series 54 circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in figure E.

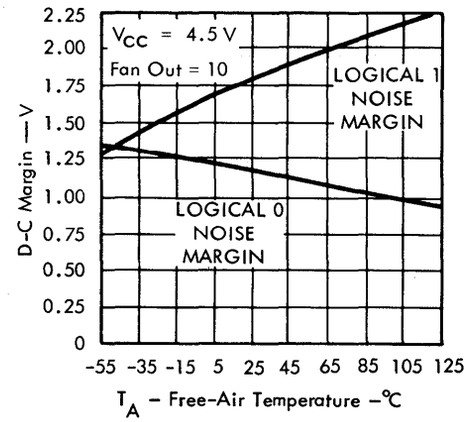
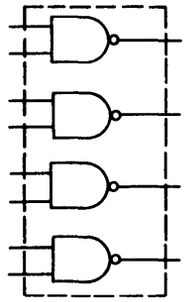


Figure E — Typical D-C Margin vs Temperature

Another important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12 Ω and logical 1 output impedance is 70 Ω. This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve waveshape integrity.

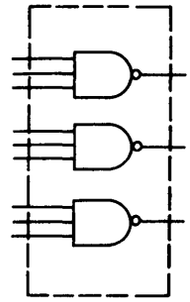
standard line summary

SN5400 See page 1005



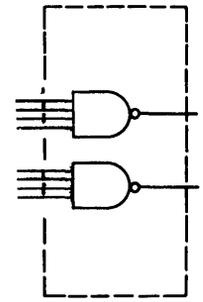
QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN5410 See page 1006



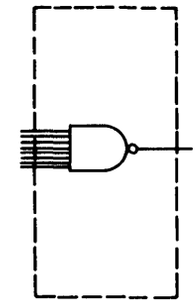
TRIPLE 3-INPUT POSITIVE NAND GATE

SN5420 See page 1007



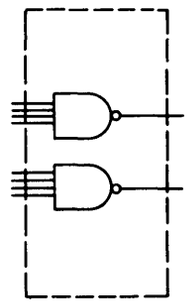
DUAL 4-INPUT POSITIVE NAND GATE

SN5430 See page 1008



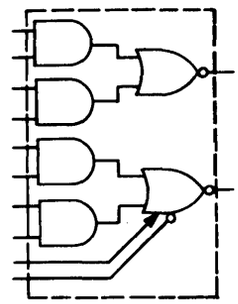
8-INPUT POSITIVE NAND GATE

SN5440 See page 1009



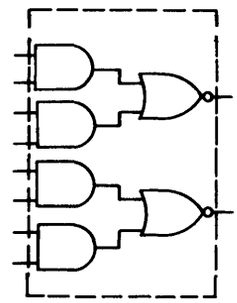
DUAL 4-INPUT POSITIVE NAND BUFFER

SN5450 See page 1010



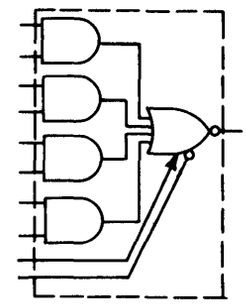
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

SN5451 See page 1010



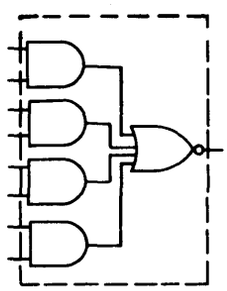
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

SN5453 See page 1012



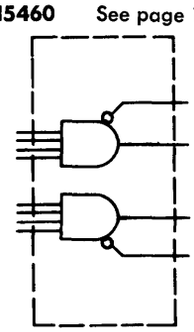
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE

SN5454 See page 1012



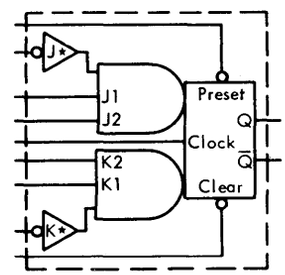
4-WIDE 2-INPUT AND-OR-INVERT GATE

SN5460 See page 1014



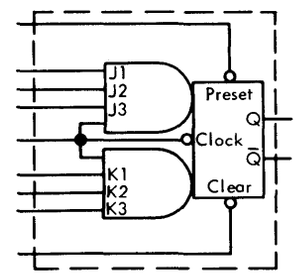
DUAL 4-INPUT EXPANDER

SN5470 See page 1015



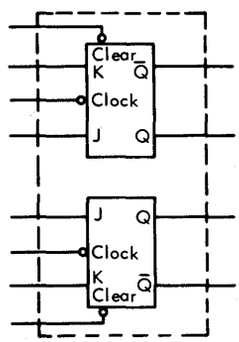
J-K FLIP-FLOP

SN5472 See page 1018



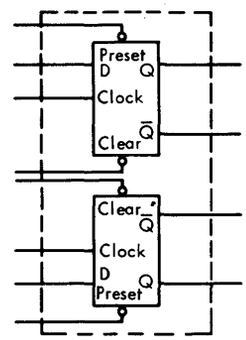
J-K MASTER-SLAVE FLIP-FLOP

SN5473 See page 1021



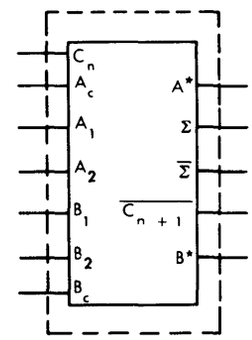
DUAL J-K MASTER-SLAVE FLIP-FLOP

SN5474 See page 1024



DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

SN5480 See page 1027



GATED FULL ADDER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = −55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Each input of the multiple-emitter input transistor requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter input. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). The carry output (C_{n+1}) of the full adder is capable of driving 5 loads (N = 5) and the A★ and B★ nodes may be used to drive 3 loads (N = 3). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

unused inputs

For optimum switching times, unused gate inputs should be tied to a positive voltage source of 2.4 V to 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Supply voltage V_{CC}, if regulated to 5.5 V maximum, may be used.

If the supply voltage V_{CC} cannot be limited to 5.5 V the following alternatives are recommended:

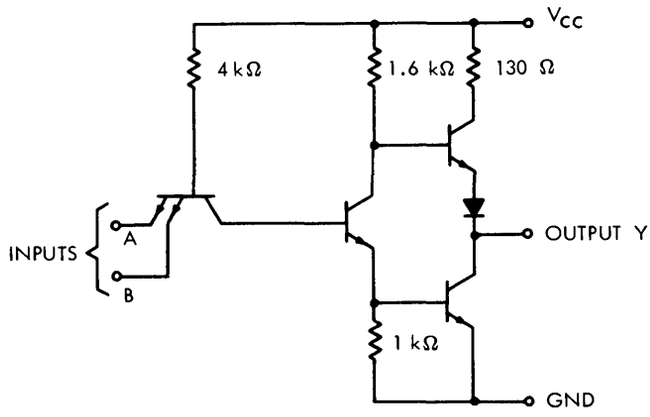
a. Connect unused gate inputs to an independent supply voltage source of 2.4 V to 5.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded.

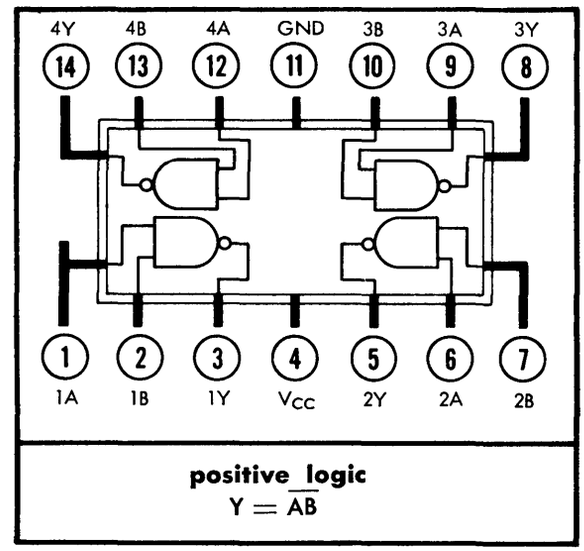
In all cases, unused J★ and K★ inputs of the SN5470 must be connected to ground.

Instructions for terminating unused inputs of the SN5480 are provided in the applications shown for that device.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.5 V		−20		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

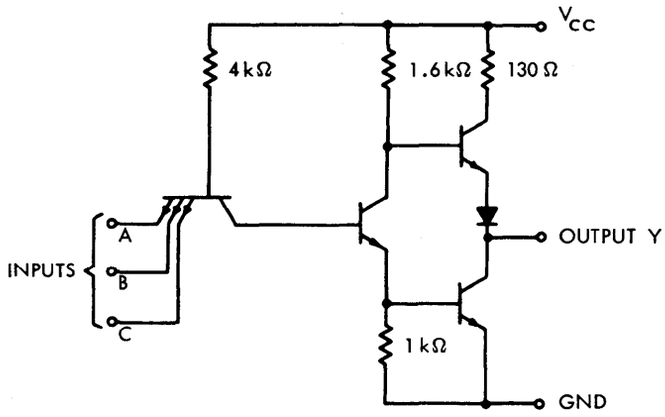
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.

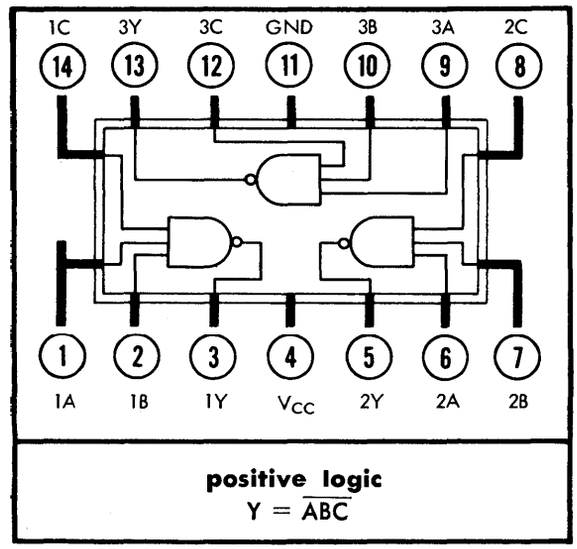
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPE SN5410
TRIPLE 3-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Output, N . . . . . 1 to 10

electrical characteristics, $T_A = -55°C$ to $125°C$

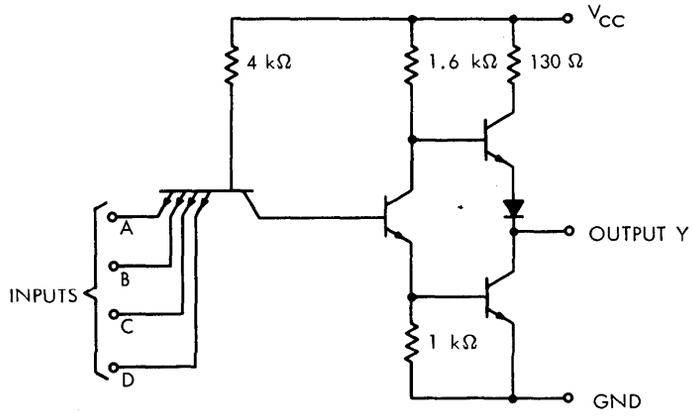
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.5 V		−20		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

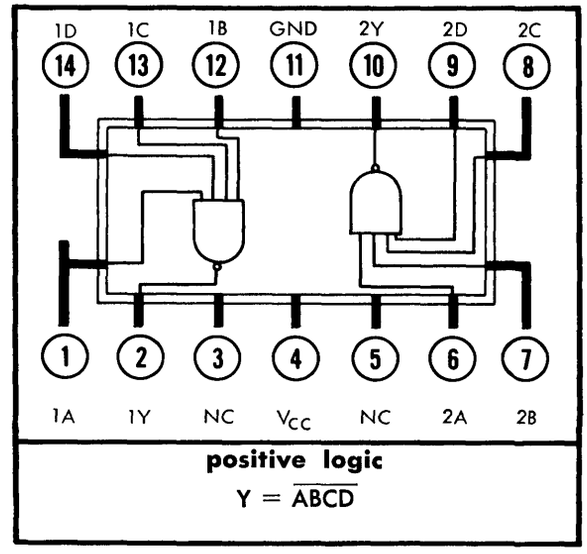
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.5 V		−20		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

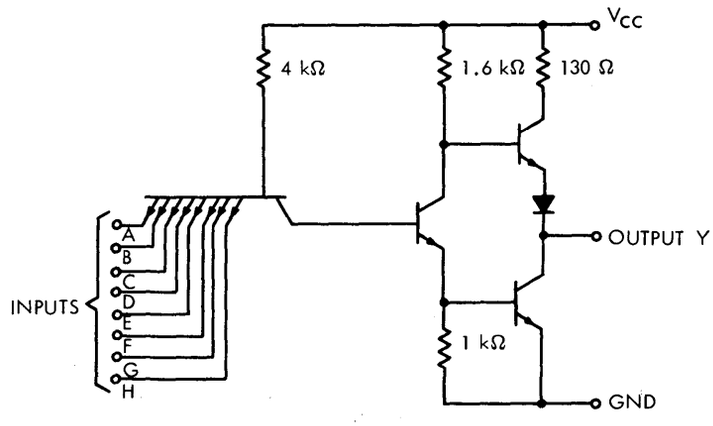
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.

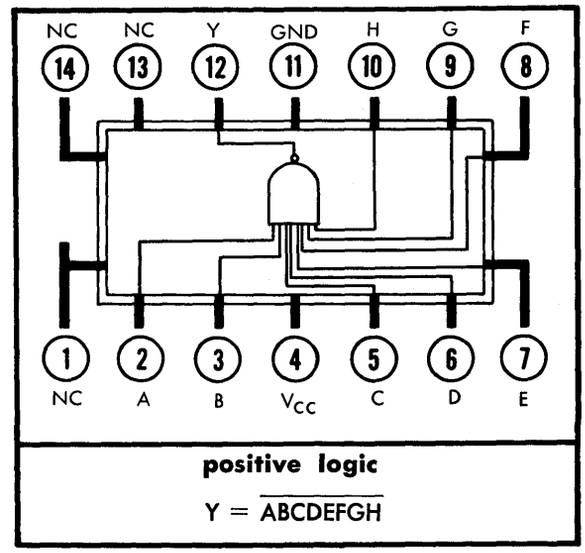
‡*These typical values are at* V_{CC} = 5 V, T_A = 25°C.

TYPE SN5430
8-INPUT POSITIVE NAND GATE

schematic



Component values shown are nominal.



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Output, N . . . . . 1 to 10

electrical characteristics, $T_A = -55°C$ to $125°C$

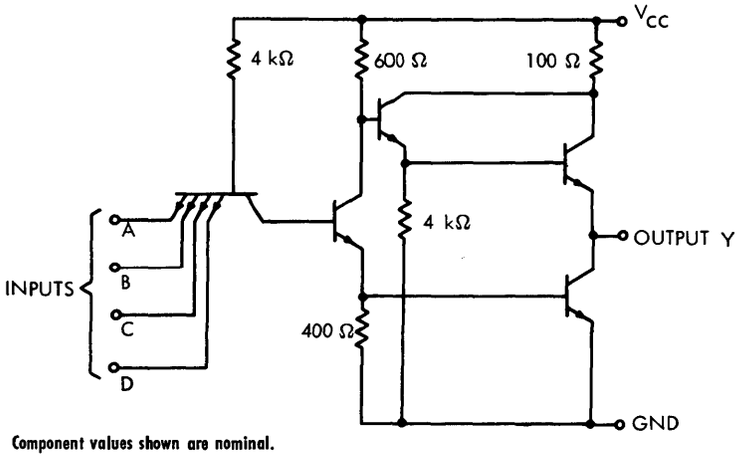
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current	5	V_{CC} = 5.5 V		−20		−55	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = 5 V,	V_{in} = 5 V		3		mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = 5 V,	V_{in} = 0		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

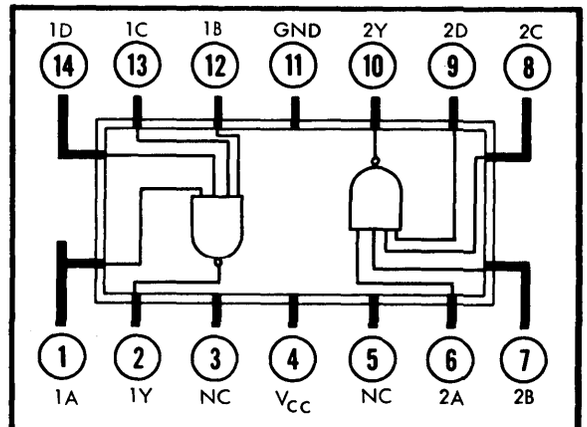
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

‡These typical values are at V_{CC} = 5 V, $T_A = 25°C$.

schematic (each gate)



Component values shown are nominal.



positive logic
$Y = \overline{ABCD}$

recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Output, N	1 to 30

electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −1.2 mA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 48 mA	V_{in} = 2 V,		0.28‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.5 V		−20		−70	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		8.6		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		2		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 30

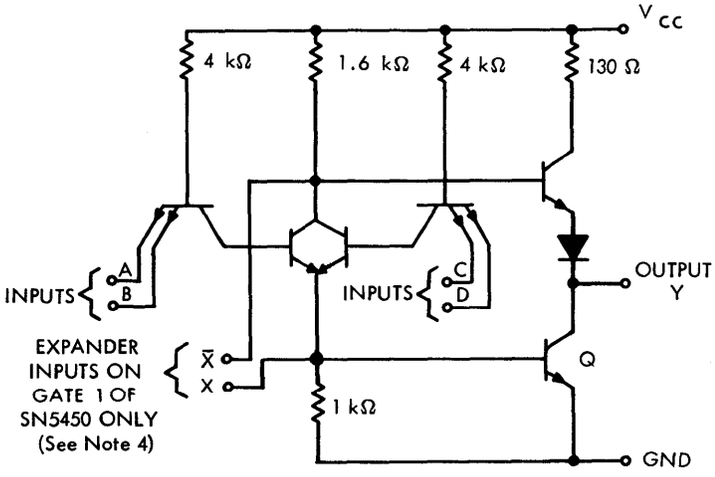
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

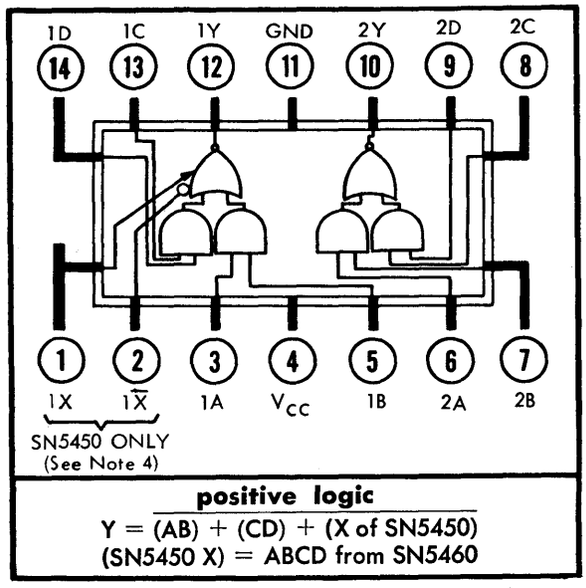
†Not more than one output should be shorted at a time.

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPES SN5450, SN5451
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

schematic (each gate)





positive logic

$Y = \overline{(AB) + (CD) + (X \text{ of SN5450})}$

(SN5450 X) = ABCD from SN5460

NOTES:
1. Component values shown are nominal.
2. Both SN5450 expander inputs are used simultaneously for expanding with the SN5460.
3. If expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN5451.
5. A total of four expander gates may be connected to the SN5450 expander inputs.

recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, T_A = –55°C to 125°C, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	V_{CC} = 4.5 V, $V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	V_{CC} = 4.5 V, $V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = –400 μA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = 4.5 V, V_{in} = 2 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	V_{CC} = 5.5 V, V_{in} = 0			–1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	11	V_{CC} = 5.5 V	–20		–55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	12	V_{CC} = 5 V, V_{in} = 5 V		3.7		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	13	V_{CC} = 5 V, V_{in} = 0		2		mA

†*Not more than one output should be shorted at a time.*

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN5450 only) using expander inputs, $T_A = -55°C$

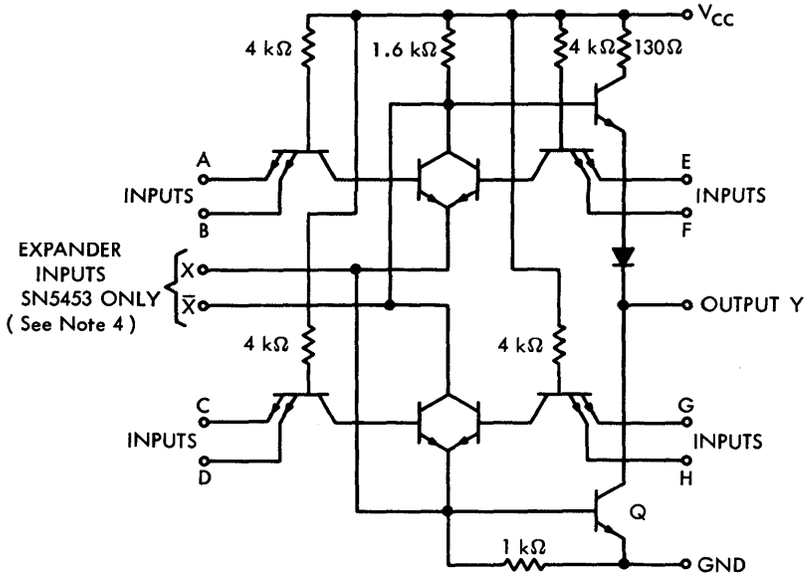
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.5$ V, $V_I = 0.4$ V, $I_{sink} = 16$ mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA, $I_1 = 0.41$ mA, $R_1 = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.5$ V, $I_{load} = -400\ \mu$A, $I_1 = 0.15$ mA, $I_2 = -0.15$ mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA, $I_1 = 0.3$ mA, $R_1 = 138\ \Omega$		0.22‡	0.4	V

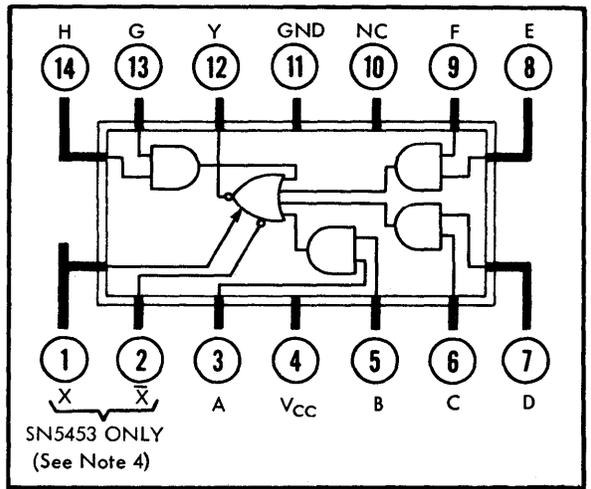
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_1 = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_1 = 15$ pF		18	29	ns

schematic





positive logic

$Y = \overline{(AB) + (CD) + (EF) + (GH) + (X \text{ of SN5453})}$

(SN5453 X) = ABCD from SN5460

NOTES: 1. Component values shown are nominal.
2. Both SN5453 expander inputs are used simultaneously for expanding with the SN5460.
3. If SN5453 expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN5454.
5. A total of four expander gates may be connected to the SN5453 expander inputs.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, T_A = –55°C to 125°C, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	V_{CC} = 4.5 V, $V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	V_{CC} = 4.5 V, $V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = –400 μA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = 4.5 V, V_{in} = 2 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	V_{CC} = 5.5 V, V_{in} = 0			–1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	11	V_{CC} = 5.5 V	–20		–55	mA
$I_{CC(0)}$	Logical 0 level supply current	12	V_{CC} = 5 V, V_{in} = 5 V		5.1		mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = 5 V, V_{in} = 0		4		mA

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN5453 only) using expander inputs, $T_A = -55°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.5$ V, $V_I = 0.4$ V, $I_{sink} = 16$ mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA, $I_1 = 0.41$ mA, $R_1 = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.5$ V, $I_{load} = -400\ \mu$A, $I_1 = 0.15$ mA, $I_2 = -0.15$ mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA, $I_1 = 0.3$ mA, $R_1 = 138\ \Omega$		0.22‡	0.4	V

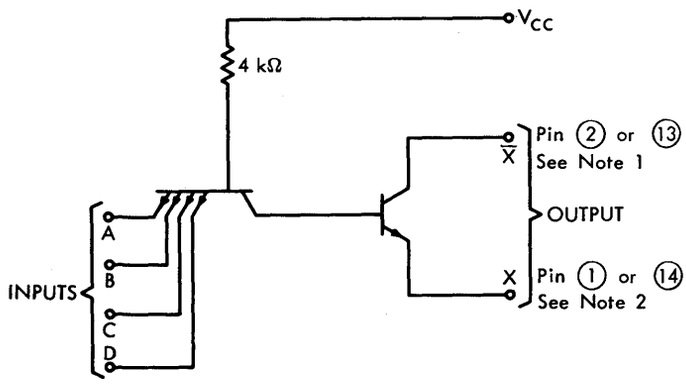
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

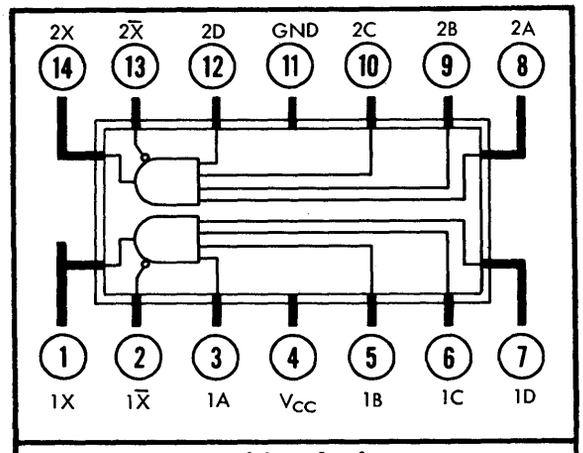
switching characteristics (SN5453 and SN5454), $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_1 = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_1 = 15$ pF		18	29	ns

TYPE SN5460
DUAL 4-INPUT EXPANDER

schematic





positive logic
X = ABCD
when connected to pins (1) and (2) of SN5450 or SN5453

NOTES: 1. Connect pin (2) or (13) to pin (2) of SN5450 or SN5453.
2. Connect pin (1) or (14) to pin (1) of SN5450 or SN5453.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN5450 or one SN5453 4

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output on level	17	V_{CC} = 4.5 V, V_1 = 1 V, R = 1.1 kΩ, T_A = –55°C,	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output off level current	18	V_{CC} = 4.5 V, V_1 = 4.5 V, R = 1.2 kΩ, I_{off} = 0.15 mA, T_A = – 55°C			0.8	V
V_{on}	Output voltage on level	17	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = –55°C			0.4	V
I_{off}	Output off level current	18	V_{CC} = 4.5 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ, . T_A = –55°C			150	μA
I_{on}	Output on level current	19	V_{CC} = 4.5 V, V_{in} = 2 V, V_1 = 1 V, T_A = –55°C	–0.3			mA
$I_{in(0)}$	Logical 0 level input current (each input)	18	V_{CC} = 5.5 V, V_{in} = 0.4 V,			–1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	20	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On level supply current (each gate)	21	V_{CC} = 5 V, V_{in} = 5 V, V_1 = 0.85 V		0.6		mA
$I_{CC(off)}$	Off level supply current (each gate)	21	V_{CC} = 5 V, V_{in} = 0, V_1 = 0.85 V		1		mA

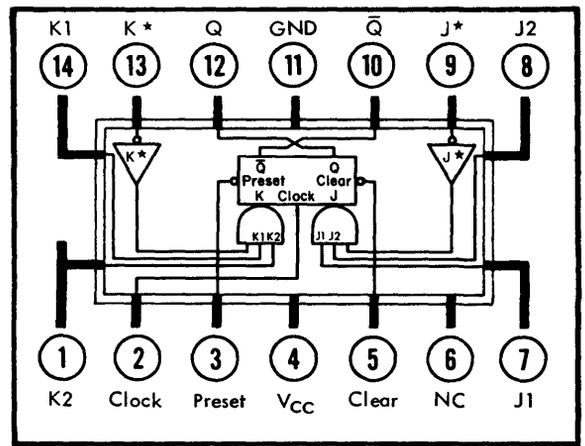
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN5450 or SN5453)	51	C_1 = 15 pF		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN5450 or SN5453)	51	C_1 = 15 pF		20	34	ns

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J\bigstar}$.
2. $K = K1 \cdot K2 \cdot \overline{K\bigstar}$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J★ or K★ are not used they must be grounded.



positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

The SN5470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The SN5470 flip-flop is ideally suited for medium- to high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . . 1 to 10
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 53) . . . . . 5 to 150 ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 53) . . . . . $\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 52) . . . . . $\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 52) . . . . . $\geq$ 25 ns

electrical characteristics, T_A = –55°C to 125°C

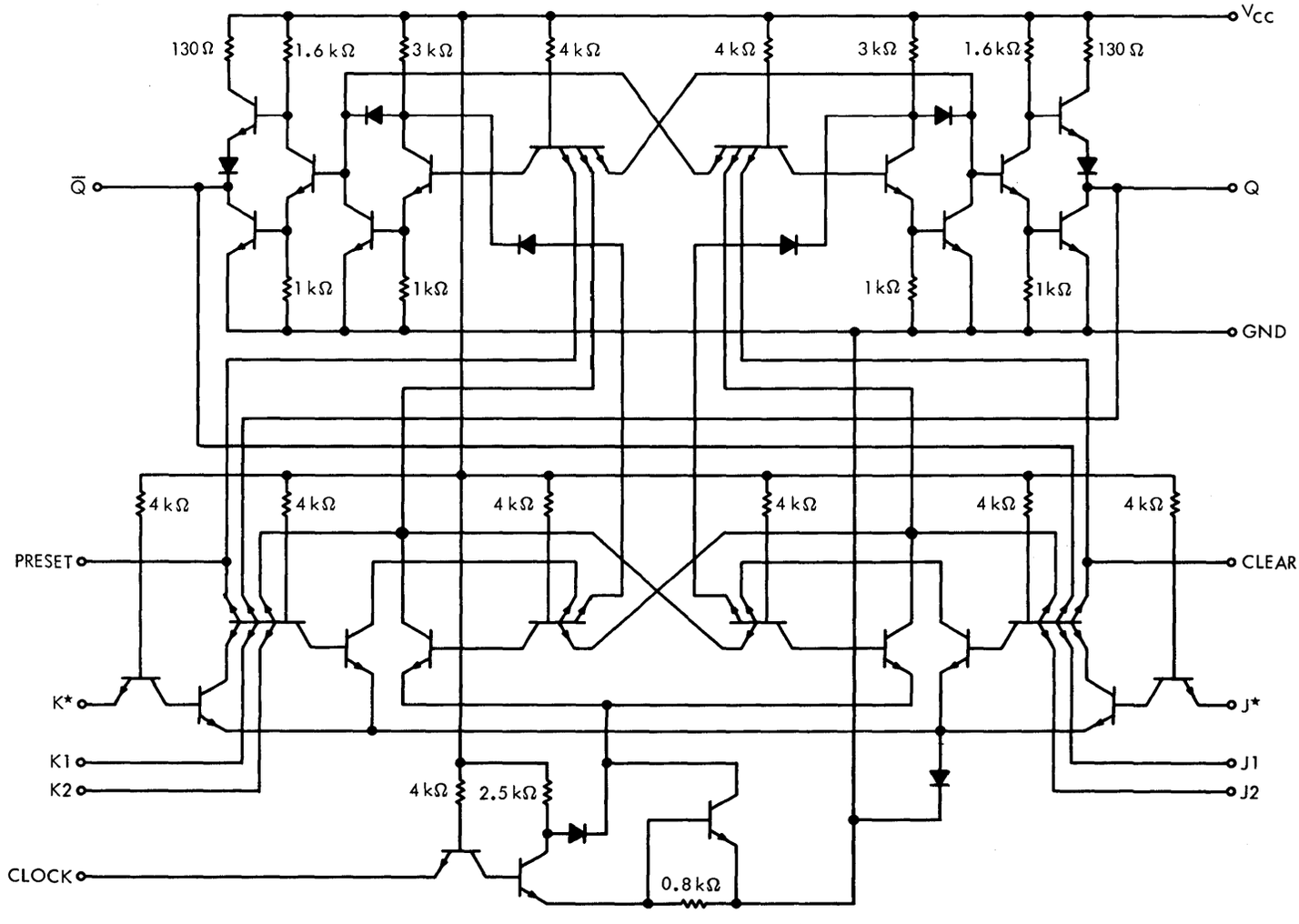
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	22	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	23	V_{CC} = 4.5 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = 4.5 V, I_{load} = –400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	23	V_{CC} = 4.5 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J★, K1, K2, K★, or clock	24	V_{CC} = 5.5 V, V_{in} = 0.4 V			–1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	24	V_{CC} = 5.5 V, V_{in} = 0.4 V			–3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J★, K1, K2, K★, or clock	25	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	25	V_{CC} = 5.5 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	26	V_{CC} = 5.5 V, V_{in} = 0	–20		–57	mA
I_{CC}	Supply current	25	V_{CC} = 5 V, V_{in} = 5 V		13		mA

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	53	C_L = 15 pF	20	35		MHz
t_{setup}	Minimum input setup time	53	C_L = 15 pF		10	20	ns
t_{hold}	Minimum input hold time	53	C_L = 15 pF		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	C_L = 15 pF			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	52	C_L = 15 pF			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	53	C_L = 15 pF	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	53	C_L = 15 pF	10	18	50	ns

schematic



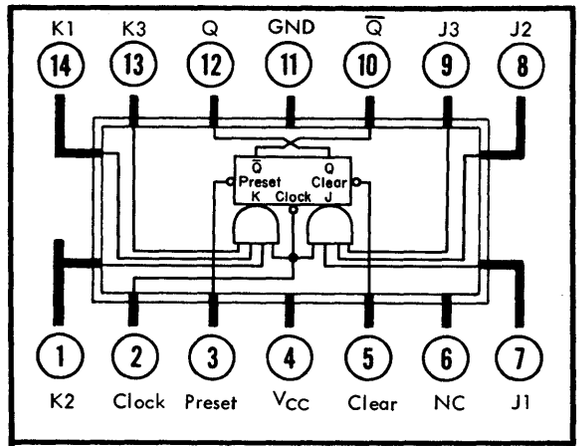
Component values shown are nominal.

TYPE SN5472
J-K MASTER-SLAVE FLIP-FLOP

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

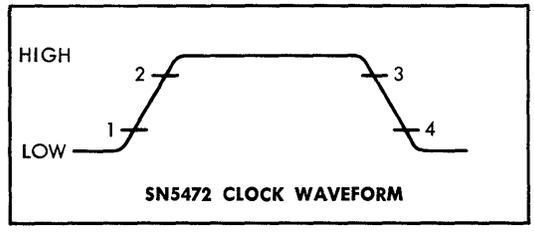


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

The SN5472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



SN5472 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54) . . . . . $\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 55) . . . . . $\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55) . . . . . $\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54) . . . . . $\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . $\geq$ 0

electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	27	$V_{CC} = 4.5$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	27	$V_{CC} = 4.5$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	27	$V_{CC} = 4.5$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	28	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	29	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	29	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	30	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	30	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	31	$V_{CC} = 5.5$ V, $V_{in} = 0$	−20		−57	mA
I_{CC}	Supply current	30	$V_{CC} = 5$ V, $V_{in} = 5$ V		8		mA

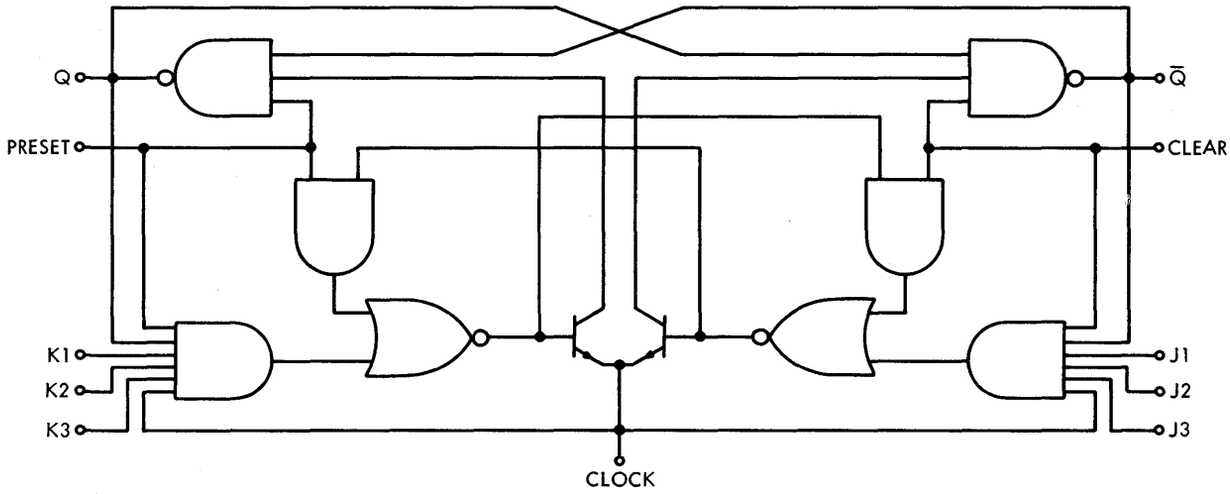
†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

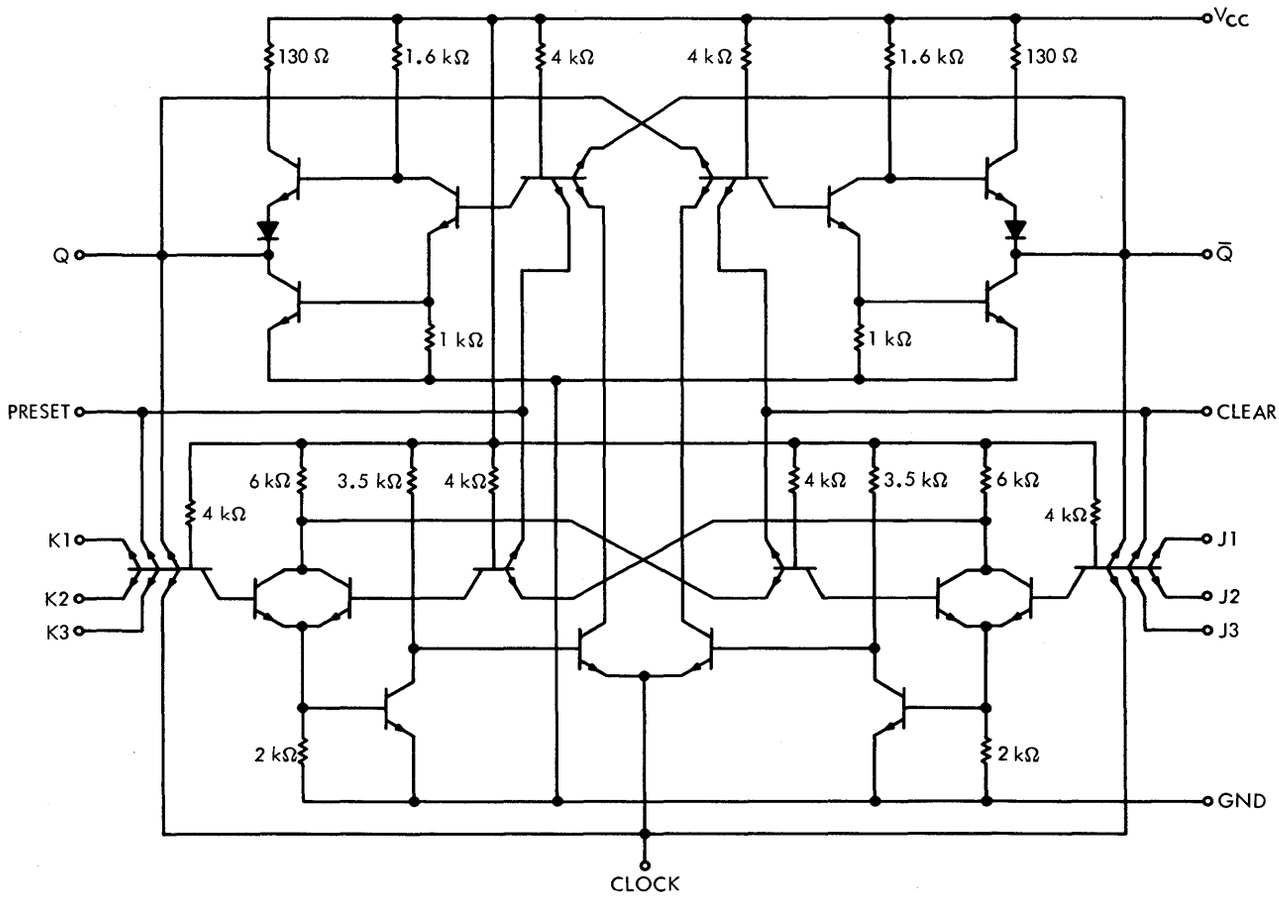
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	$C_l = 15$ pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	55	$C_l = 15$ pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	55	$C_l = 15$ pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	$C_l = 15$ pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	$C_l = 15$ pF	10	34	50	ns

TYPE SN5472
J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



schematic

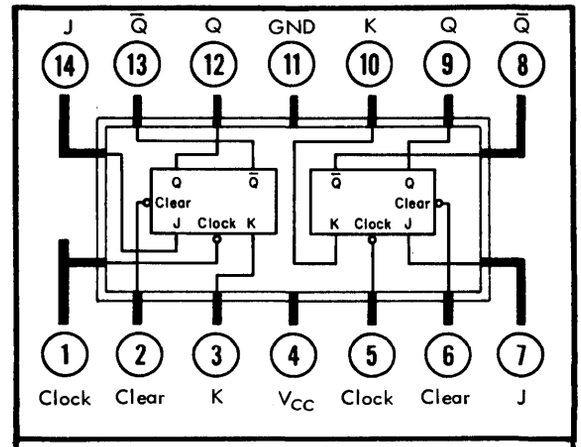


Component values shown are nominal.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



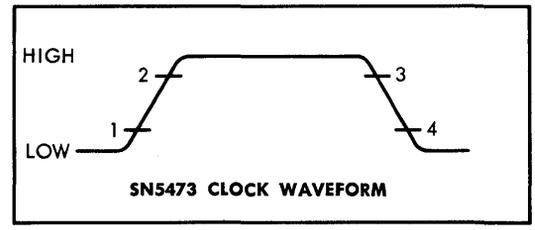
positive logic

Low input to clear sets Q to logical 0
Clear is independent of clock

description

The SN5473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



SN5473 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54)	$\geq$ 20 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55)	$\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54)	$\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold}	$\geq$ 0

electrical characteristics, $T_A = -55°C$ to $125°C$

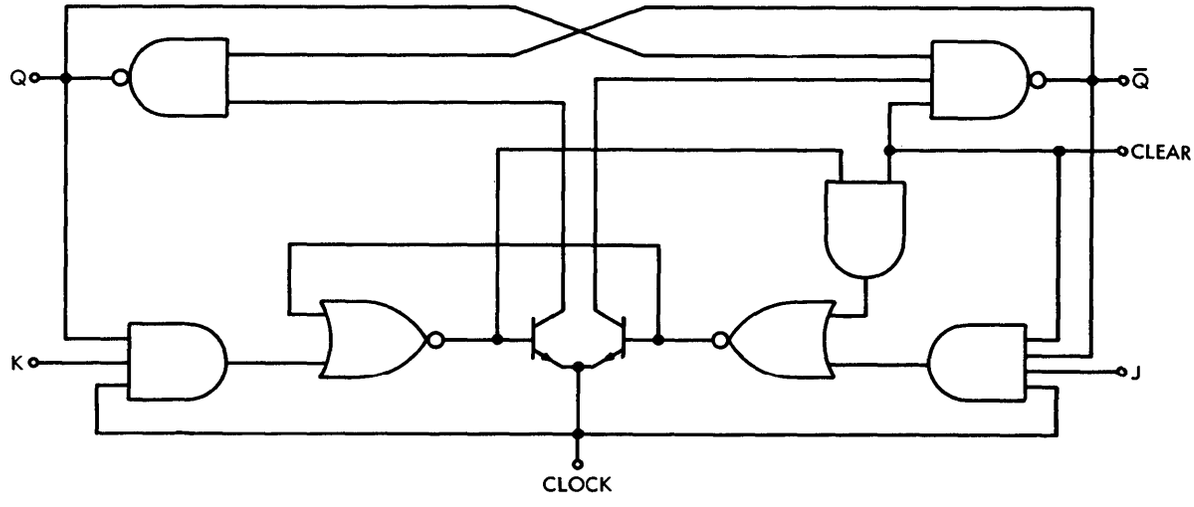
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	32	$V_{CC} = 4.5$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	32	$V_{CC} = 4.5$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	32	$V_{CC} = 4.5$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	33	$V_{CC} = 4.5$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	34	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	34	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	35	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	35	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	36	$V_{CC} = 5.5$ V, $V_{in} = 0$	−20		−57	mA
I_{CC}	Supply current (each flip-flop)	35	$V_{CC} = 5$ V, $V_{in} = 5$ V		8		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

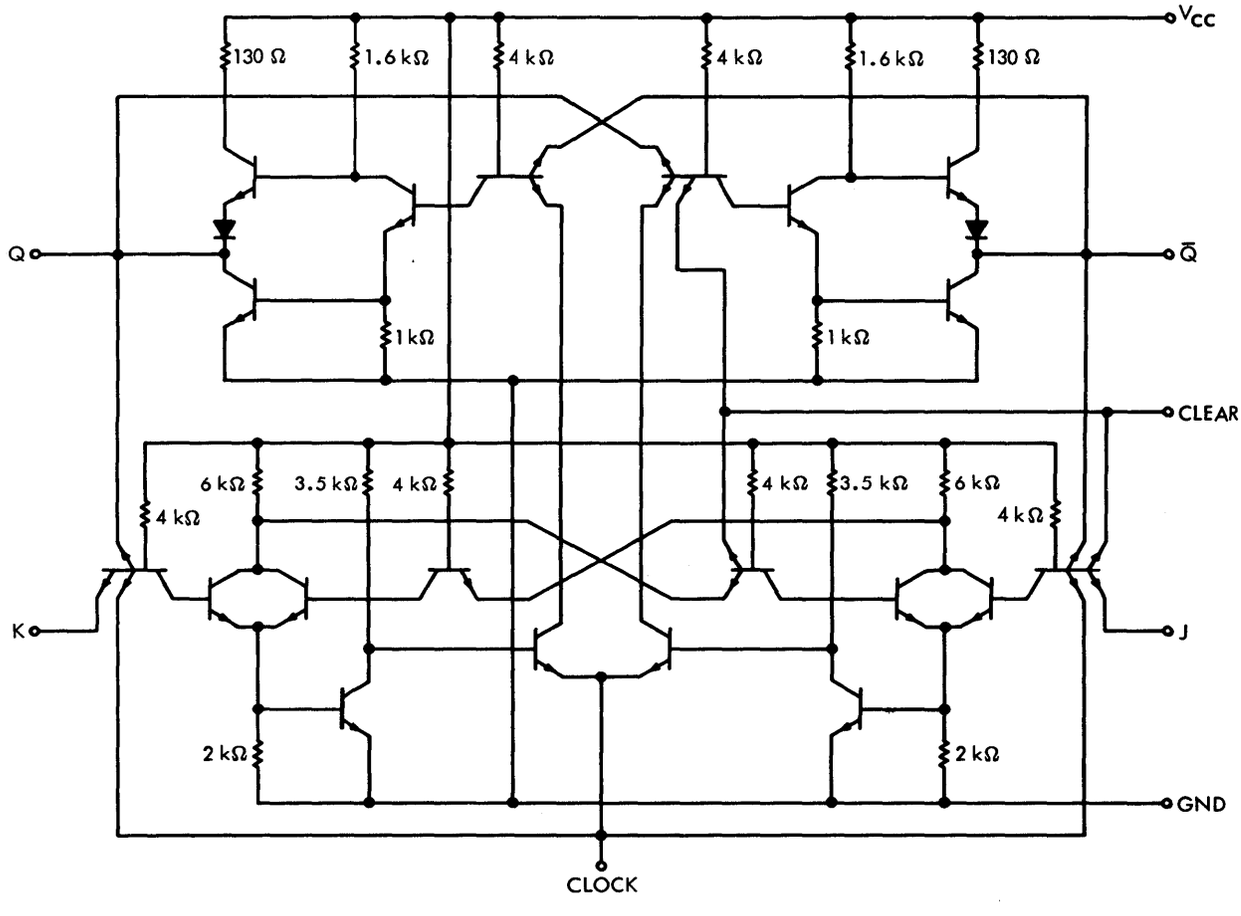
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	$C_1 = 15$ pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	55	$C_1 = 15$ pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	55	$C_1 = 15$ pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15$ pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15$ pF	10	34	50	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

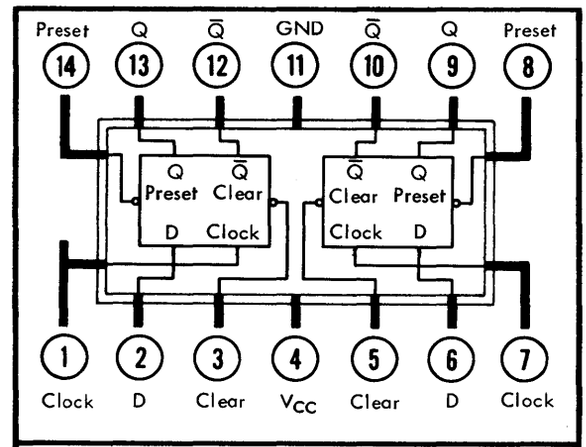
TYPE SN5474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

logic

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.



positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

The SN5474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN5474 dual flip-flop has the same clocking characteristics as the SN5470 gated (edge-triggered) flip-flop and both are ideally suited for medium-to-high-speed applications. The SN5474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 56) . . . . . $\geq$ 30 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 53) . . . . . $\geq$ 30 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 53) . . . . . $\geq$ 30 ns

electrical characteristics, T_A = –55°C to 125°C

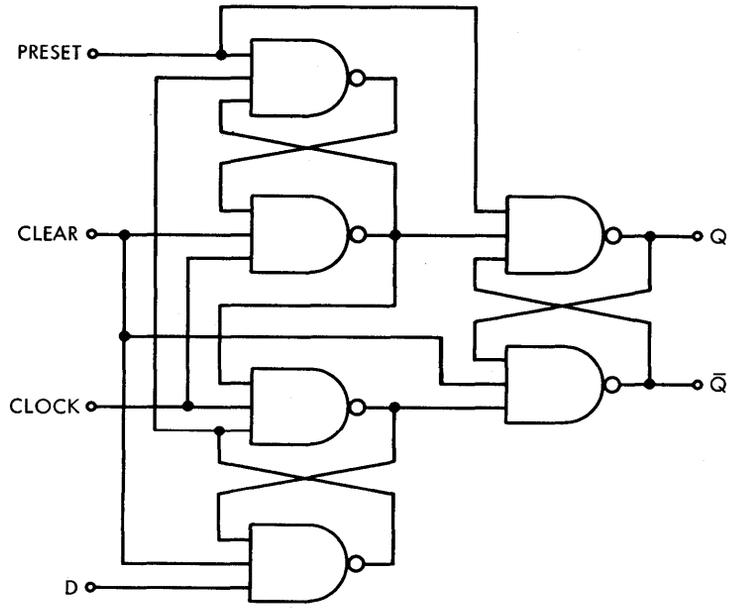
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	37	V_{CC} = 4.5 V		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	37	V_{CC} = 4.5 V				0.8	V
$V_{out(1)}$	Logical 1 output voltage	37	V_{CC} = 4.5 V,	I_{load} = –400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	38	V_{CC} = 4.5 V,	I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	39	V_{CC} = 5.5 V,	V_{in} = 0.4 V			–1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	39	V_{CC} = 5.5 V,	V_{in} = 0.4 V			–3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	40	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	40	V_{CC} = 5.5 V,	V_{in} = 2.4 V			80	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	40	V_{CC} = 5.5 V,	V_{in} = 2.4 V			120	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	41	V_{CC} = 5.5 V,	V_{in} = 0	–20		–57	mA
I_{CC}	Supply current (each flip-flop)	40	V_{CC} = 5.5 V,	V_{in} = 5 V		8.5		mA

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V.

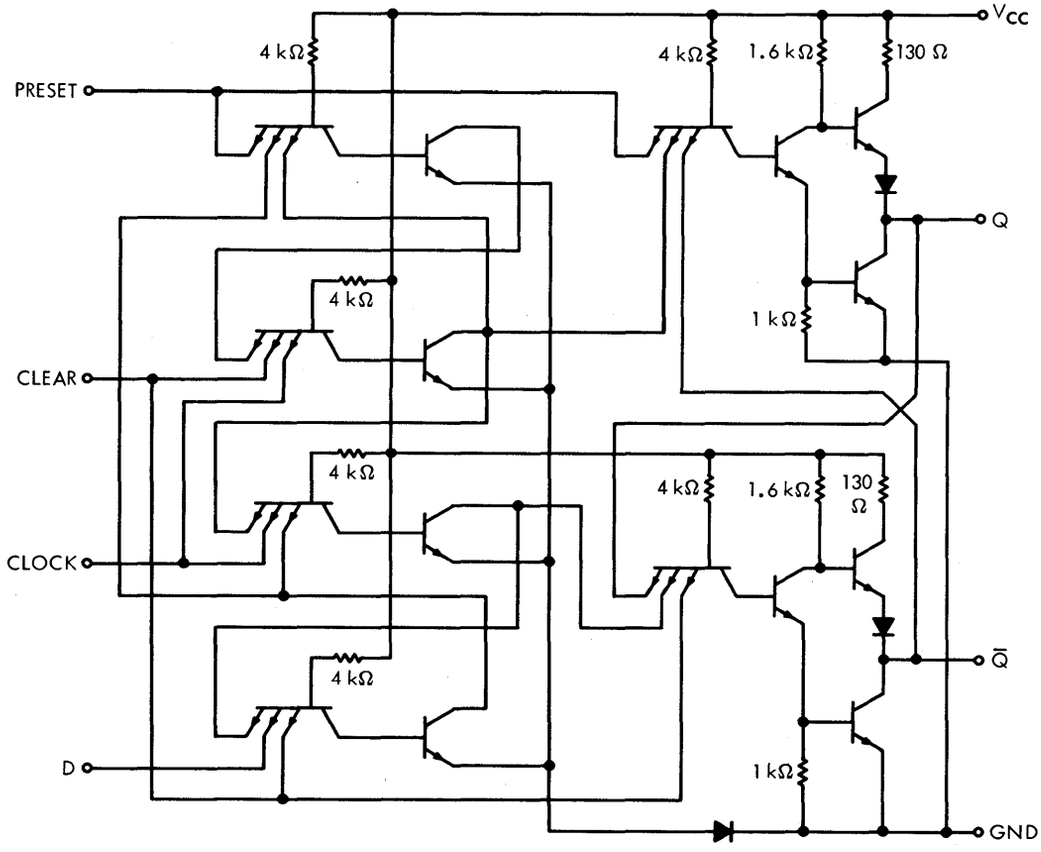
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	56	C_l = 15 pF	15	25		MHz
t_{setup}	Minimum input setup time	56	C_l = 15 pF		15	20	ns
t_{hold}	Minimum input hold time	56	C_l = 15 pF		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	53	C_l = 15 pF			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	53	C_l = 15 pF			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	56	C_l = 15 pF	10	28	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	56	C_l = 15 pF	10	20	50	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



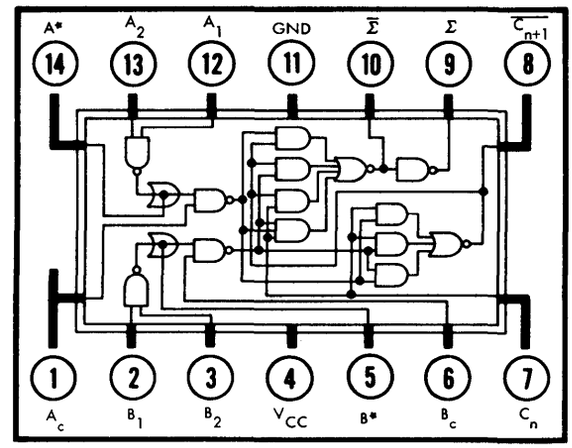
Component values shown are nominal.

logic

TRUTH TABLE (See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES: 1. $A = \overline{A\bigstar \cdot A_c}$, $B = \overline{B\bigstar \cdot B_c}$
where $A\bigstar = \overline{A_1 \cdot A_2}$, $B\bigstar = \overline{B_1 \cdot B_2}$
2. When $A\bigstar$ or $B\bigstar$ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, $A\bigstar$ or $B\bigstar$ respectively must be open or used to perform Dot-OR logic.



description

The SN5480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Allowable Fan-Out From Outputs:

$\overline{C_{n+1}}$, N . . . . . 1 to 5

Σ or $\overline{\Sigma}$, N . . . . . 1 to 10

$A\bigstar$ or $B\bigstar$, N . . . . . 1 to 3

electrical characteristics, $T_A = -55°C$ to $125°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	42 and 43	$V_{CC} = 4.5$ V, $V_{in(0)} = 0.8$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage	42 and 43	$V_{CC} = 4.5$ V, $V_{in(1)} = 2$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	43	$V_{CC} = 4.5$ V	2.4	3.5 ‡		V
$V_{out(0)}$	Logical 0 output voltage	42	$V_{CC} = 4.5$ V		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	44	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A★ or B★	45	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V			−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	45	$V_{CC} = 5.5$ V, $V_{in} = 0.4$ V (all inputs and outputs open)			−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	46	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			15	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	47	$V_{CC} = 5.5$ V, $V_{in} = 2.4$ V			200	μA
			$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$†	48	$V_{CC} = 5.5$ V	−20		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$†	48	$V_{CC} = 5.5$ V	−20		−70	mA
I_{CC}	Supply Current	49	$V_{CC} = 5$ V		21		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	N = 5		13	17	ns
t_{pd0}			2	N = 5		3	7	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	N = 5		18	25	ns
t_{pd0}			4	N = 5		38	55	ns
t_{pd1}	A_C	Σ	5	N = 10		52	70	ns
t_{pd0}			6	N = 10		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	N = 10		38	55	ns
t_{pd0}			8	N = 10		56	75	ns
t_{pd1}	A_1	A★	9	$C_L = 15$ pF		48	65	ns
t_{pd0}			10	$C_L = 15$ pF		17	25	ns
t_{pd1}	B_1	B★	11	$C_L = 15$ pF		48	65	ns
t_{pd0}			12	$C_L = 15$ pF		17	25	ns

¶t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

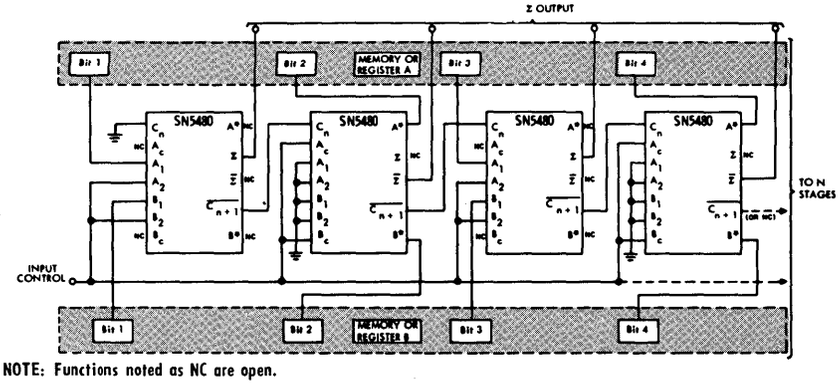
n-bit binary adder or subtractor (see figures F and G)

The SN5480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN5480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (figure F). The inverted carry output is a *true* carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

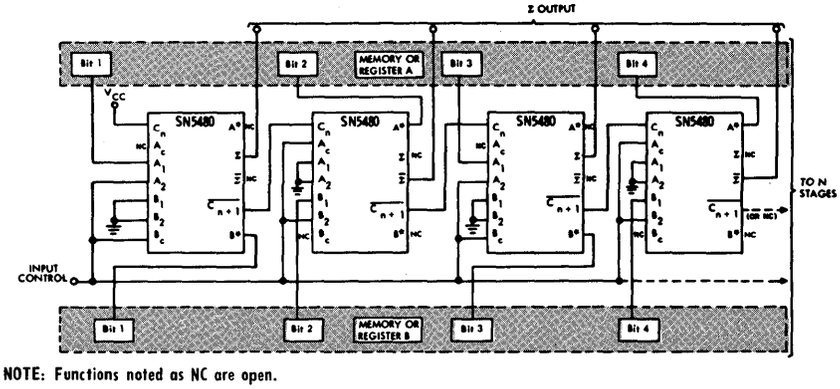
When performing subtraction (figure G) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to A_2 and B_2 of odd-numbered bits and to A_c and B_c of even-numbered bits. For the subtractor (figure G), input control is applied to A_2 and B_c of the odd-numbered bits and to A_c and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE F — N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE G — N-BIT BINARY SUBTRACTOR

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure H)

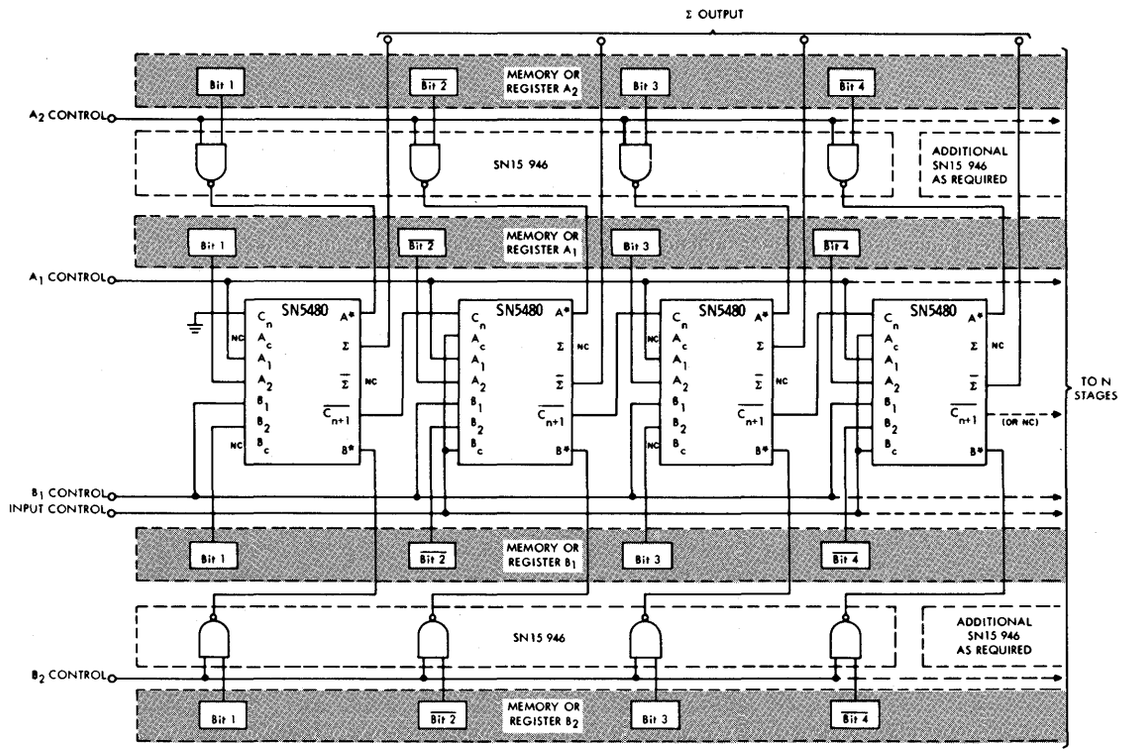
This application fully utilizes the flexibility of the input gating available within the SN5480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1 and externally by a type SN15 946 DTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fan-out rules should be observed.) In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines *and* the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15 946) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

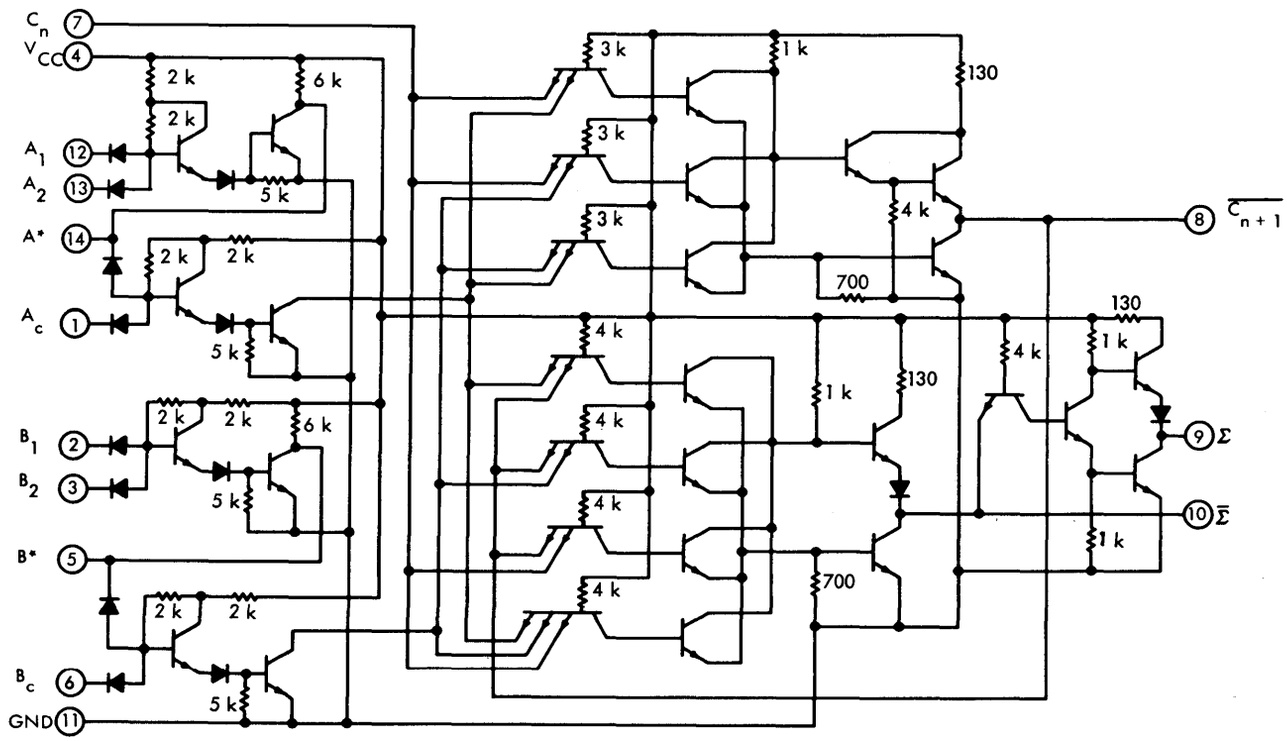
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



NOTE: Functions noted as NC are open.

FIGURE H. N-BIT BINARY ADDER WITH REGISTER SELECTION

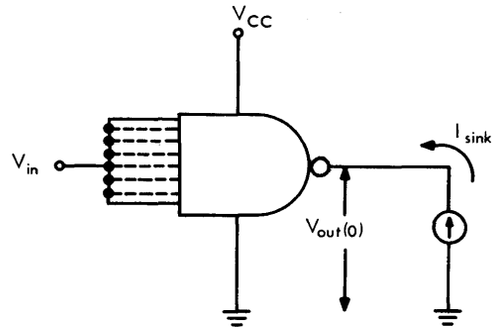
schematic diagram



Component values shown are nominal.
Resistor values are in ohms.

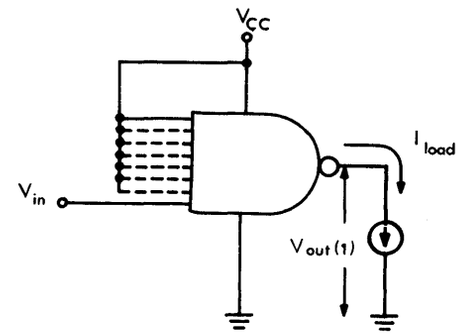
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



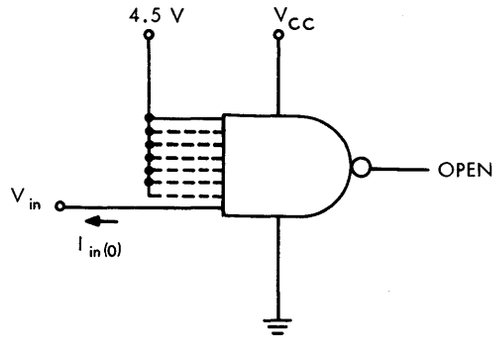
1. All inputs tested simultaneously.

FIGURE 1



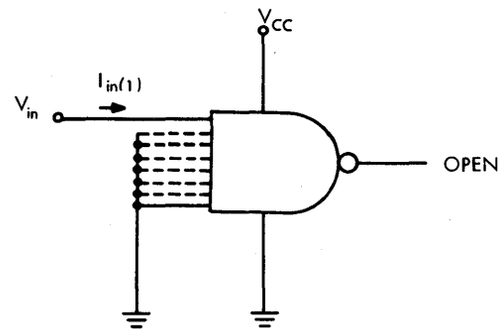
1. Each input tested separately.

FIGURE 2



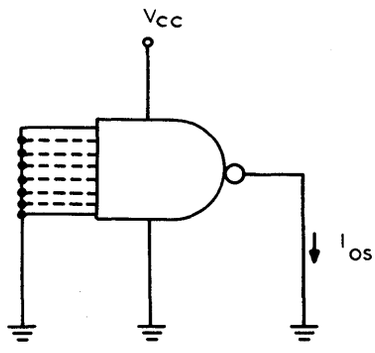
1. Each input tested separately.

FIGURE 3



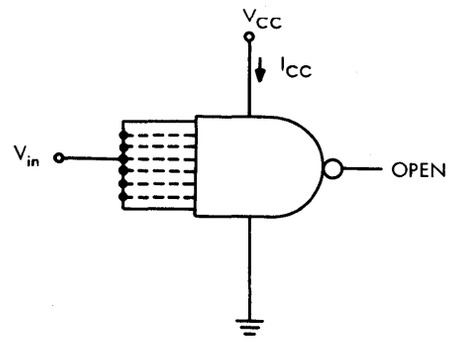
1. Each input tested separately.

FIGURE 4



1. Each gate tested separately.

FIGURE 5



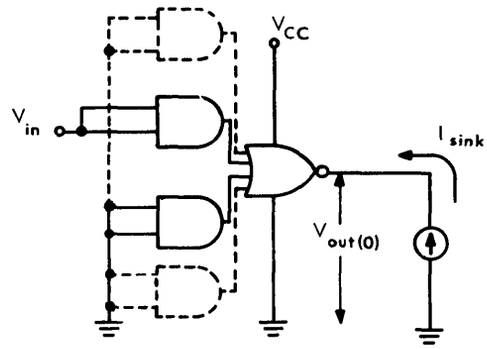
1. Test logical 0 and logical 1 conditions.

FIGURE 6

§Arrows indicate actual direction of current flow.

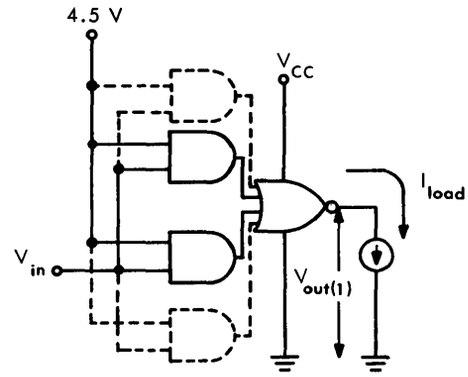
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



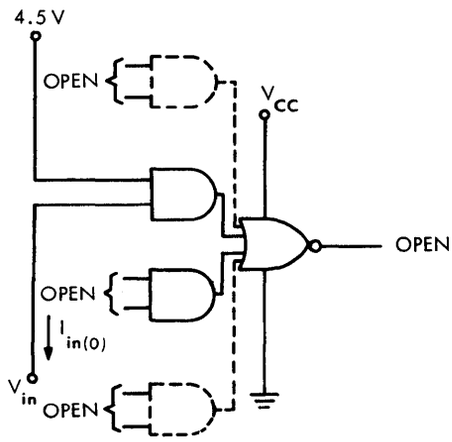
1. Each AND section tested separately.

FIGURE 7



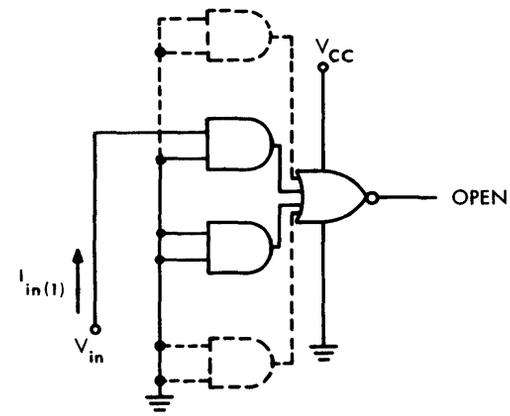
1. Each pair of inputs tested separately.

FIGURE 8



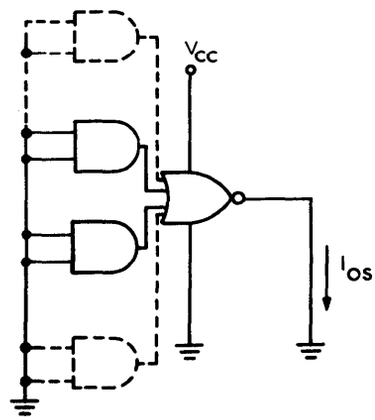
1. Each input tested separately.

FIGURE 9



1. Each input tested separately.

FIGURE 10



1. Each gate tested separately.

FIGURE 11

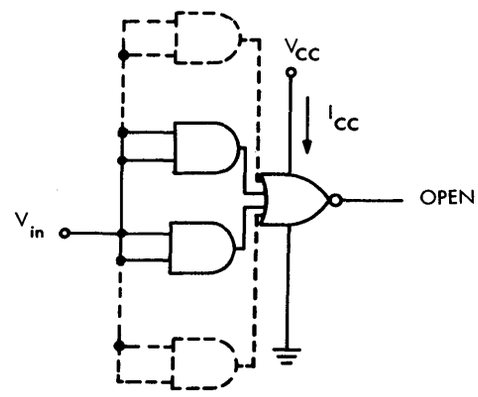


FIGURE 12

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

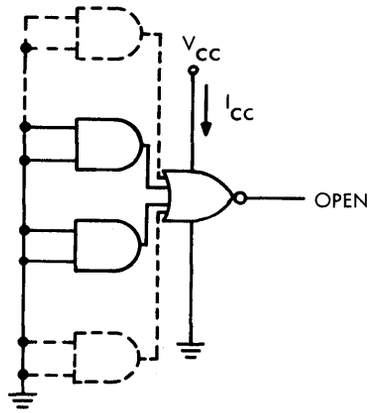


FIGURE 13

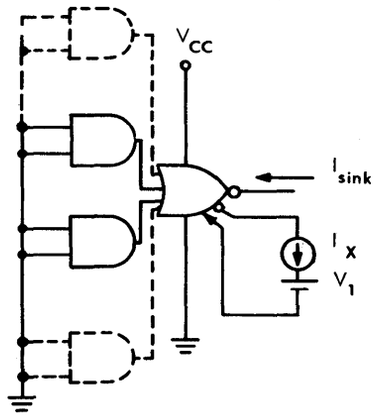


FIGURE 14

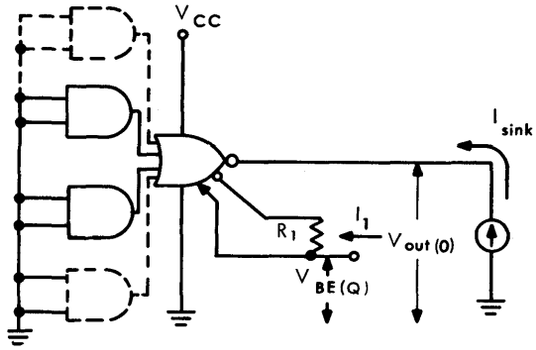


FIGURE 15

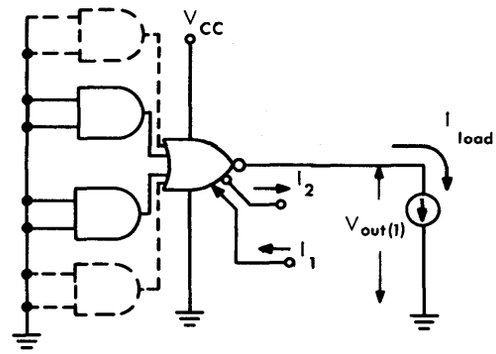
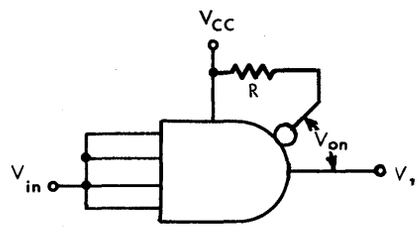
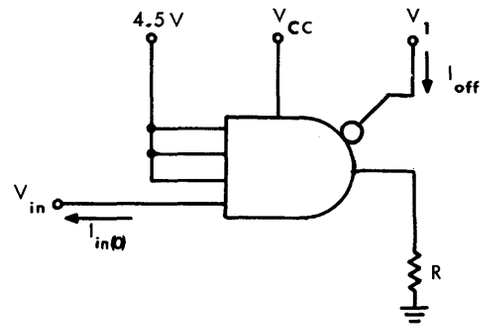


FIGURE 16



1. All inputs tested simultaneously.

FIGURE 17



1. Each input tested separately.

FIGURE 18

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

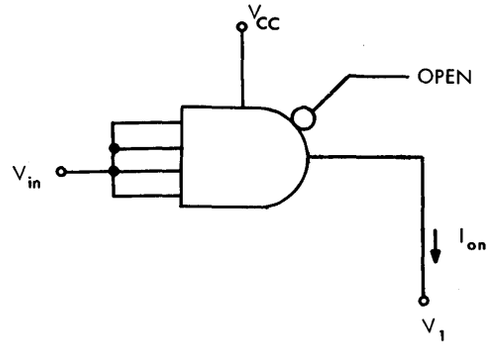
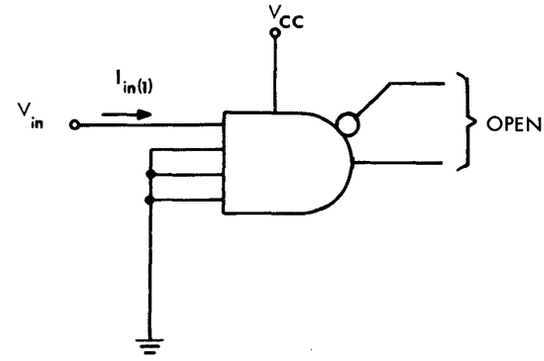
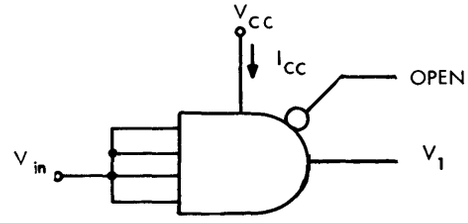


FIGURE 19



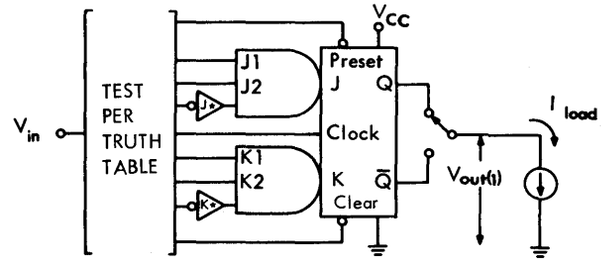
1. Each input tested separately.

FIGURE 20



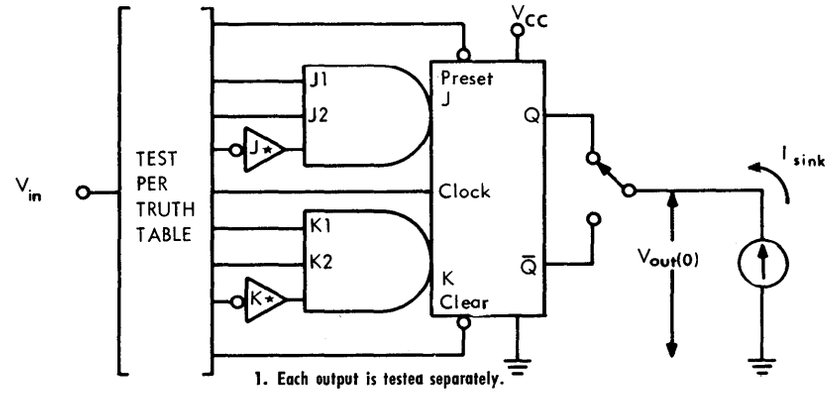
1. Test "on" and "off" conditions.

FIGURE 21



1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 22



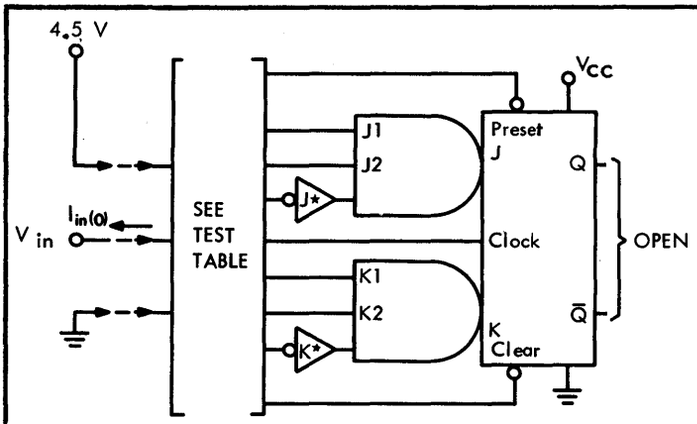
1. Each output is tested separately.

FIGURE 23

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

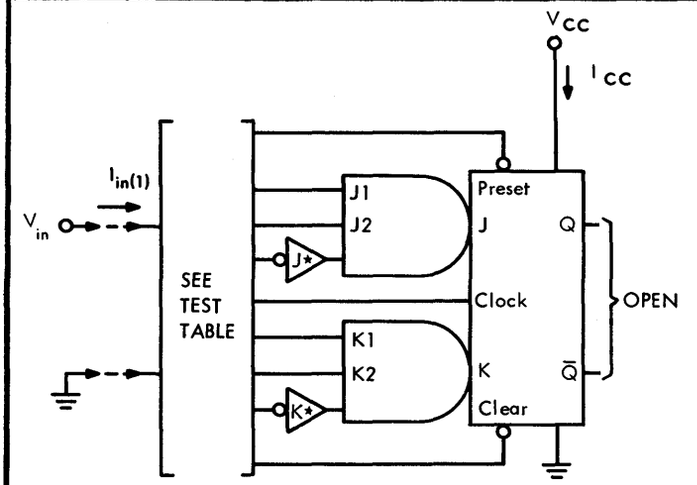
d-c test circuits§ (continued)



TEST TABLE			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J★	Clear
J1	J2	J★	Clear
J★	None	None	None
K2	K1	K★	Preset
K1	K2	K★	Preset
K★	None	None	None
Clock	None	None	None
Preset	K1 and K2	K★	None
Clear	J1 and J2	J★	None

1. Each output is tested separately.

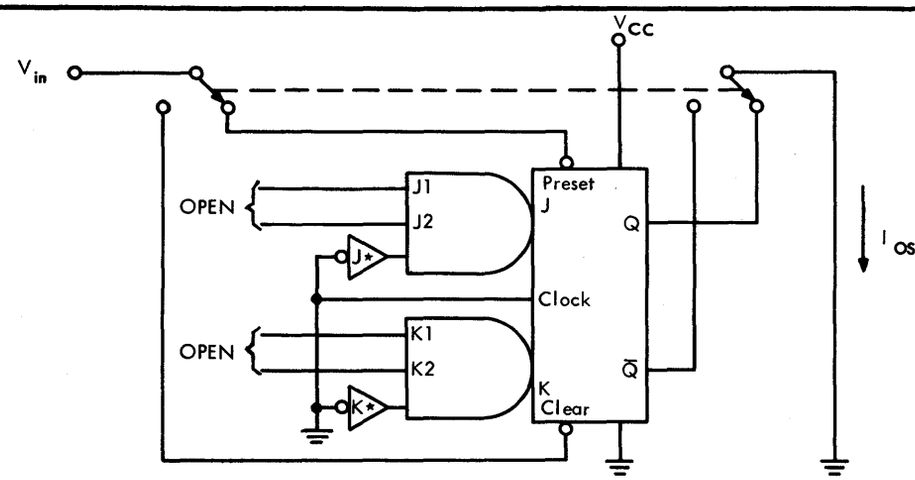
FIGURE 24



TEST TABLE (See Note 2)		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J★
J1	J2 and Clear	J★
J★	None	None
K2	K1 and Preset	K★
K1	K2 and Preset	K★
K★	None	None
Clock	None	None
Preset	K1 and K2	K★
Clear	J1 and J2	J★

1. Each input is tested separately.
2. Test voltage and grounds are applied to inputs in accordance with test table, and $I_{in(1)}$ is measured for input being tested.

FIGURE 25



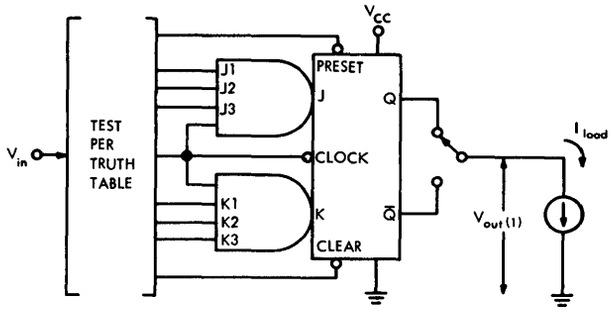
1. Each output is tested separately.

FIGURE 26

§ Arrows indicate actual direction of current flow.

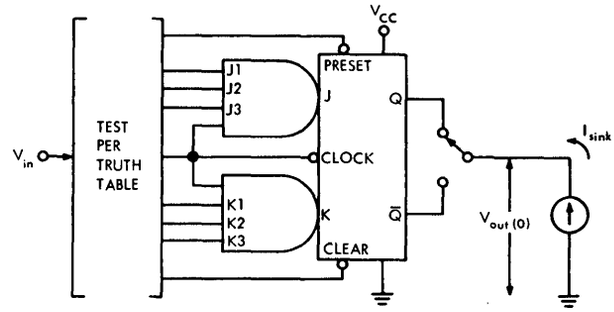
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



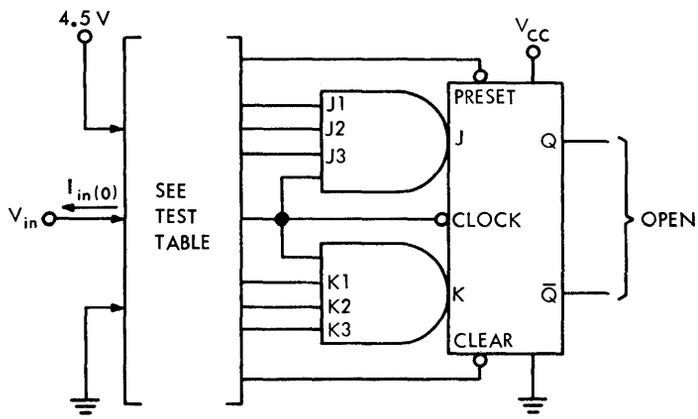
1. Each output is tested separately.

FIGURE 27



1. Each output is tested separately.

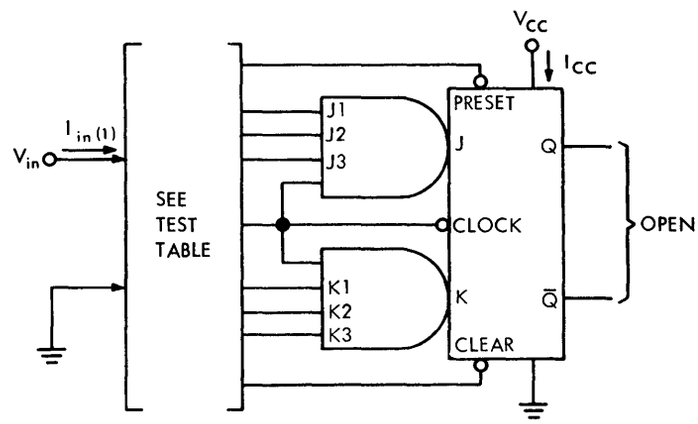
FIGURE 28



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} ($Test_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 29



1. Each input is tested separately.

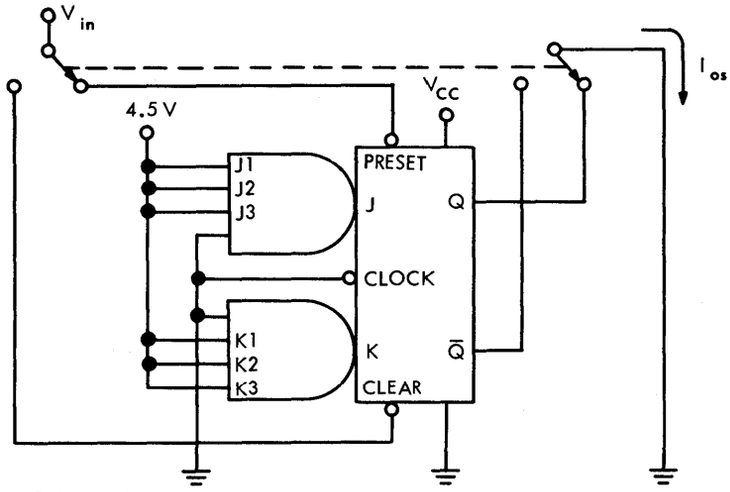
TEST TABLE	
Apply V_{in} ($Test_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 30

§Arrows indicate actual direction of current flow.

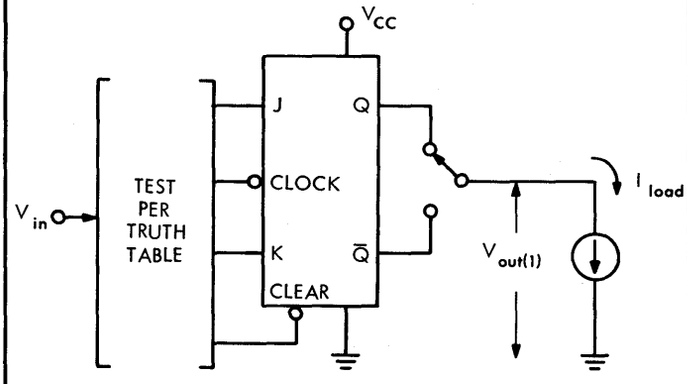
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



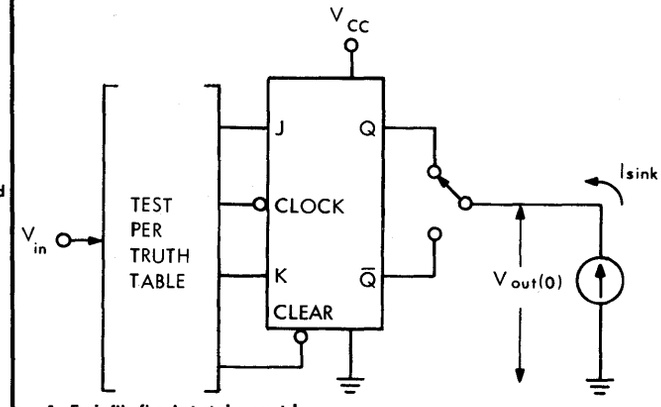
1. Each output is tested separately.

FIGURE 31



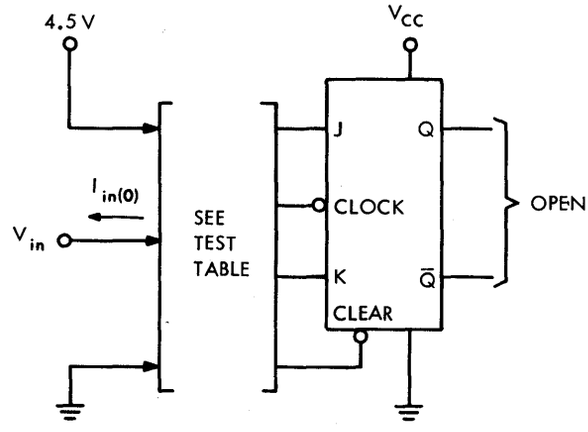
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 32



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 33



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

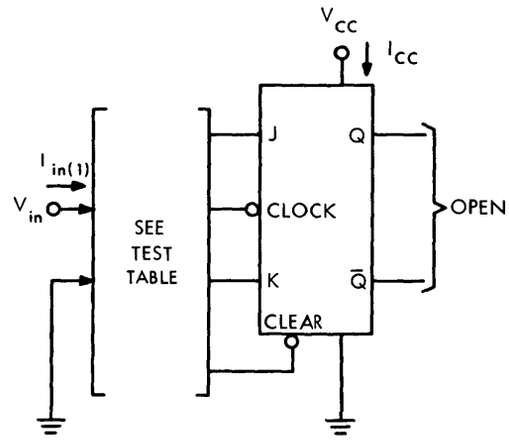
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.

FIGURE 34

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

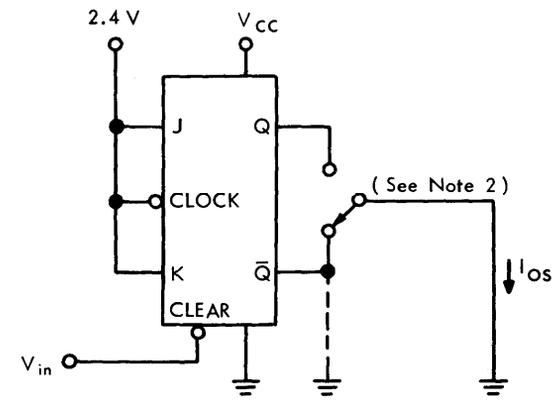
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
J	Clock and Clear	None
K	Clock	Clear

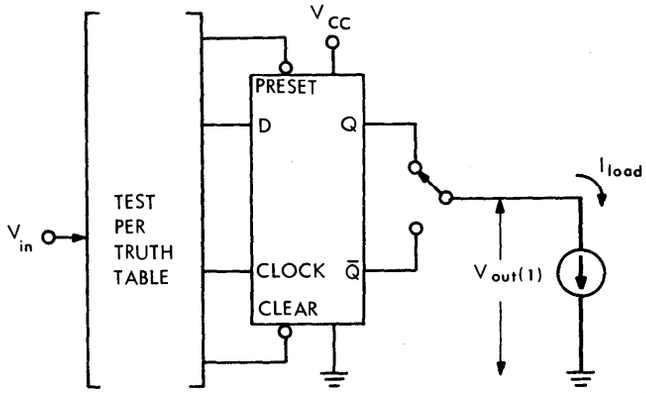
1. Each flip-flop is tested separately.

FIGURE 35



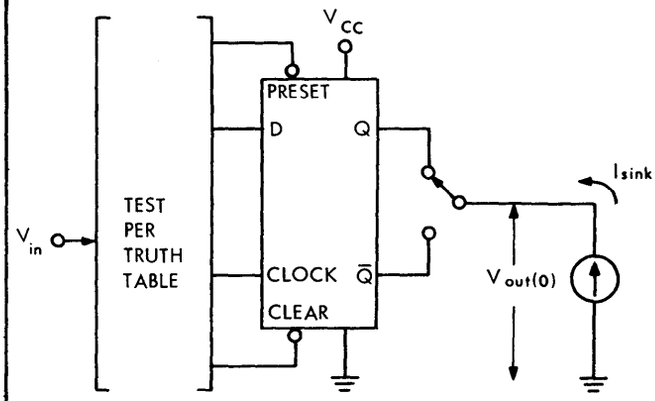
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, open all inputs, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 36



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 37



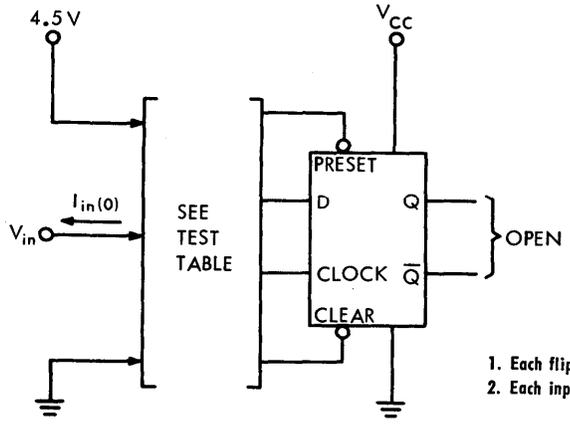
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 38

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

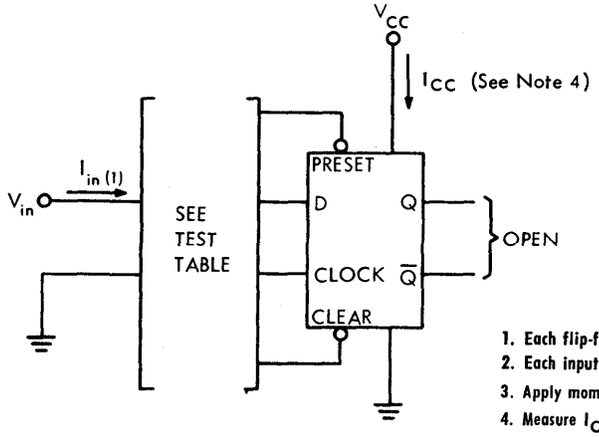
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply GND
Clock	Clear and Preset	D
Preset	Clear and Clock	D
Clear	Clock and D	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

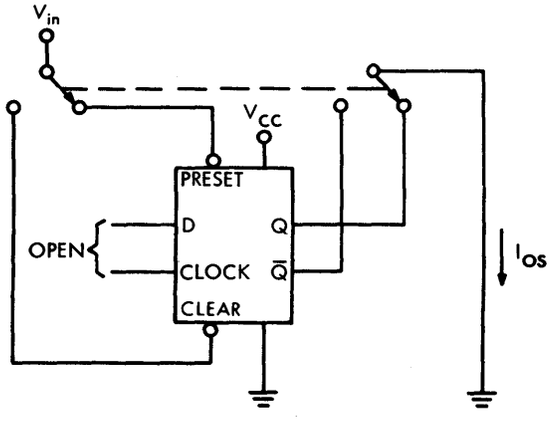
FIGURE 39



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Apply 4.5 V	Apply GND
Clock	None	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	None	D, Clock, and Q
D	Clock	Clear

1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. Apply momentary GND to Clock, then 4.5 V.
4. Measure I_{CC} with D and clock input at GND.

FIGURE 40



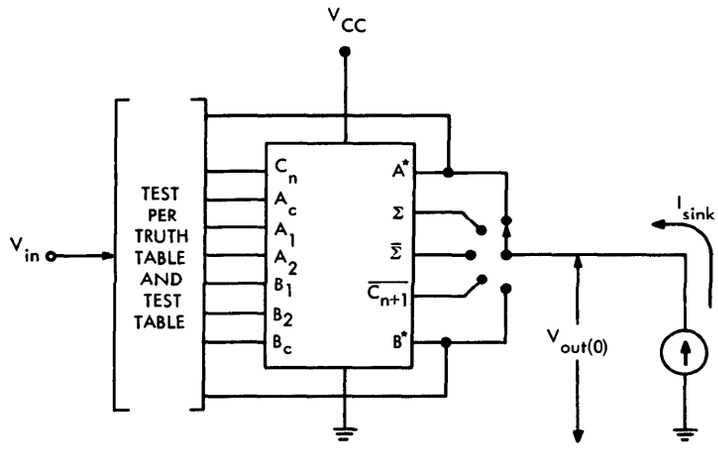
1. Each output is tested separately.

FIGURE 41

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)

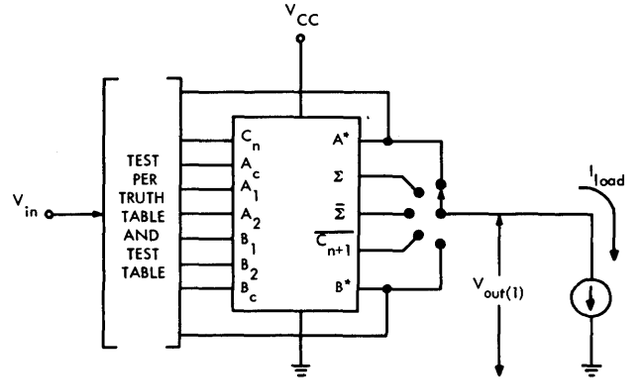


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ_i or $\overline{\Sigma_i}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 42



TEST TABLE

Output Under Test	I_{load} (Min)
Σ_i or $\overline{\Sigma_i}$	-400 μA
$\overline{C_n + 1}$	-200 μA
A★ or B★	-120 μA

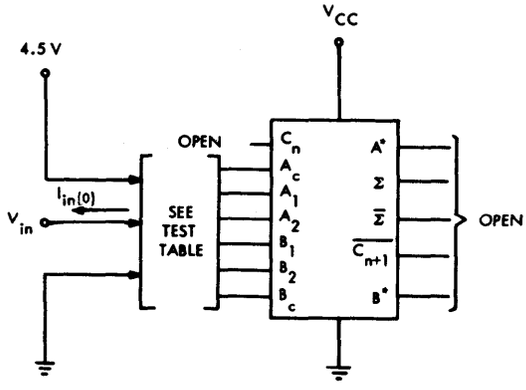
1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

FIGURE 43

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§(continued)

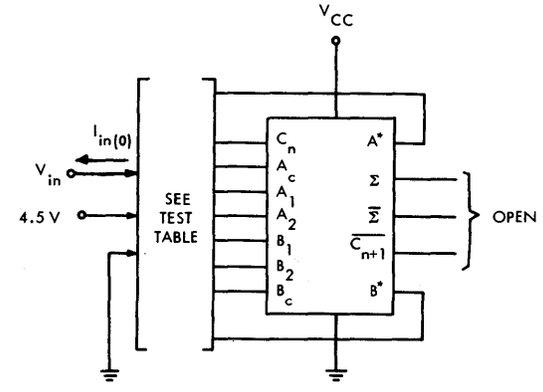


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_C	None	A_1 and A_2
B_C	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 44



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_C	A_1 and A_2
B★	B_C	B_1 and B_2
C_n	None	None

Unused inputs are open.

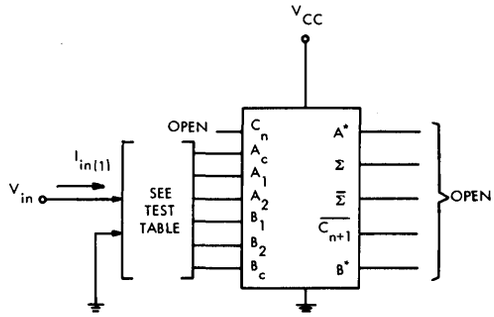
1. Each input is tested separately.

FIGURE 45

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§(continued)



TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

1. Each input is tested separately.

FIGURE 46

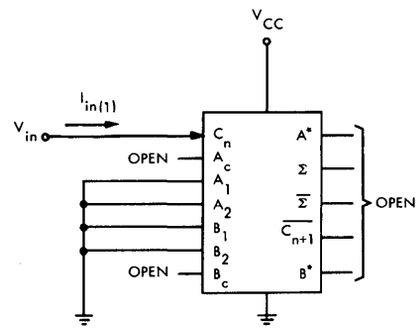
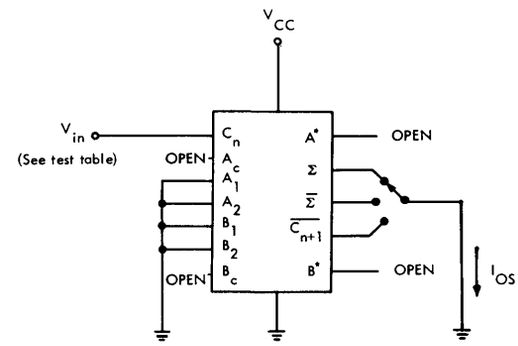


FIGURE 47



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C_{n+1}}$	GND

FIGURE 48

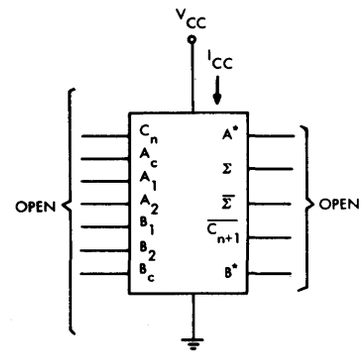
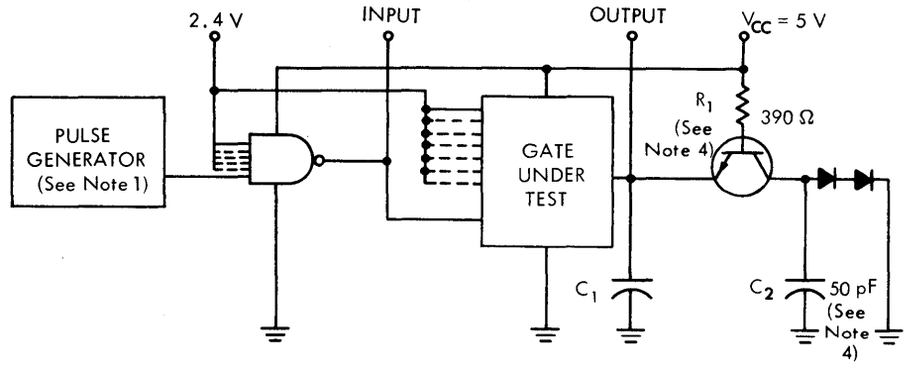


FIGURE 49

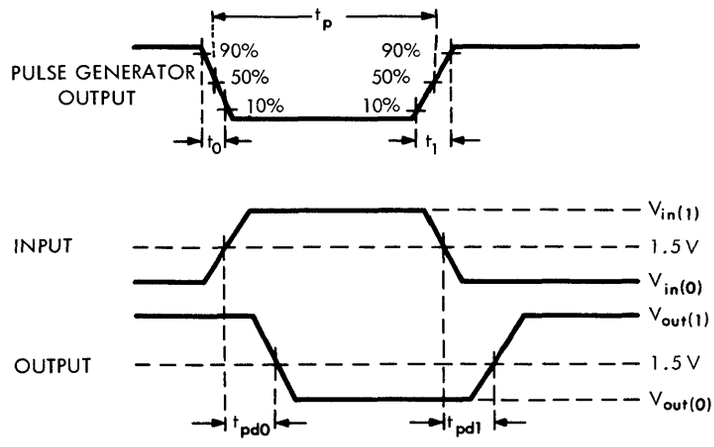
§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



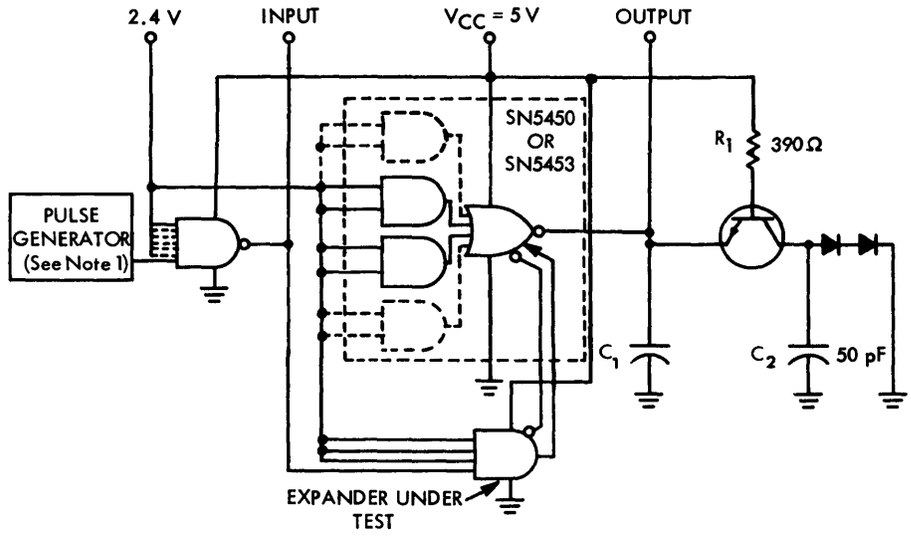
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_0 = t_1 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. Test SN5440 with $R_1 = 130\ \Omega$, $C_2 = 150$ pF.
5. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
6. C_1 includes probe and jig capacitance.

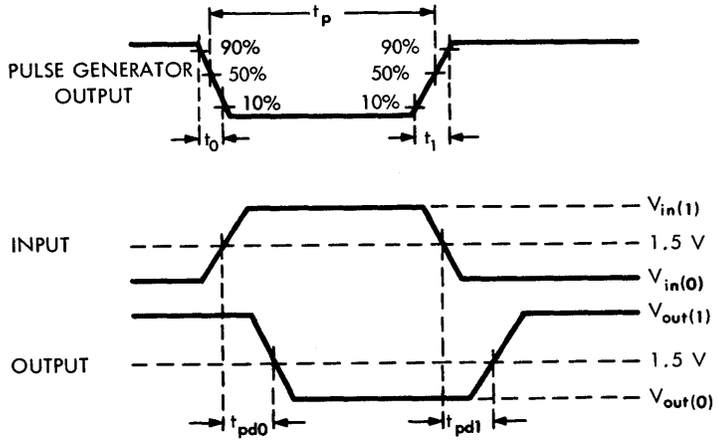
FIGURE 50 — GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



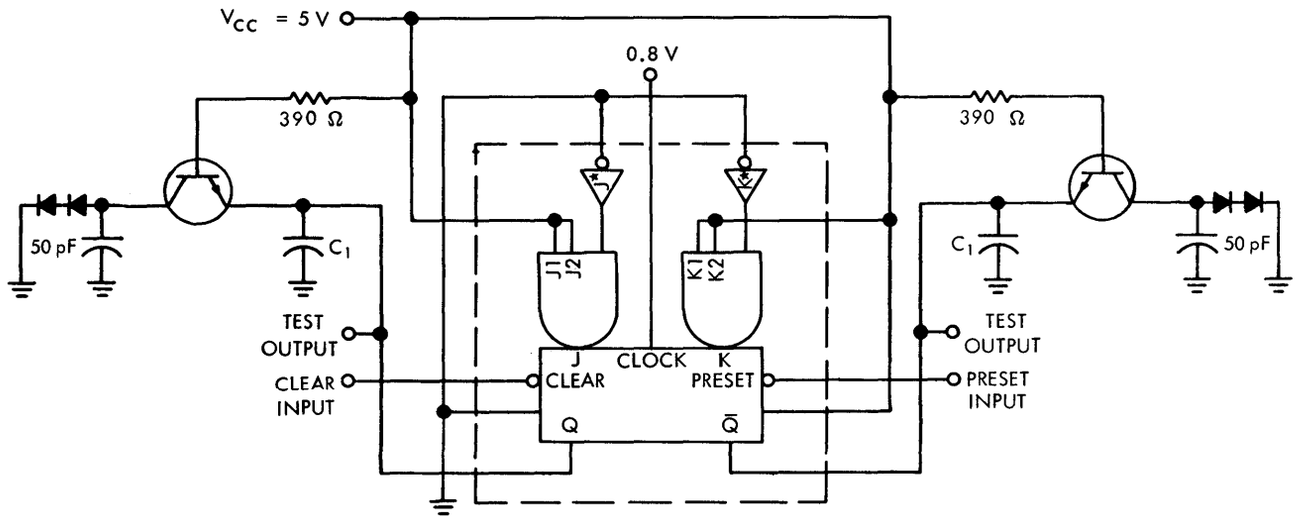
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_0 = t_1 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
5. C_1 includes probe and jig capacitance.

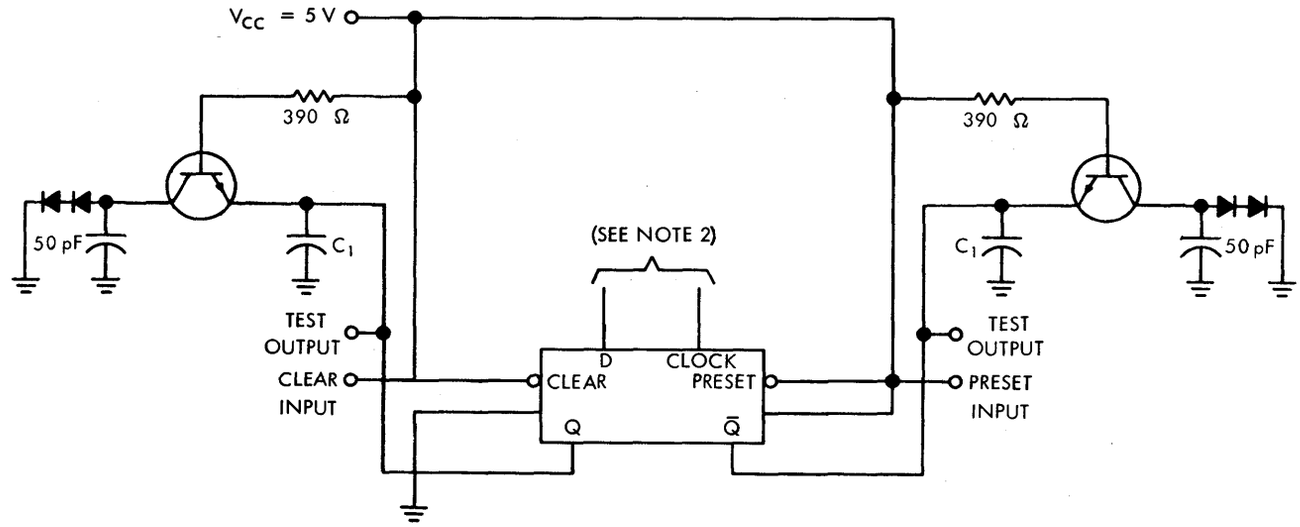
FIGURE 51 — EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT SN5470



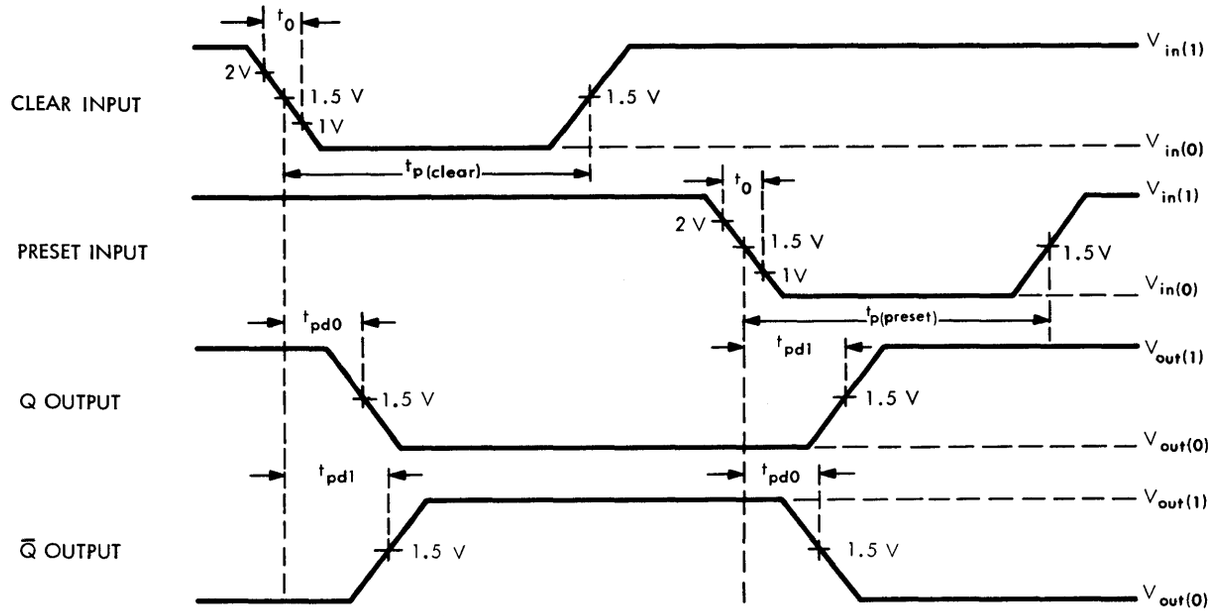
TEST CIRCUIT SN5474

NOTES: 1. Present or clear function of the SN5470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the SN5474 dominate regardless of the state of clock or D inputs.
3. All transistors are 2N2368.
4. All diodes are 1N916.
5. C_l includes probe and jig capacitance.

FIGURE 52 — SN5470 AND SN5474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



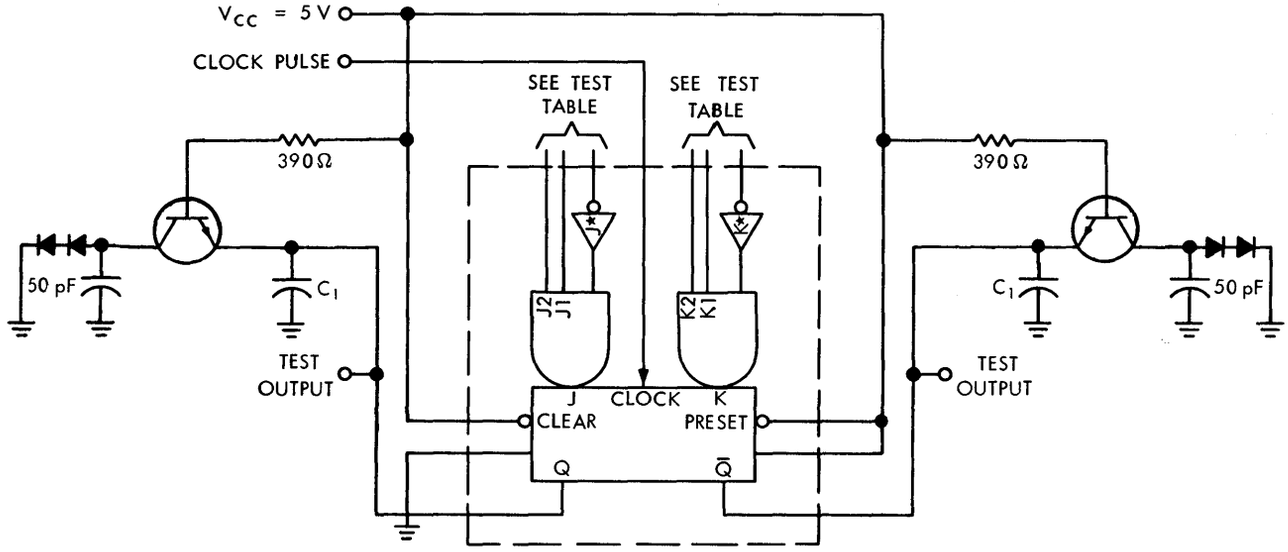
VOLTAGE WAVEFORMS

NOTE 6: Clear or preset input pulse characteristics: $V_{in(0)} = 0.4$ V, $V_{in(1)} = 2.4$ V, $t_0 = 3$ to 6 ns, $t_p = 25$ ns for the SN5470, and $t_p = 30$ ns for SN5474.

FIGURE 52—SN5470 AND SN5474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)

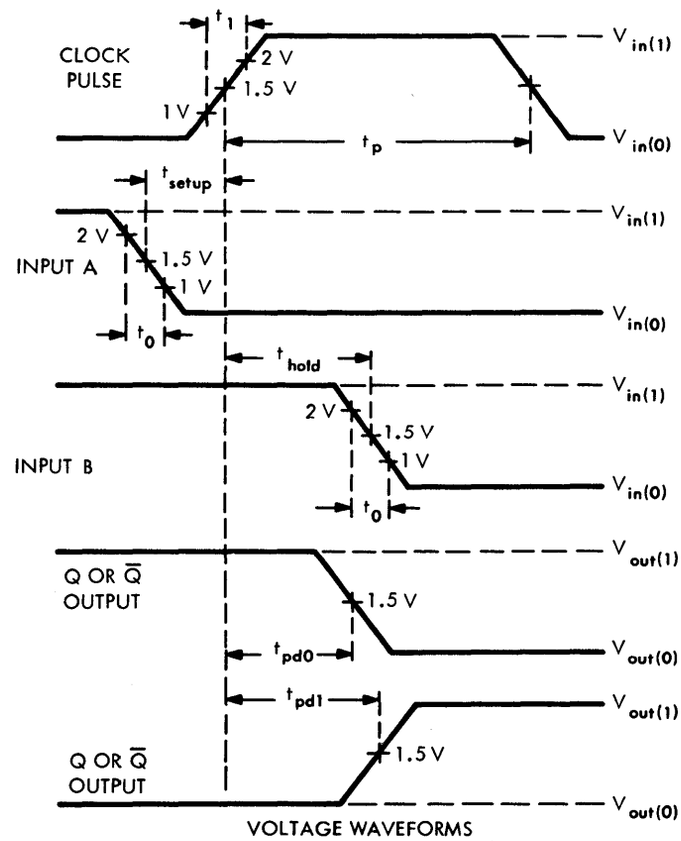
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY + 2.4 V	GND
1	t_{setup} at J★	J★	None	J1, J2, K1, K2	K★
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	t_{setup} at K★	K★	None	J1, J2, K1, K2	J★
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J★ and K★

NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, t_1 = 15 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.
4. Input pulse characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, t_0 = 3 to 6 ns.
5. All transistors are 2N2368.
6. All diodes are 1N916.
7. C_1 includes probe and jig capacitance.

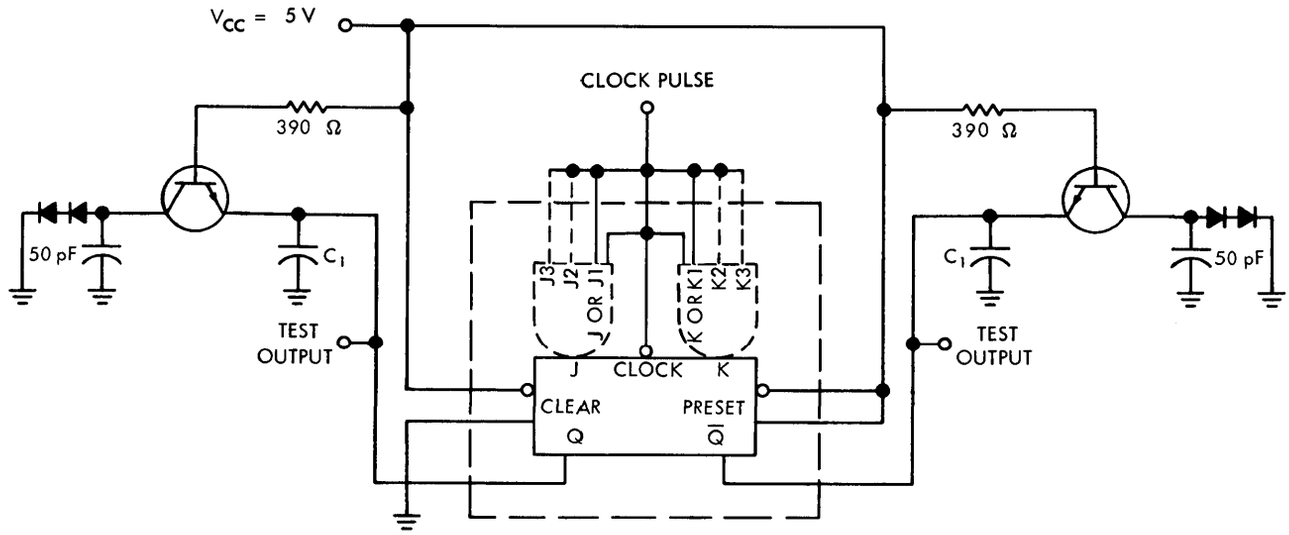


VOLTAGE WAVEFORMS

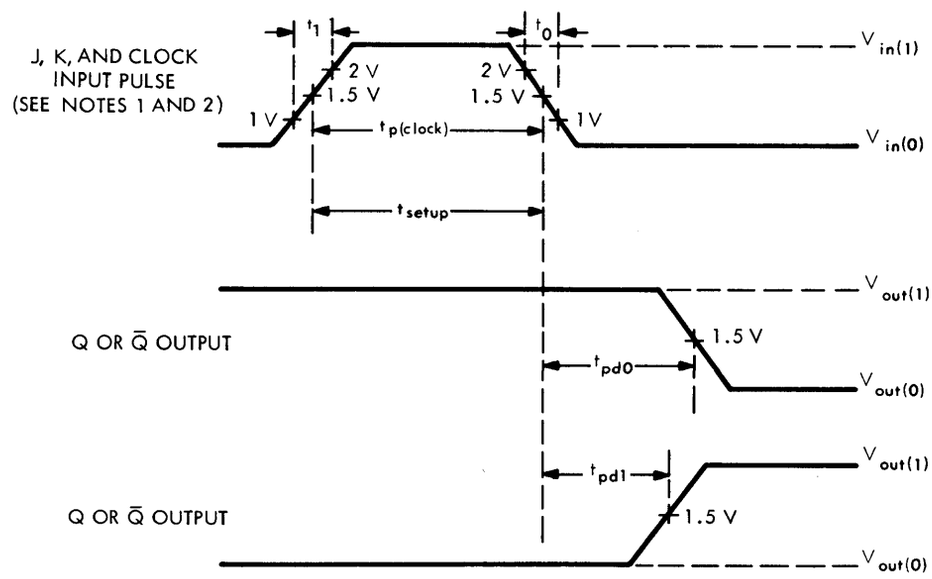
FIGURE 53 — SN5470 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

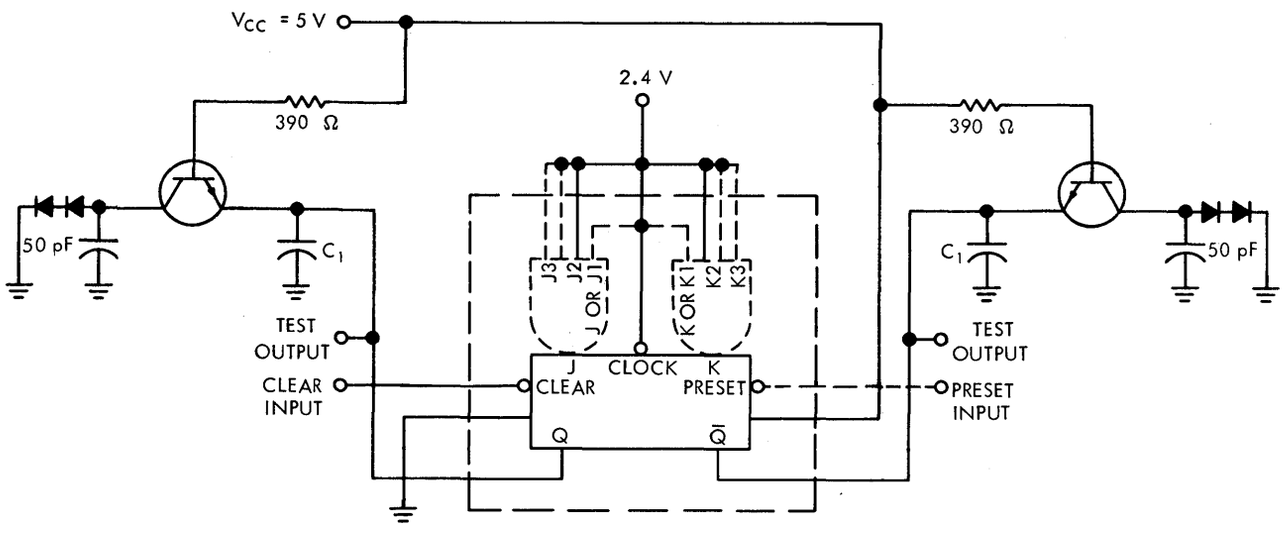
NOTES: 1. Clock, J, and K input pulse characteristics: $V_{in(0)}$ = 0.4 V, $C_{in(1)}$ = 2.4 V, t_1 = t_0 = 15 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. For the SN5472, J = J1 • J2 • J3 and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the SN5472 only. The SN5473 Dual Flip-Flop has direct J and K inputs and preset is not available.
4. All transistors are 2N2368.
5. All diodes are 1N916.
6. C_1 includes probe and jig capacitance.

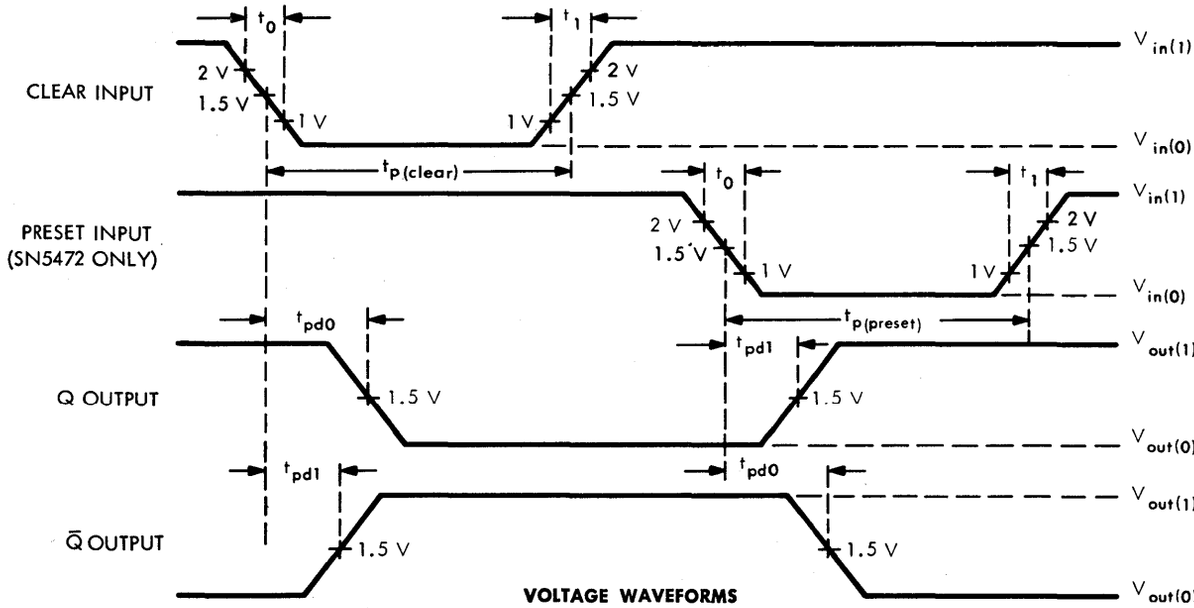
FIGURE 54 — SN5472, SN5473 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



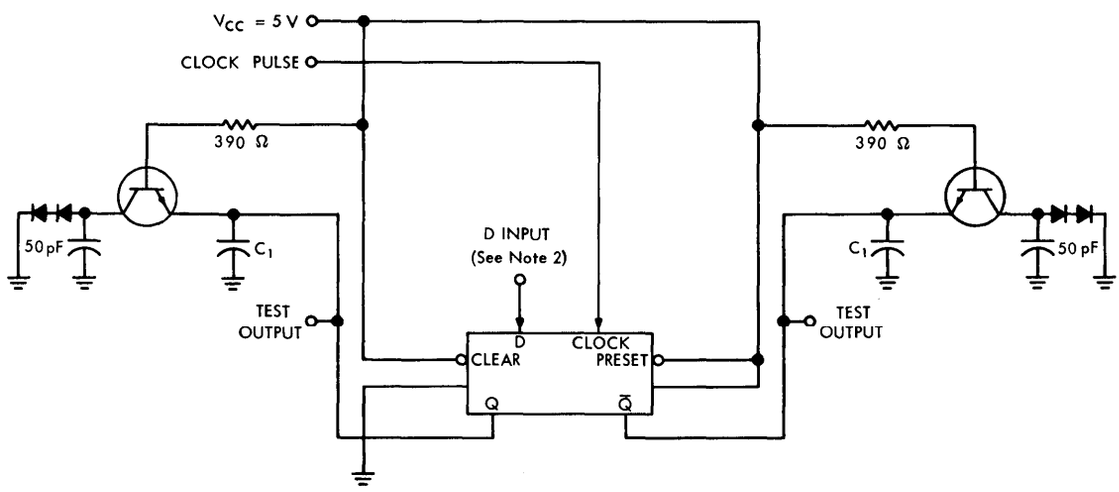
VOLTAGE WAVEFORMS

NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2. Clear or preset input pulse characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, t_1 = t_0 = 15 ns, $t_{p(clear)}$ = $t_{p(preset)}$ = 25 ns, and PRR = 1 MHz.
3. Gated inputs (shown with dotted lines) are for the SN5472 only. The SN5473 Dual Flip-Flop has direct J and K inputs and preset is not available.
4. All transistors are 2N2368.
5. All diodes are 1N916.
6. C_1 includes probe and jig capacitance.

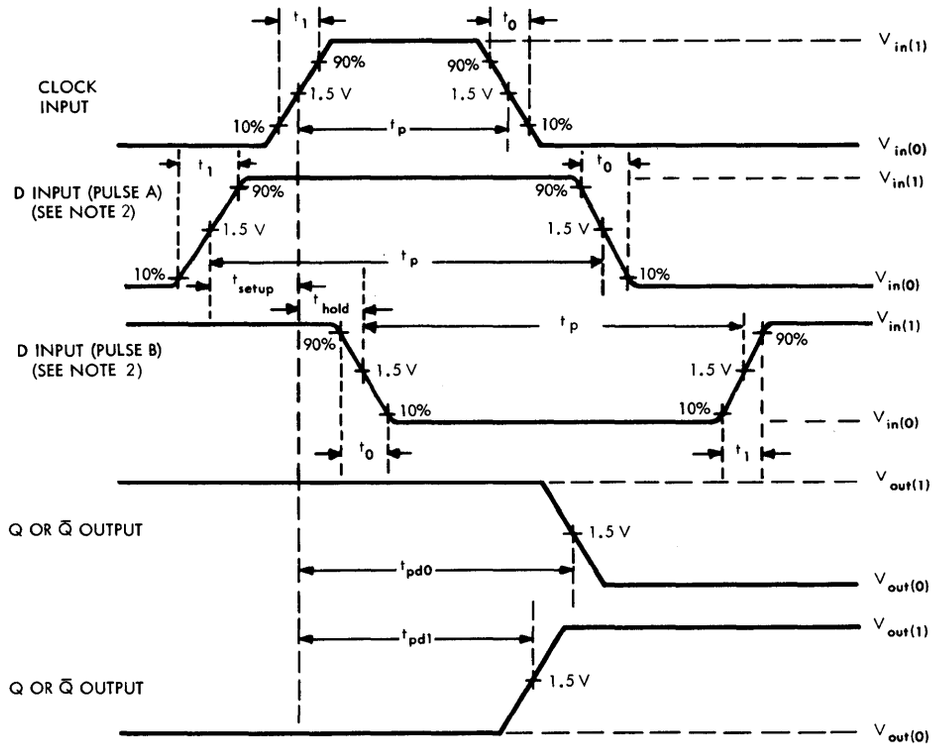
FIGURE 55 — SN5472 AND SN5473 PRESET/CLEAR PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Clock input pulse has the following characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, $t_1 = t_0$ = 15 ns, t_p = 30 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. D input (pulse A) is used to measure t_{pd1} at Q and t_{pd0} at $\bar{Q}$. Pulse B is used to measure t_{pd1} at $\bar{Q}$ and t_{pd0} at Q. D input (pulse A) has the following characteristics: $t_1 = t_0$ = 15 ns, t_{setup} = 20 ns, t_p = 60 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $t_1 = t_0$ = 15 ns, t_{hold} = 5 ns, t_p = 60 ns, and PRR is 50% of the clock PRR.

3. All transistors are 2N2368.

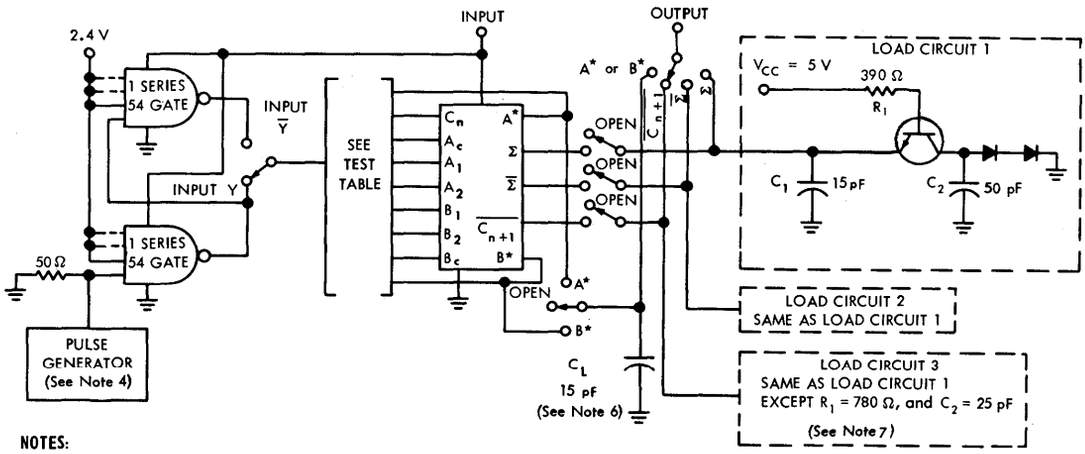
4. All diodes are 1N916.

5. C_1 includes probe and jig capacitance.

FIGURE 56 — SN5474 FLIP-FLOP SWITCHING TIME

PARAMETER MEASUREMENT INFORMATION

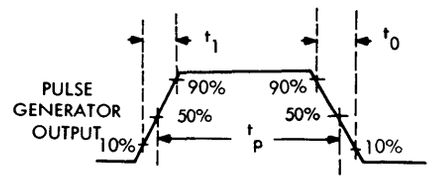
switching characteristics (continued)



NOTES:

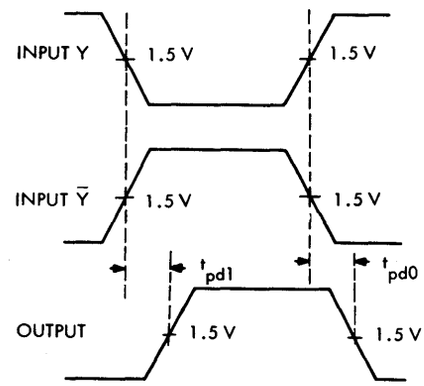
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L and C_1 include probe and jig capacitance.
7. Load circuit 3 simulates output load of 5.
8. All transistors are 2N2368.
9. All diodes are 1N916.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)

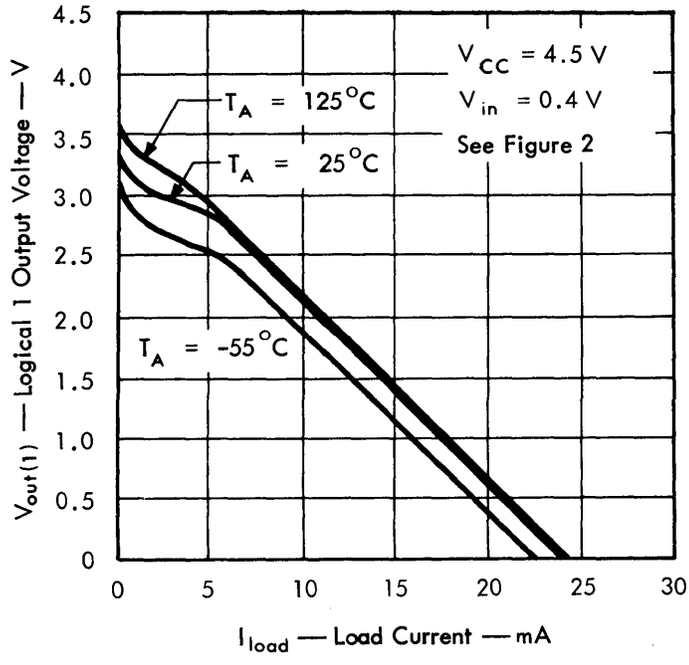


VOLTAGE WAVEFORMS

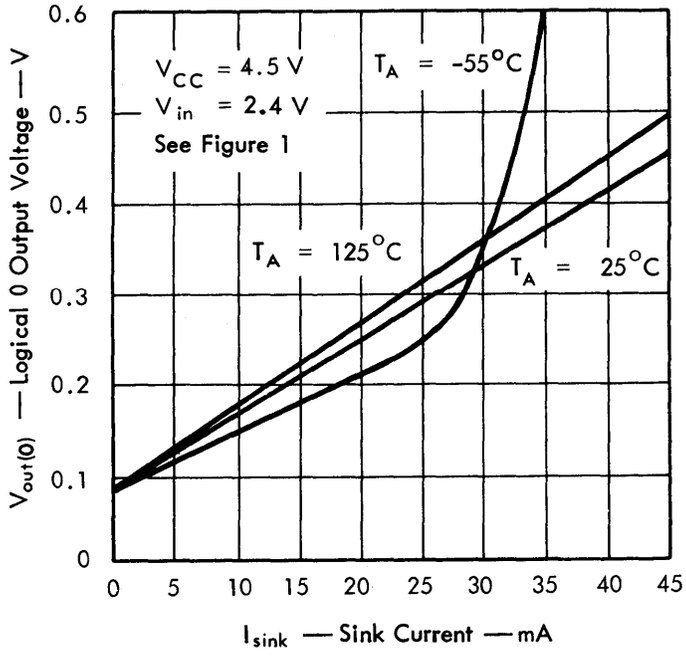
FIGURE 57 — SN5480 SWITCHING TIMES

TYPICAL CHARACTERISTICS §

LOGICAL 1 OUTPUT VOLTAGE vs LOAD CURRENT



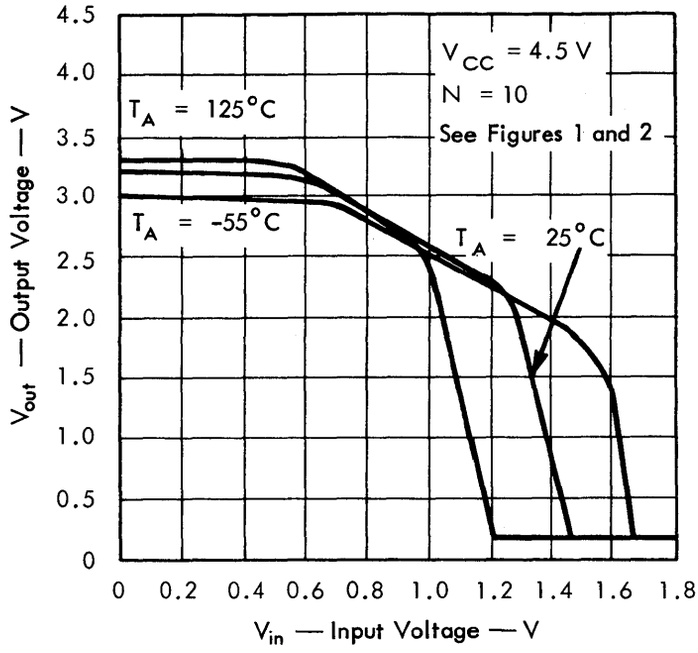
LOGICAL 0 OUTPUT VOLTAGE vs SINK CURRENT



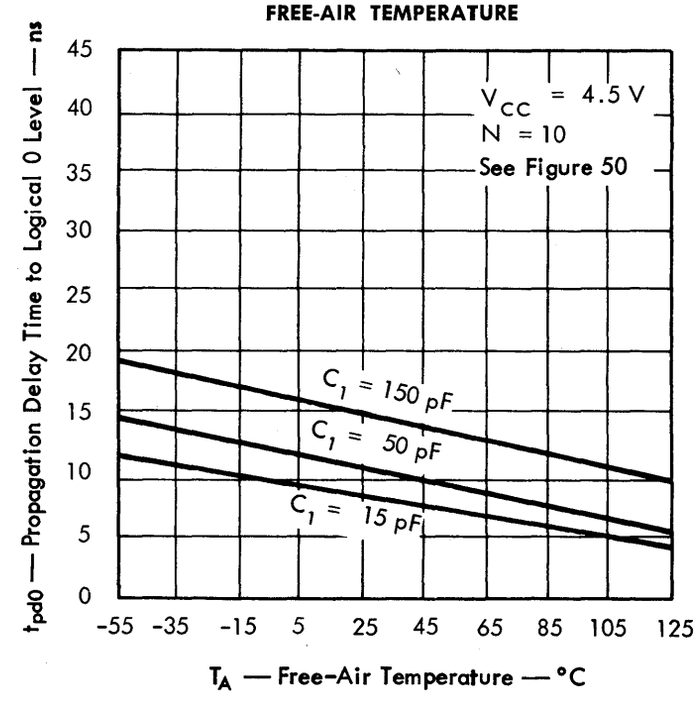
§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.

TYPICAL CHARACTERISTICS §

OUTPUT VOLTAGE vs INPUT VOLTAGE



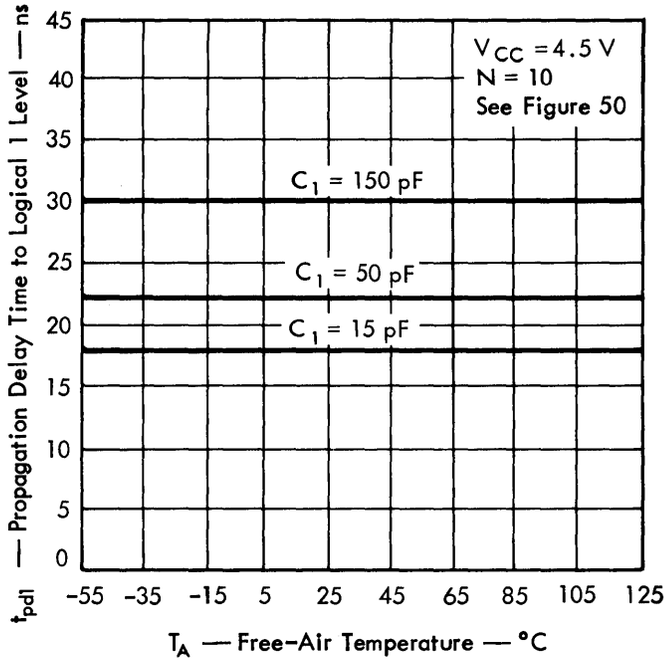
PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL vs FREE-AIR TEMPERATURE



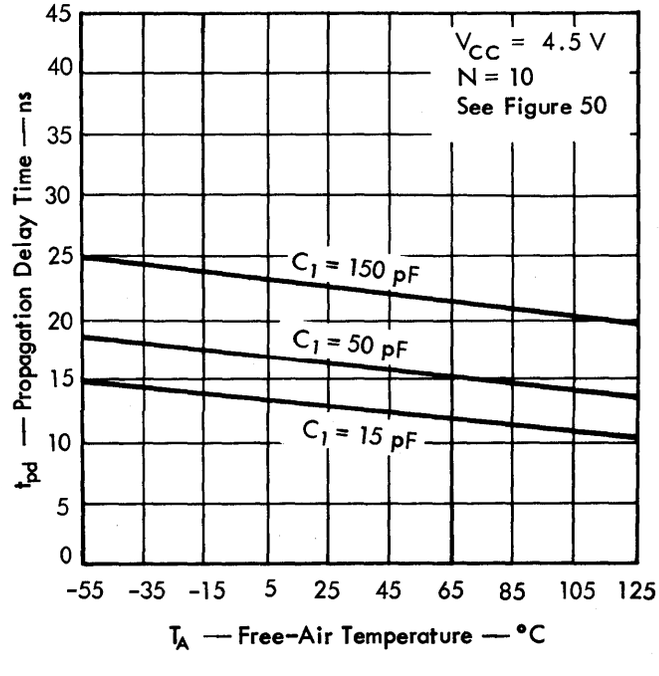
§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.

TYPICAL CHARACTERISTICS §

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



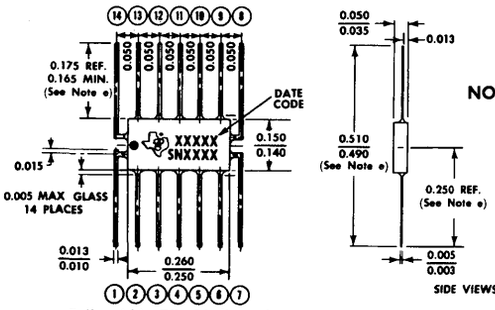
§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.

MECHANICAL DATA

general

Series 54 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 54 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



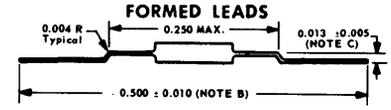
Falls within TO-84 dimensions

NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.

FORMED LEADS



NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

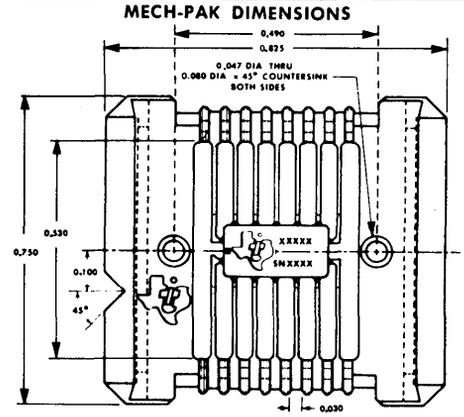
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

How to Insert Pages

1. Place pile of insert pages at right of book.
2. Grasp plastic tabs and pull all three straps out of book.
3. Work from back of book to front, placing insert sheets in numerical order by page number*, aligning their holes with holes in book.
4. After *all* insert sheets are in place, with left hand slip long ends of *all three straps* into right-hand holes.
5. With right hand, slip short ends of straps into left-hand holes. The book is now re-bound.

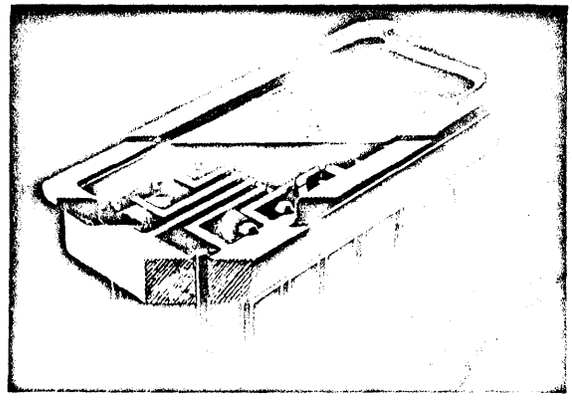
To delete pages, tear them out one at a time as you would tear sheets from a tablet.

***Certain large blocks of page numbers have intentionally been omitted** from the bound book. These numbers are reserved for insert pages.

DIGITAL SEMICONDUCTOR NETWORKS IN A PLUG-IN FLAT PACKAGE

Description

Series 74P consists of Series 74 general-purpose digital circuits mounted in 16-pin hermetically sealed plug-in flat packages.



INDUSTRIAL 16-PIN PLUG-IN FLAT PACKAGE

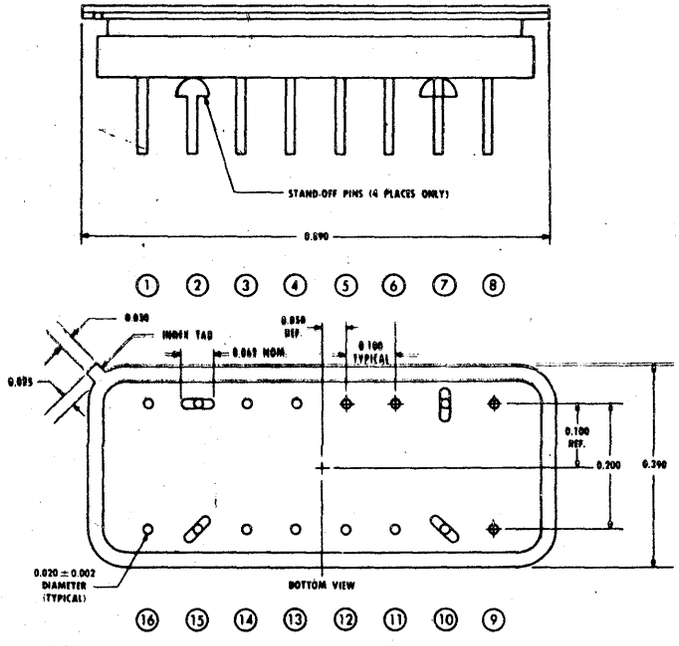
Package features

- **plug-in pin configuration ideal for economical flow-soldering techniques**
- **pins on 100-mil grid spacings for industrial-type circuit-boards**
- **economical package construction**
- **sturdy pins for easy insertion**
- **welded hermetic seal**
- **low profile for space savings**

This inexpensive plug-in package is adaptable to conventional low-cost assembly and design techniques, including high-volume manual or automatic insertion, flow- or wave-soldering, and the use of economical circuit boards designed with 100-mil grid spacings. The package has two rows of firm pins out the bottom with the rows spaced 200 mils apart. A flange tab is provided for indexing, simplifying both manual and automatic insertion. The package has a rugged ceramic-fo-metal construction and a welded-metal hermetic seal, assuring the highest degree of network rigidity and reliability.

Mechanical data

Series 74P networks are mounted in a ceramic-to-metal, hermetically sealed, plug-in package. The circuit and leads are insulated from the package. Leads require no additional cleaning or processing prior to soldering.



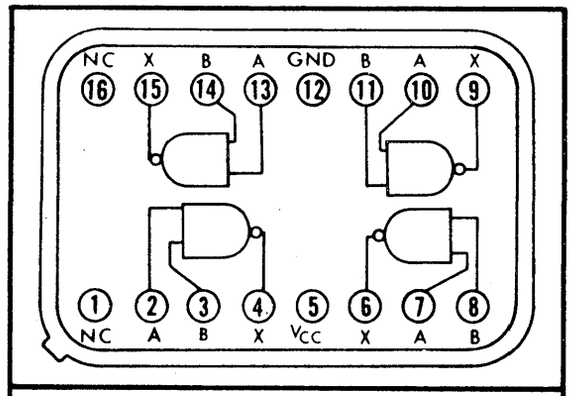
NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK INDUSTRIAL PACKAGE

Specifications, logic symbols, and pin numbers

Schematic diagrams, fan-out rules and specifications for all Series 74P networks are identical to those of the corresponding Series 74 network. Logic symbols for all Series 74P networks are shown here to provide external circuit pin connections. The absence of internal connections to a package is indicated by NC.

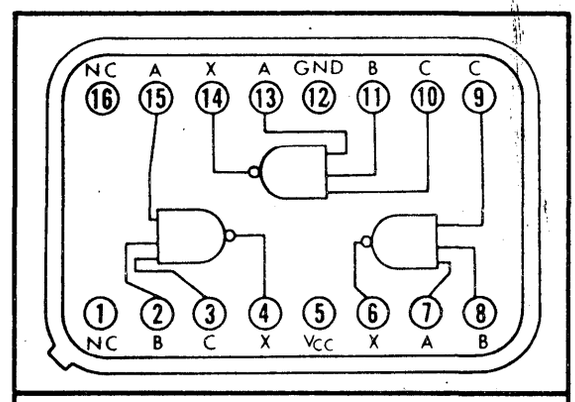
TYPE SN7400P
QUADRUPLE 2-INPUT POSITIVE NAND GATE



positive logic

$X = \overline{AB}$

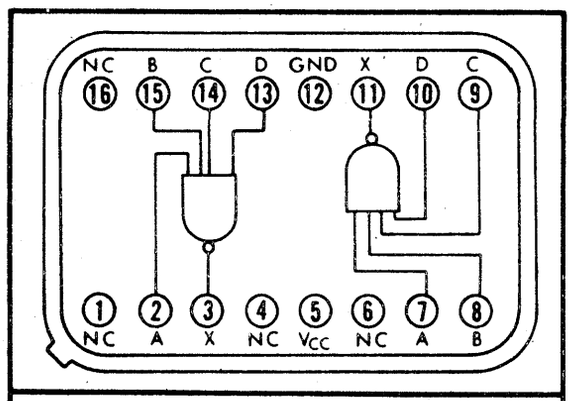
TYPE SN7410P
TRIPLE 3-INPUT POSITIVE NAND GATE



positive logic

$X = \overline{ABC}$

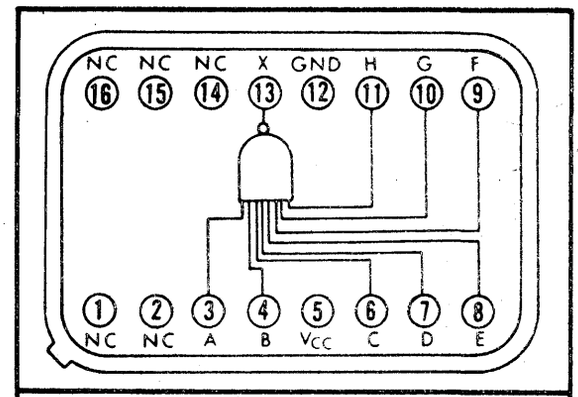
TYPE SN7420P
DUAL 4-INPUT POSITIVE NAND GATE



positive logic

$X = \overline{ABCD}$

TYPE SN7430P
8-INPUT POSITIVE NAND GATE



positive logic

$X = \overline{ABCDEFGH}$

Manufacturer.

Texas Instruments, Inc., Semiconductor Components Division, P.O. Box 5012, Dallas, Texas.

Continued

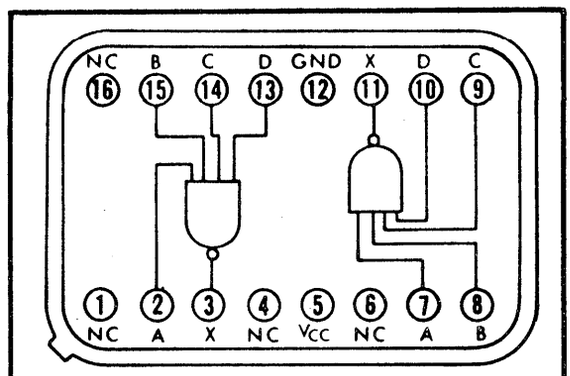
logic definition

Series 74P logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

TYPE SN7440P
DUAL 4-INPUT POSITIVE NAND "POWER" GATE

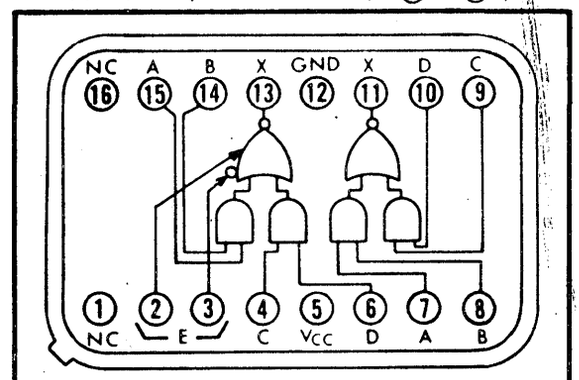


positive logic

$X = \overline{ABCD}$

TYPE SN7450P
EXPANDABLE DUAL EXCLUSIVE-OR GATE

Both expander inputs are used simultaneously for expanding with the SN7460P. If expander is not used leave pins (2) and (3) open.



positive logic

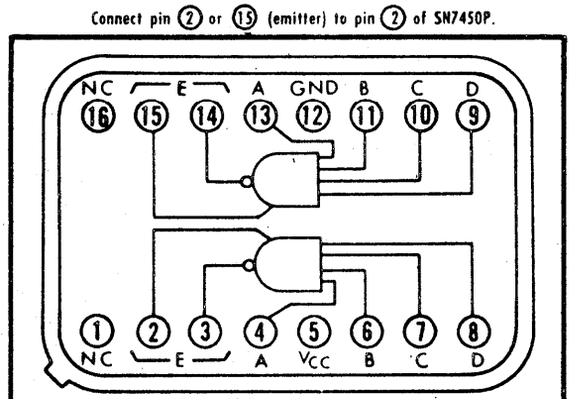
$X = \overline{AB + CD + E}$

E = ABCD from SN7460P

TYPE SN7460P
DUAL 4-INPUT EXPANDER FOR SN7450P

Connect pin (3) or (14) (collector) to pin (3) of SN7450P.

Connect pin (2) or (15) (emitter) to pin (2) of SN7450P.

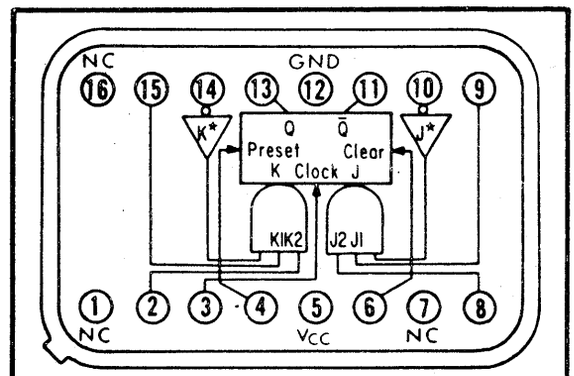


positive logic

$E = \overline{ABCD}$

When connected to pins (2) and (3) of SN7450P.

TYPE SN7470P
J-K FLIP-FLOP



positive logic

Low input to preset sets Q to logical 1

Low input to clear sets Q to logical 0

SERIES 54 930
BULLETIN NO. DL-S 669227, NOVEMBER 1966

HIGH-SPEED TTL DIGITAL SEMICONDUCTOR NETWORKS IN DTL PIN CONFIGURATIONS

description

Series 54 930 consists of Texas Instruments high-speed TTL circuits with pin configurations and logic functions that make them electrically compatible and mechanically interchangeable with Series 15 930 DTL circuits. In addition to five interchangeable networks, an 8-input NAND gate and a dual AND-OR-INVERT gate are available.

comparative features

	SERIES 15 930 DTL	SERIES 54 930 TTL
Gate propagation delay time (typically)	25 ns	13 ns
Fan-out capability (DTL can drive 8 DTL or 5 TTL loads, TTL can drive 10 TTL or 10 DTL loads)	8	10
Noise immunity (guaranteed)	350 mV	400 mV

standard line summary

FUNCTION	TYPES	SIMILAR DTL CIRCUIT
Dual 4-Input Positive NAND Gate	SN54 930	SN15 930
Dual 4-Input Positive NAND Buffer	SN54 932	SN15 932
Quadruple 2-Input Positive NAND Gate	SN54 946	SN15 946
Triple 3-Input Positive NAND Gate	SN54 962	SN15 962
8-Input Positive NAND Gate	SN54 965	None
Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN54 966	None
Master-Slave Flip-Flop	SN54 948	SN15 931/SN15 945/SN15 948

specifications

Schematic diagrams, fan-out rules, maximum ratings, temperature ranges, and electrical characteristics are identical to those of the corresponding Series 54 type number.

SERIES 54 930 TYPE	CORRESPONDING SERIES 54 TYPE
SN54 930	SN5420
SN54 932	SN5440
SN54 946	SN5400
SN54 948	See Note 1
SN54 962	SN5410
SN54 965	SN5430
SN54 966	SN5451

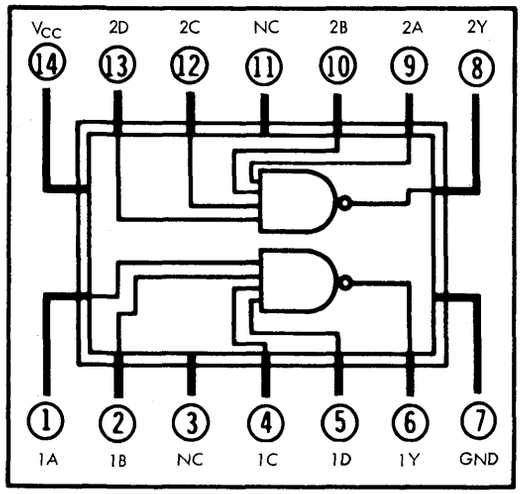
NOTE 1: The SN54 948 has no corresponding Series 54 type. Electrical and switching characteristics are included in this data sheet.

†Patented by Texas Instruments

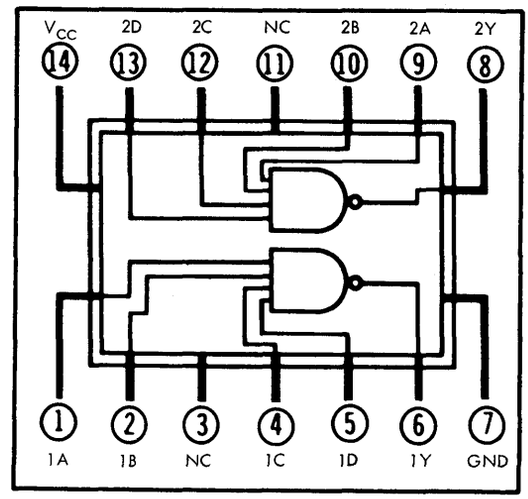
TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PIN CONFIGURATIONS

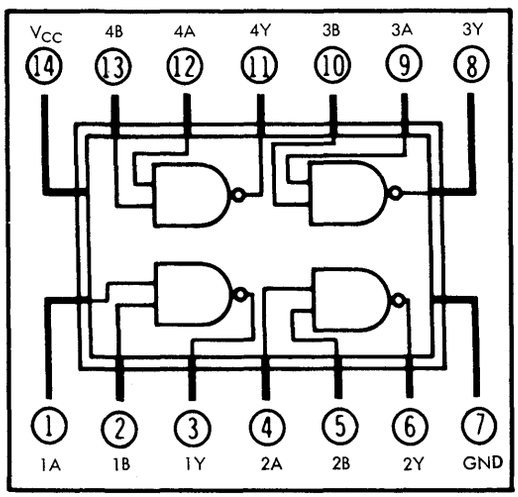
SN54 930
DUAL 4-INPUT POSITIVE NAND GATE



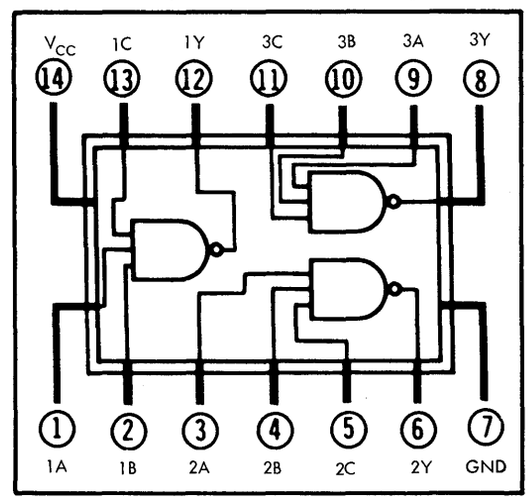
SN54 932
DUAL 4-INPUT POSITIVE NAND BUFFER



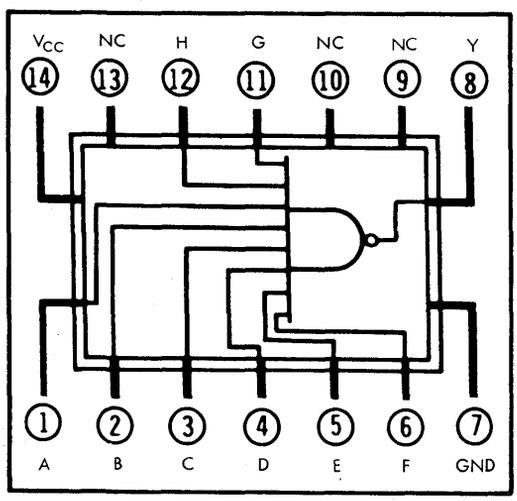
SN54 946
QUADRUPLE 2-INPUT POSITIVE NAND GATE



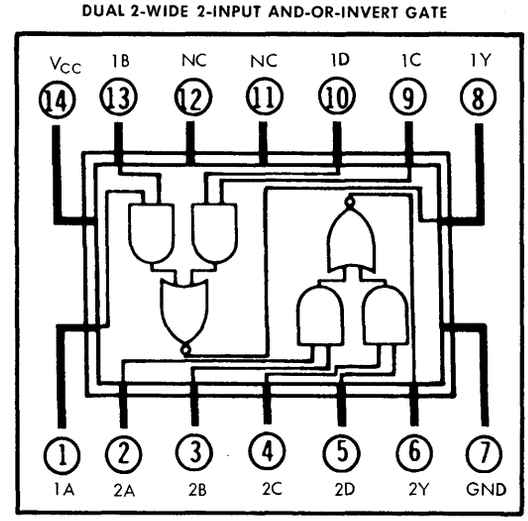
SN54 962
TRIPLE 3-INPUT POSITIVE NAND GATE



SN54 965
8-INPUT POSITIVE NAND GATE



SN54 966
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



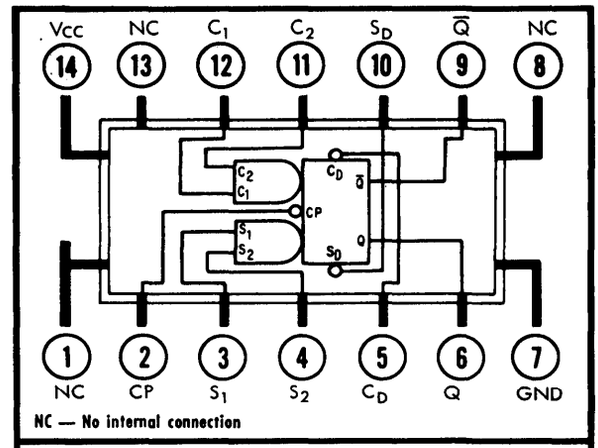
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	*Indeterminate*

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to C_D sets Q to logical 0

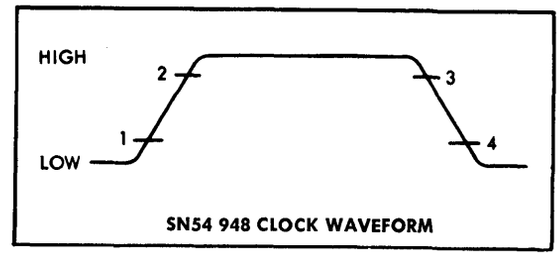
Low input to S_D sets Q to logical 1

C_D and S_D are independent of CP

description

The SN54 948 flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.



SN54 948 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 6) . . . . . $\geq$ 20 ns
Width of Direct Set Pulse, $t_{p(SD)}$ (See Figure 7) . . . . . $\geq$ 25 ns
Width of Direct Clear Pulse, $t_{p(CD)}$ (See Figure 7) . . . . . $\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 6) . . . . . applied clock pulse width
Input Hold Time, t_{hold} . . . . . $\geq$ 0

electrical characteristics, T_A = –55°C to 125°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Logical 0 input voltage	1	V_{CC} = 4.5 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = 4.5 V, I_{load} = –400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = 4.5 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at C_1, C_2, S_1, or S_2	3	V_{CC} = 5.5 V, V_{in} = 0.4 V			–1.6	mA
$I_{in(0)}$	Logical 0 level input current at C_D or S_D	3	V_{CC} = 5.5 V, V_{in} = 0.4 V			–3.2	mA
$I_{in(0)}$	Logical 0 level input current at CP	3	V_{CC} = 5.5 V, V_{in} = 0.4 V			–4.8	mA
$I_{in(1)}$	Logical 1 level input current at C_1, C_2, S_1, or S_2	4	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_D or S_D	4	V_{CC} = 5.5 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at CP	4	V_{CC} = 5.5 V, V_{in} = 2.4 V			120	μA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current †	5	V_{CC} = 5.5 V, V_{in} = 0	–20		–57	mA
I_{CC}	Supply current	4	V_{CC} = 5 V, V_{in} = 5 V		8		mA

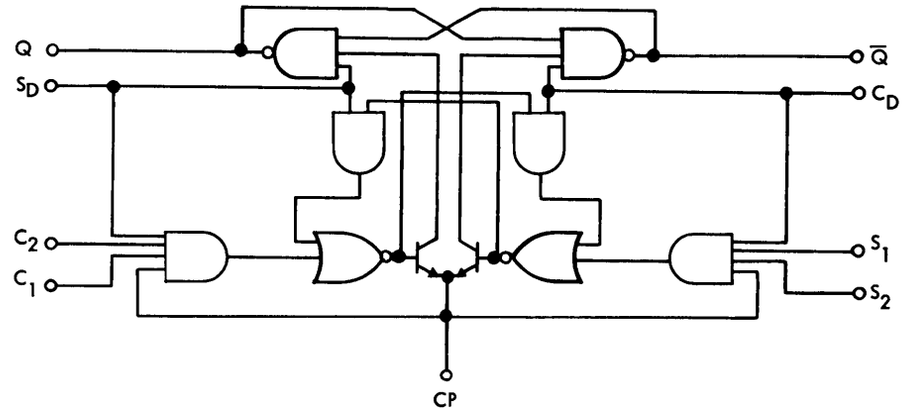
† Not more than one output should be shorted at a time.

‡ These typical values are at V_{CC} = 5 V.

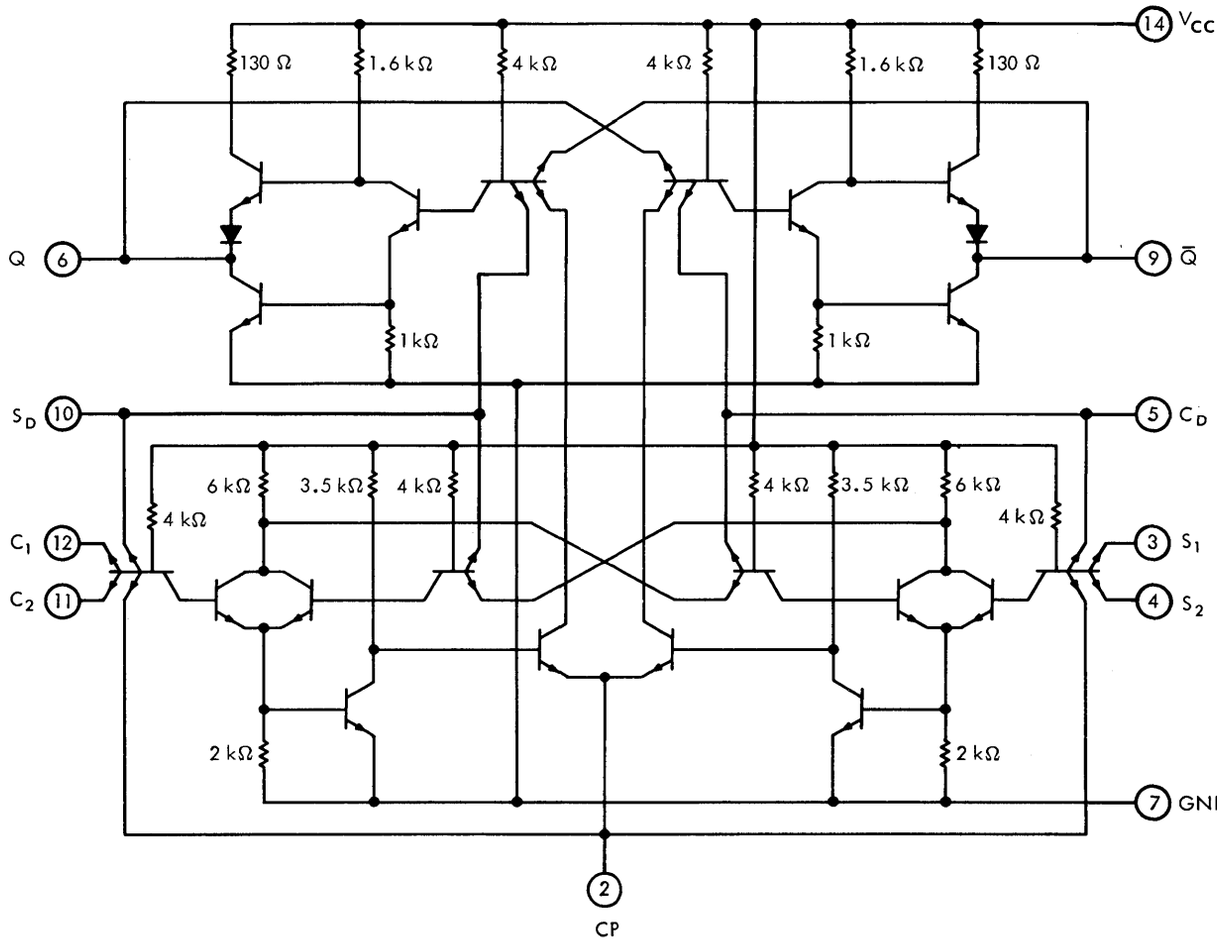
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	6		10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from C_D or S_D to output	7			26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from C_D or S_D to output	7			34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from C_1, C_2, S_1, or S_2 to output	6		10	26	50	ns
t_{pd0}	Propagation delay time to logical 1 level from C_1, C_2, S_1, or S_2 to output	6		10	34	50	ns

functional block diagram

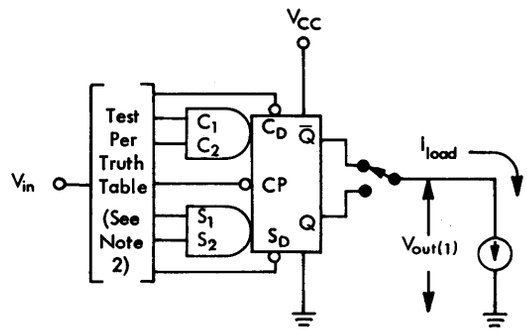


schematic



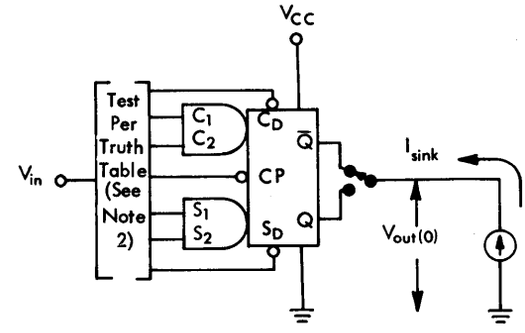
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



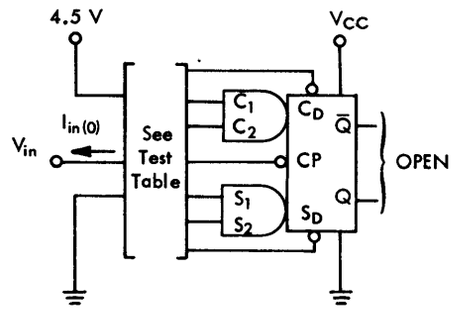
1. Each output is tested separately.
2. Direct inputs C_D and S_D are tested for proper operation.

FIGURE 1



1. Each output is tested separately.
2. Direct inputs C_D and S_D are tested for proper operation.

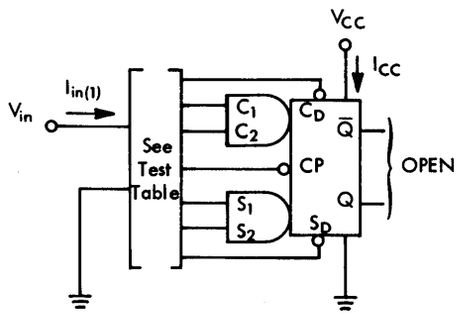
FIGURE 2



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test I_{in})	Apply Momentary GND, Then 4.5 V	Apply 4.5 V
CP	C_D	C_1, C_2, S_1, S_2, and S_D
CP	S_D	C_1, C_2, S_1, S_2, and C_D
C_D	None	S_1, S_2, and CP
S_D	None	C_1, C_2, and CP
C_1	None	C_2, S_D, and CP
C_2	None	C_1, S_D, and CP
S_1	None	S_2, C_D, and CP
S_2	None	S_1, C_D, and CP

FIGURE 3



1. Each input is tested separately.
2. When testing I_{CC}, all inputs and outputs are open.

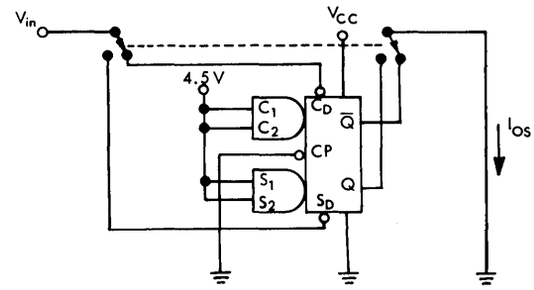
TEST TABLE	
Apply V_{in} (Test I_{in})	Ground
CP	C_D, S_D, C_1, C_2, S_1, and S_2
C_D	CP, S_1, and S_2
S_D	CP, C_1, and C_2
C_1	CP, S_D, and C_2
C_2	CP, S_D, and C_1
S_1	CP, C_D, and S_2
S_2	CP, C_D, and S_1

FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

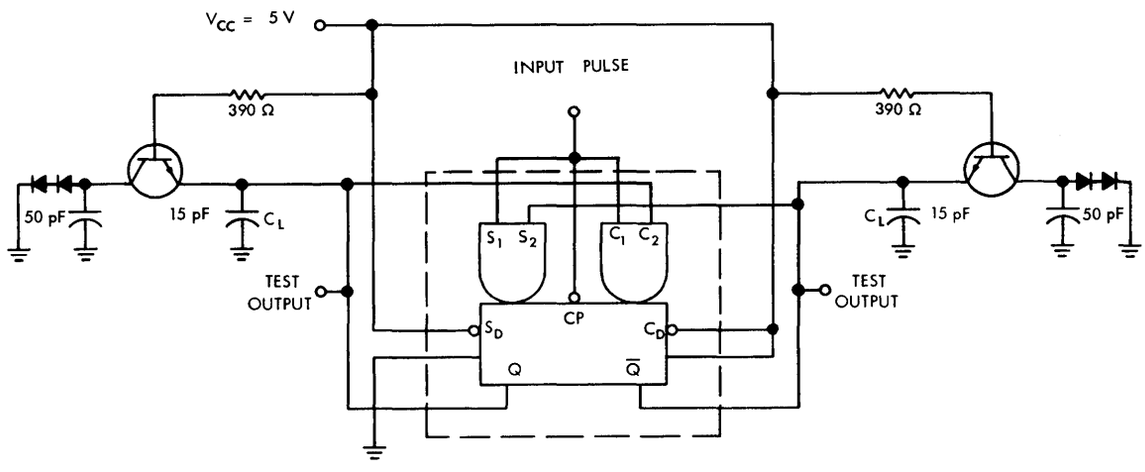


1. Each output is tested separately.

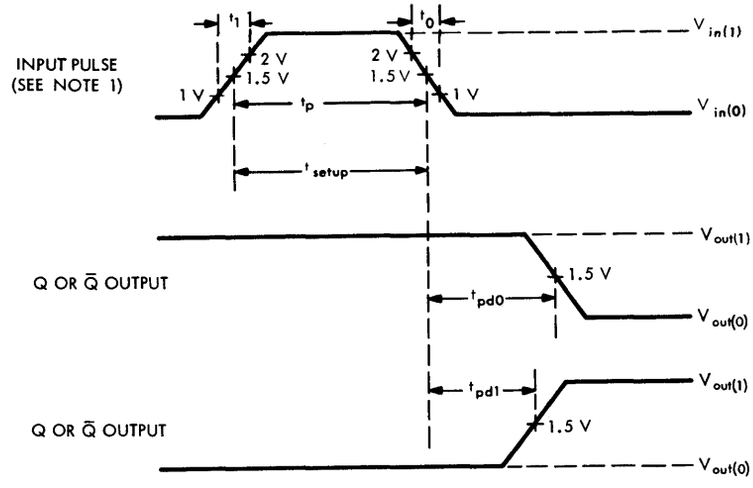
FIGURE 5

†Arrows indicate actual direction of current flow.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 \leq 15$ ns, $t_p = 20$ ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. All transistors are 2N2368.

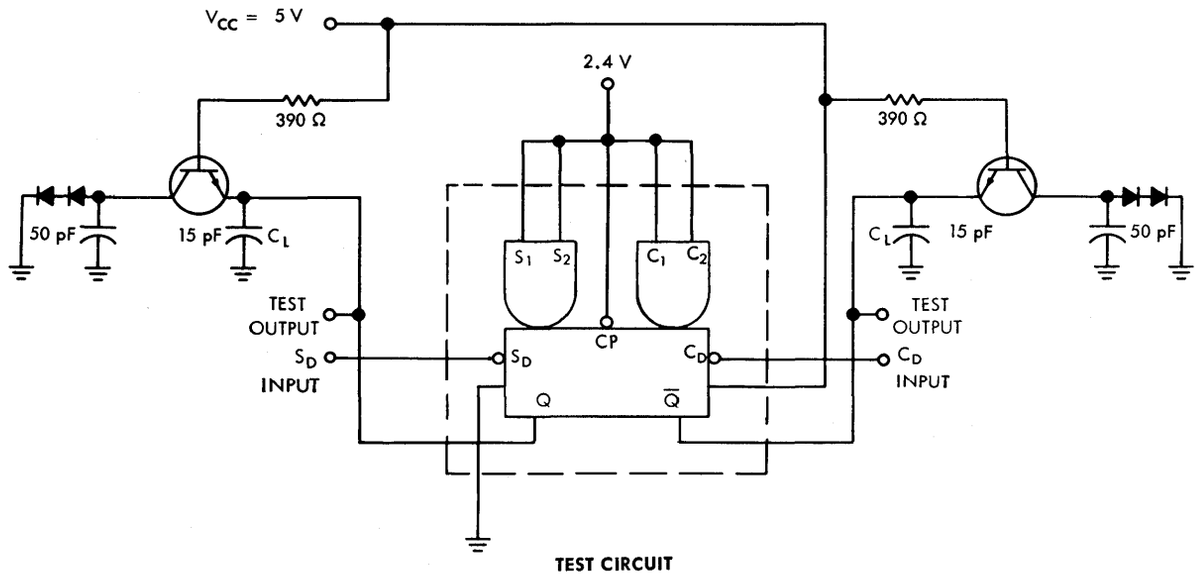
3. All diodes are 1N916.

4. C_L *includes probe and jig capacitance.*

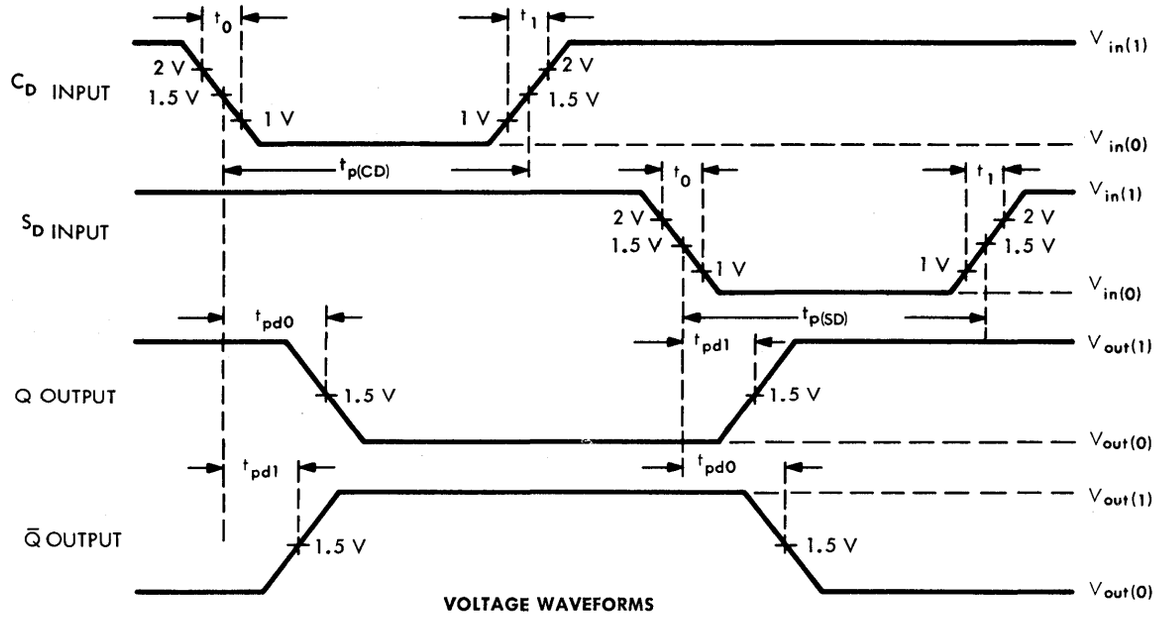
FIGURE 6 — PROPAGATION DELAY TIMES FROM CLOCKED INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. C_D or S_D inputs dominate regardless of the state of clock, C_1, C_2 or S_1, S_2 inputs.

2. C_D or S_D input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 \leq 15$ ns, $t_{p(CD)} = t_{p(SD)} = 25$ ns, and PRR = 1 MHz.

3. All transistors are 2N2368.

4. All diodes are 1N916.

5. C_L includes probe and jig capacitance.

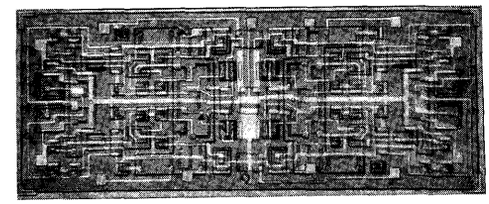
FIGURE 7 — C_D AND S_D PROPAGATION DELAY TIMES

SERIES 53
BULLETIN NO. DL-S 668907, NOVEMBER 1966
REPLACES BULLETINS NOS. 634187 THROUGH 634192, DECEMBER 1963;
NOS. 657751 THROUGH 657758, AUGUST 1965; AND NO. 7446, MARCH 1965

DIGITAL SEMICONDUCTOR NETWORKS FOR GENERAL PURPOSE SYSTEM APPLICATIONS

application

Series 53 semiconductor networks are ideally suited for general-purpose digital applications, including computer, data handling, and control systems. Series 53 is designed and characterized for use over the full military temperature range of –55°C to 125°C.



DUAL J-K FLIP-FLOP BAR

features

LOW SYSTEM COST

- **multifunction devices offering lowest cost per logic function**

ADVANCED PERFORMANCE

- **attractive speed/power ratio**
- **high a-c noise rejection from low output impedance**
- **waveshape integrity maintained over rated temperature and loading conditions by double-ended output stage**

EASE OF DESIGN

- **complete family available — 15 networks**
- **modified DTL circuitry simplifies system design**
- **fan-out of 10 from each double-ended output**

description

Series 53 is a compatible line of digital semiconductor networks capable of performing all basic and some special logic functions. All basic logic functions are offered as multifunction networks. Utilization of this complete line of compatible networks reduces systems engineering design time, while the use of multifunction networks reduces system cost per logic function.

Series 53 logic employs a modified form of diode-transistor logic (DTL) where transistors replace conventional diodes in order to improve circuit performance. Input transistors reduce drive requirements while offset transistors improve switching speed. The Series 53 low-impedance output stage maintains symmetrical waveshapes over wide ranges of d-c fan-out, capacitive loads, and operating temperatures. The low-impedance output also provides a high degree of protection against capacitively coupled noise transients on system information lines.

CONTENTS

†Patented by Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical operating characteristics, T_A = –55°C to 125°C, supply voltage V_{CC} = 3 V to 4 V

Speed: Gate Propagation Delay	35 ns
Flip-flop Toggle Rate	4 MHz
Fan-Out Capability (Double-ended Outputs)	10
Fan-In With Expanders	25 max
Output Impedance	< 50 Ω
Average Power Dissipation: Per Gate	12 mW
Per Flip-flop	40 mW

design characteristics

Series 53 is a compatible line of digital semiconductor integrated circuits built and characterized for medium-speed applications (up to 4 MHz) over the full military temperature range. The networks are fabricated from triple-diffused planar silicon, and employ a modified form of diode-transistor logic selected to take advantage of inherent integrated-circuit characteristics.

As in conventional diode logic (Figure A), logic is performed at node A of a Series 53 gate (Figure B).

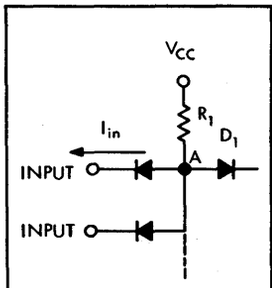


FIGURE A. Diode AND Logic

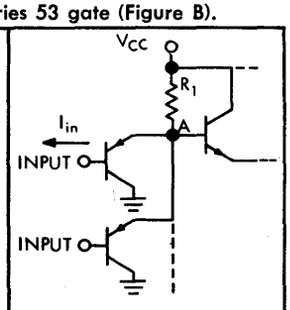


FIGURE B. Series 53 AND Logic

The gain of the p-n-p transistors replacing the input diodes increases the effective drive capability of the preceding stage. The voltage at node A is now a function of I_{in}, R_1, and the p-n-p transistor gain, rather than only I_{in} and R_1 as in diode logic. The effect of the transistor gain is to minimize the importance of the resistor value in the circuit's performance. Since silicon resistors have inherently wide production tolerances and high temperature coefficients, the transistor gain makes fabrication of Series 53 networks more economical while assuring greater stability over the full military temperature range.

The n-p-n transistor which replaces the offset diode D_1 also has gain, increasing the circuit drive capability and improving the waveshapes at node A.

This basic AND logic configuration is coupled with an inverting double-ended output stage (Figure C) in each Series 53 NAND/NOR gate and each flip-flop.

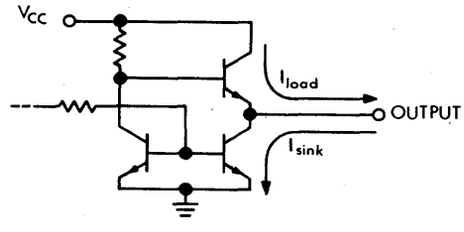


FIGURE C. Series 53 Double-Ended Output Stage

The most important feature of the Series 53 NAND/NOR gate or flip-flop output stage is its ability to supply load and sink current with low output impedance. This provides high d-c fan-out to both types of loads and simplifies interface design. Low output impedance in either state ensures that turn-on and turn-off waveshapes will remain sharp and symmetrical over a wide range of d-c and capacitive loadings throughout the temperature range. The low output impedance of these outputs ensure that every information line will have a low-impedance termination, providing valuable protection against a-c coupled noise transients.

All Series 53 networks are fabricated using a 4-step planar diffusion process. First, an n-type diffusion is made in the p-type substrate, forming the n-p-n collectors only. A second n-type diffusion is made forming the base area of the p-n-p transistors, isolation region of the resistors, one section of the capacitors, and further forming the n-p-n collectors. This sequence reduces the n-p-n transistor $r_{CE(sat)}$ to approximately 30 ohms, while keeping the p-n-p base width narrow and the gain high (typically 12). The next step is a p-type diffusion which forms the p-n-p emitters, n-p-n bases, resistors, and another portion of the capacitors. The final diffusion is an n-type, forming the n-p-n emitters and completing the capacitors.

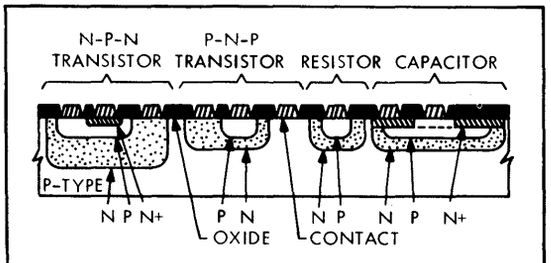


FIGURE D. Series 53 Triple-Diffused Structure

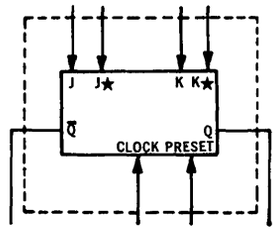
Two AND/OR gates, the SN5320 and SN5340, provide additional flexibility for the logic designer. These gates may be used in applications where noninverted signals and/or reduced propagation delay times are necessary and high fan-out is not a requirement. Characteristics of the AND/OR gates limit the number which may be cascaded (connected in series) between any Series 53 circuit and Series 53 flip-flops or inverter/drivers.

SERIES 53 AND/OR GATE CASCADING CAPABILITY

Minimum V_{CC}	3.2 V	3.6 V	4.0 V
Maximum number of AND/OR gates which may be cascaded	1	2	3

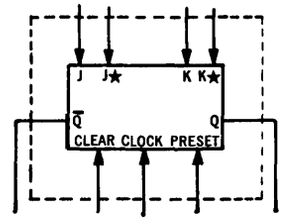
standard line summary

SN5300 See Page 2005



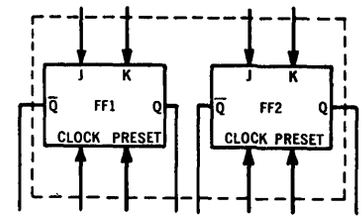
J-K FLIP-FLOP WITH PRESET

SN5301 See Page 2007



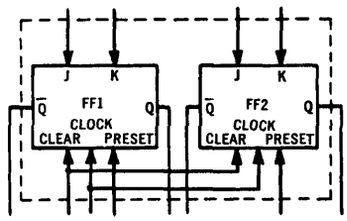
J-K FLIP-FLOP WITH PRESET AND CLEAR

SN5302 See Page 2009



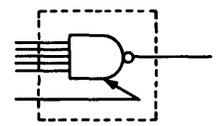
DUAL J-K FLIP-FLOP WITH PRESET

SN5304 See Page 2011



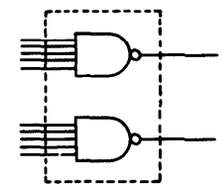
DUAL J-K
FLIP-FLOP WITH PRESET AND CLEAR

SN5310 See Page 2013



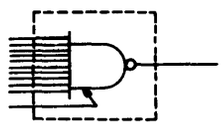
5-INPUT EXPANDABLE NAND/NOR GATE

SN5311 See Page 2015



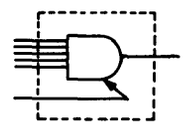
DUAL 5-INPUT NAND/NOR GATE

SN5315 See Page 2016



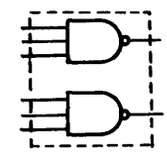
10-INPUT EXPANDABLE NAND/NOR GATE

SN5320 See Page 2018



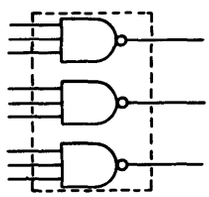
5-INPUT EXPANDABLE AND/OR GATE
(ALSO USABLE AS 5-INPUT EXPANDER)

SN5330 See Page 2020



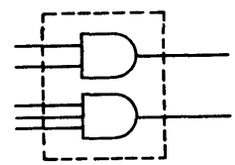
DUAL 3-INPUT NAND/NOR GATE

SN5331 See Page 2021



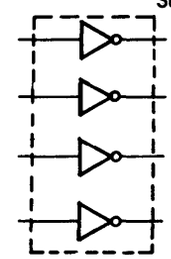
TRIPLE 3-INPUT NAND/NOR GATE

SN5340 See Page 2022



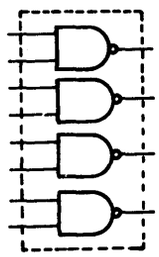
DUAL AND/OR GATE

SN5350 See Page 2024



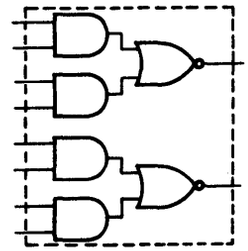
QUADRUPLE INVERTER/DRIVER

SN5360 See Page 2025



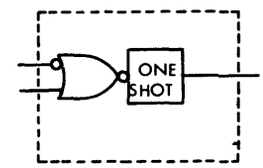
QUADRUPLE 2-INPUT NAND/NOR GATE

SN5370 See Page 2026



DUAL EXCLUSIVE-OR GATE

SN5380 See Page 2027



ONE-SHOT
MONOSTABLE MULTIVIBRATOR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . +7 V
Supply Voltage V_{EE} With Respect to V_{CC} (SN5320 and SN5340) . . . . . –7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . V_{CC}
Operating Free-Air Temperature Range . . . . . –55°C to 125°C
Storage Temperature Range . . . . . –65°C to 150°C

NOTES: 1. Voltage values (with the exception of the V_{EE} rating above) are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 53 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input current requirements

Weighted values of input current requirements reflect worst-case conditions for $T_A = -55°C$ to 125°C and $V_{CC} = 3$ V to 4 V. One positive load (N + = 1) requires current into the input at a logical 1 voltage level (0.5 mA at $V_{CC} = 3$ V or $V_{CC} = 4$ V). One negative load (N– = 1) requires current out of the input at a logical 0 voltage level (0.25 mA at $T_A = -55°C$, or 0.19 mA at $T_A = 125°C$). Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS

NETWORK	TYPE	INPUT	N+ LOADS	N– LOADS
FLIP-FLOPS	5300, 5301 5302	J, J★, K, K★, Preset, Clear	1	0
		Clock	2.5	2.5
	5304	J, K, Preset	1	0
		Clear	2	0
		Clock	5	5
GATES AND EXPANDER	5310, 5311, 5315, 5320, 5330, 5331, 5340, 5360, 5370	Each Input	0	1
ONE-SHOT	5380	T, T★	1	0
INVERTER	5350	Each Input	2	0

output drive capability

Weighted values of fan-out reflect the ability of an output to drive current to N+ loads and sink current from N– loads under worst-case conditions. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

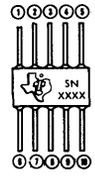
WEIGHTED VALUES OF FAN-OUT

NETWORK	OUTPUT	N+ LOADS	N– LOADS
FLIP-FLOPS, NAND/NOR GATES, AND ONE-SHOT	Each Output	10	10
INVERTER (SN5350)	Each Output	10	10
	4 Inverters in parallel	40	40
AND/OR GATES SN5320 and SN5340	Each Output	4	4

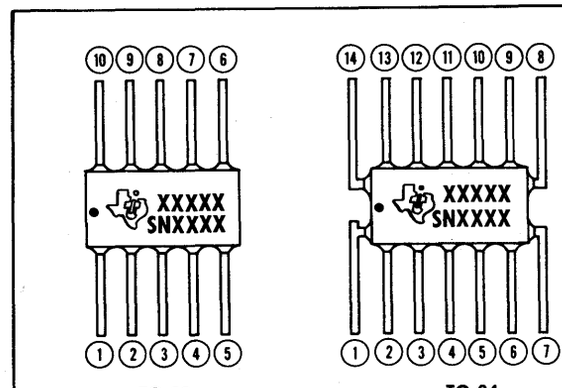
pin identification

Pin identification for Series 53 networks is shown in the illustration at the right. Symbolization on package denotes orientation. For dimensions see mechanical data.

CAUTION:
Pin numbers of the 10-pin package have been renumbered in accordance with TO-89. The electrical functions are in the same physical location as shown on all previous data. Former pin numbers of 10-pin package are shown for reference.



FORMER PIN NOS.



TO-89 TO-84

logic

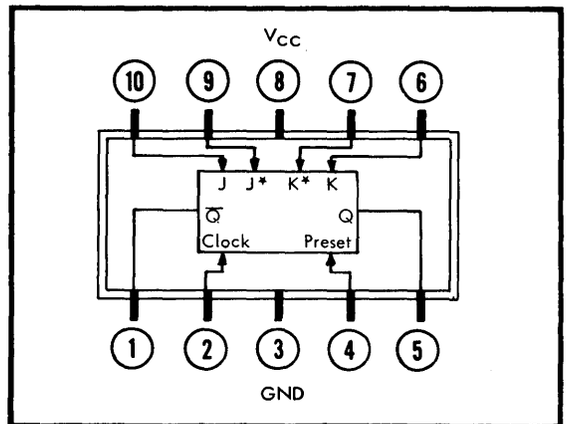
TRUTH TABLES

J★ = K★ = 1		
t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

J = K = 0		
t_n		t_{n+1}
J★	K★	Q
0	0	$\overline{Q}$n
0	1	1
1	0	0
1	1	Qn

ADDITIONAL INPUT LOGIC COMBINATIONS				
t_n				t_{n+1}
J	K	J★	K★	Q
0	1	0	0	$\overline{Q}$n
1	0	0	0	$\overline{Q}$n
1	1	0	0	$\overline{Q}$n
0	1	0	1	$\overline{Q}$n
1	1	0	1	$\overline{Q}$n
1	0	1	0	$\overline{Q}$n
1	1	1	0	$\overline{Q}$n
1	0	0	1	1
0	1	1	0	0

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse



positive logic

High input to preset sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+	10
Maximum Fan-out From Each Output Into Negative Loads, N–	10
Fall Time of Clock Pulse $t_{f(clock)}$	20 to 150 ns
Minimum Width of Clock Pulse $t_{p(clock)}$	50 ns
Rise Time of Clock Pulse $t_{r(clock)}$	10 to 500 ns

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, J★, K★, preset, and clock	1, 2	V_{CC} = 3 V	1.5		3	V
			V_{CC} = 4 V	1.5		4	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, J★, K★, preset, and clock	1, 2		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	3	N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	J, K, J★, K★, or preset input current	3	V_{in} = 2.7 V	0		0.5	mA
I_{in}	Clock input current	3	V_{in} = 2 V	0		1.25	mA
			V_{in} = 0.3 V, T_A = –55°C			–0.625	mA
			V_{in} = 0.3 V, T_A = 125°C			–0.475	mA
$I_{CC(av)}$	Average supply current	4	V_{CC} = 3 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		9		mA
			V_{CC} = 4 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		13		mA

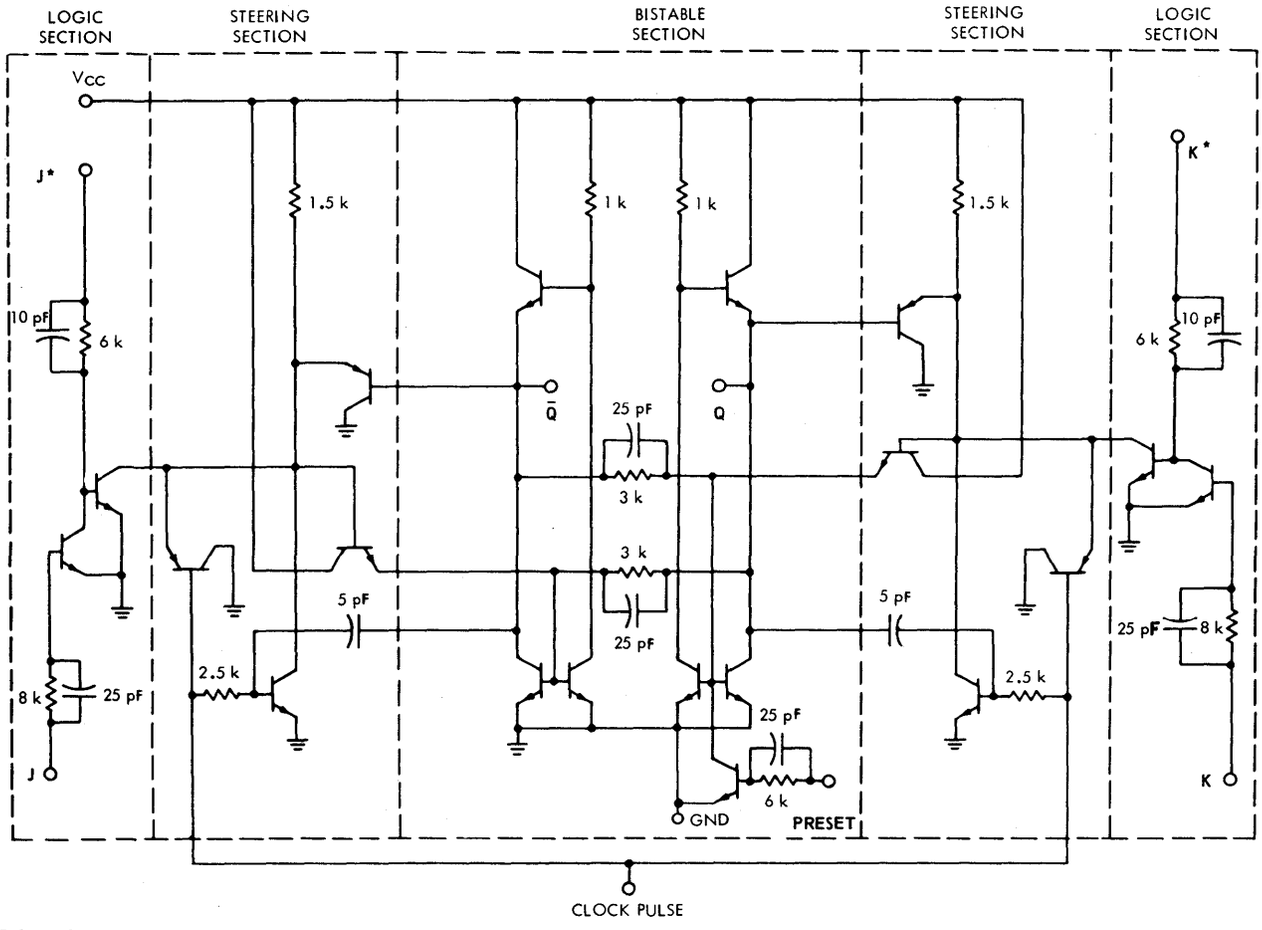
CAUTION:

This device was formerly TYPE SN530. Pin numbers of the SN5300 have been renumbered in accordance with TO-89. The electrical functions of the SN530 and the SN5300 are in the same physical location. See **pin identification,** *page 2004, for SN530 pin numbers.*

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ V, N + = N– = 0

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, f = 1 MHz *J, J★, K and K★ Input:* $V_{in} = V_{CC}$ *Preset Input:* $V_{in} = 0$	20	30	ns
t_r	Rise Time			20	45	ns
t_s	Storage Time			40	60	ns
t_f	Fall Time			25	40	ns
$t_{set(1)}$	Time to Set a Logical 1: J or K	23	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, f = 1 MHz *J, J★, K or K★ Input:* $V_{in(1)} = 2.5$ V, $V_{in(0)} = 0$, $t_r = t_f = 50$ ns	50		ns
	J★ or K★			35		ns
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		ns
	J★ or K★			40		ns
t_{preset}	Preset Time	24	*Clock Input:* $V_{in} = 0$ *Preset Input:* $V_{in} = 2.5$ V, $t_f = 50$ ns	55		ns

schematic



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

logic

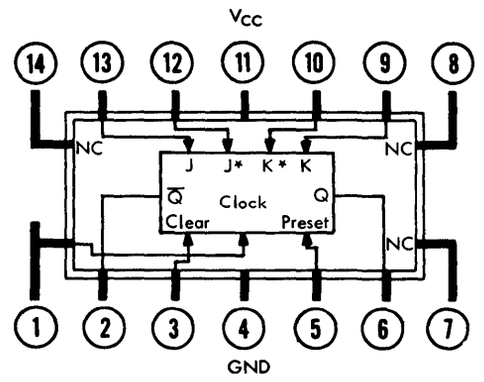
TRUTH TABLES

J★=K★=1		
t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

J=K=0		
t_n		t_{n+1}
J★	K★	Q
0	0	$\overline{Q}$n
0	1	1
1	0	0
1	1	Qn

ADDITIONAL INPUT LOGIC COMBINATIONS				
t_n				t_{n+1}
J	K	J★	K★	Q
0	1	0	0	$\overline{Q}$n
1	0	0	0	$\overline{Q}$n
1	1	0	0	$\overline{Q}$n
0	1	0	1	$\overline{Q}$n
1	1	0	1	$\overline{Q}$n
1	0	1	0	$\overline{Q}$n
1	1	1	0	$\overline{Q}$n
1	0	0	1	1
0	1	1	0	0

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse



NC — No internal connection.

positive logic

High input to preset sets Q to logical 1
High input to clear sets Q to logical 0

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10
Fall Time of Clock Pulse $t_{f(clock)}$ . . . . . 20 to 150 ns
Minimum Width of Clock Pulse $t_{p(clock)}$ . . . . . 50 ns
Rise Time of Clock Pulse $t_{r(clock)}$ . . . . . 10 to 500 ns

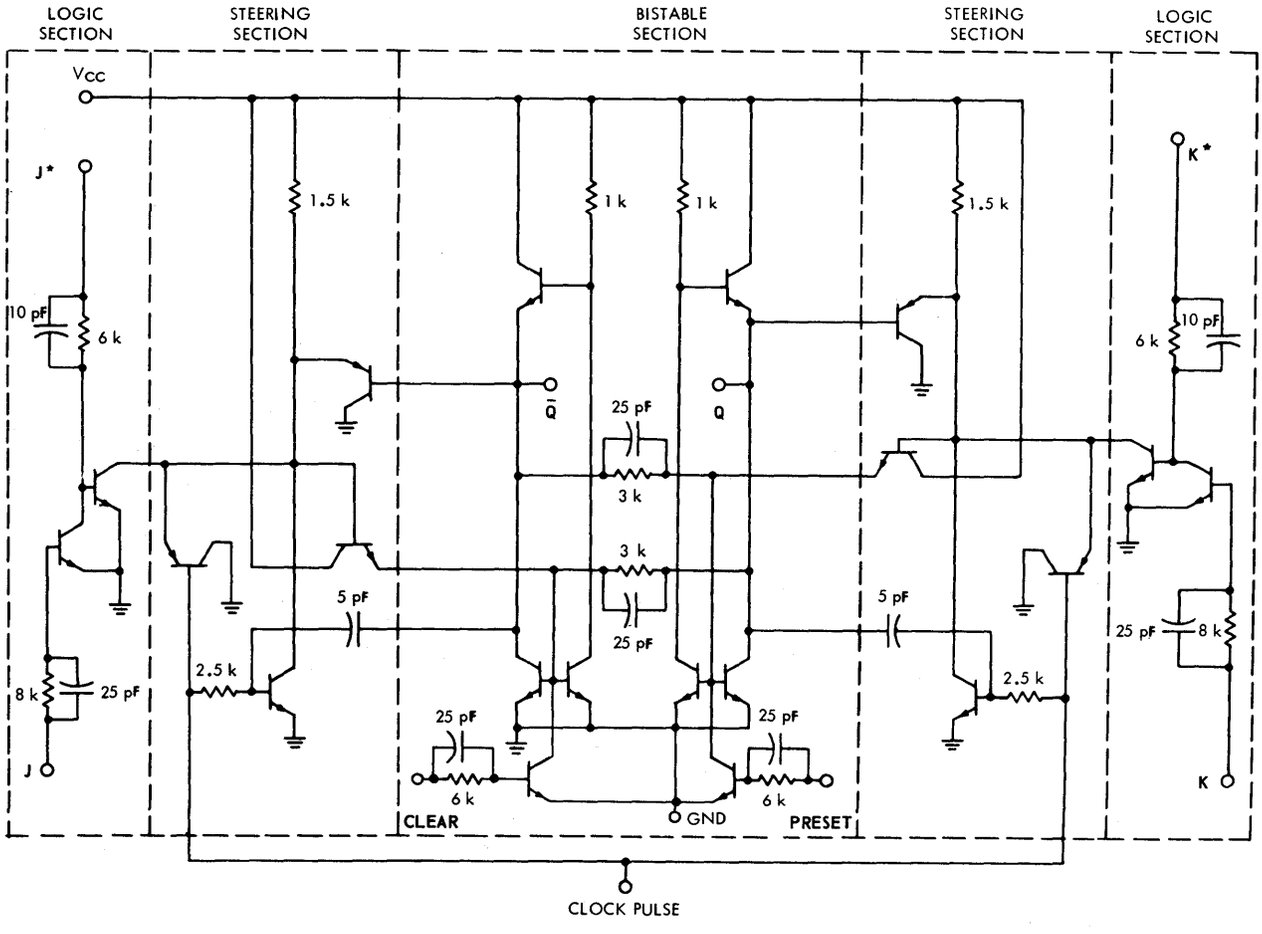
electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, J★, K★, preset, clock and clear	1, 2	V_{CC} = 3 V	1.5		3	V
			V_{CC} = 4 V	1.5		4	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, J★, K★, preset, clock and clear	1, 2		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	3	N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	J, K, J★, K★, preset, or clear input current	3	V_{in} = 2.7 V	0		0.5	mA
I_{in}	Clock input current	3	V_{in} = 2 V	0		1.25	mA
			V_{in} = 0.3 V, T_A = –55°C			–0.625	mA
			V_{in} = 0.3 V, T_A = 125°C			–0.475	mA
$I_{CC(av)}$	Average supply current	4	V_{CC} = 3 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		9		mA
			V_{CC} = 4 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		13		mA

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ V, N + = N– = 0

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns,	20	30	ns
t_r	Rise Time		$t_p = 500$ ns, f = 1 MHz	20	45	ns
t_s	Storage Time		*J, J★, K and K★ Input:* $V_{in} = V_{CC}$	40	60	ns
t_f	Fall Time		*Preset Input:* $V_{in} = 0$	25	40	ns
			Clear Input: $V_{in} = 0$			
$t_{set(1)}$	Time to Set a Logical 1:	23	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns,			
	J or K		$t_p = 500$ ns, f = 1 MHz	50		ns
	J★ or K★		*J, J★, K and K★ Input:* $V_{in(1)} = 2.5$ V,	35		ns
$t_{set(0)}$	Time to Set a Logical 0:		$V_{in(0)} = 0$, $t_r = t_f = 50$ ns			
	J or K			40		ns
	J★ or K★			40		ns
t_{preset}	Preset Time	24	*Clock Input:* $V_{in} = 0$	55		ns
			Preset Input: $V_{in} = 2.5$ V, $t_f = 50$ ns			
t_{clear}	Clear Time	24	*Clock Input:* $V_{in} = 0$	75		ns
			Clear Input: $V_{in} = 2.5$ V, $t_f = 50$ ns			

schematic



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

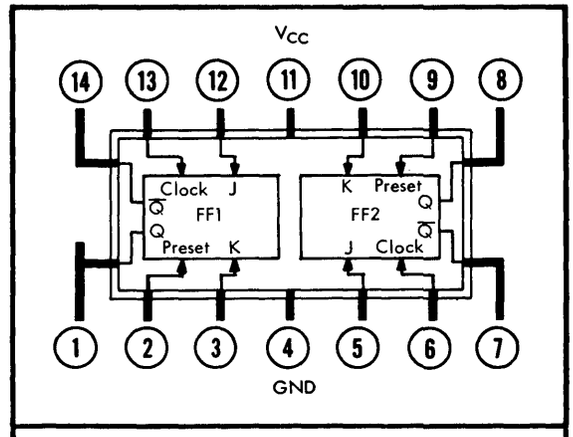
logic

TRUTH TABLE
EACH FLIP-FLOP

t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}n$

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse



positive logic

High input to preset sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10
Fall Time of Clock Pulse $t_{f(clock)}$ . . . . . 20 to 150 ns
Minimum Width of Clock Pulse $t_{p(clock)}$ . . . . . 50 ns
Rise Time of Clock Pulse $t_{r(clock)}$ . . . . . 10 to 500 ns

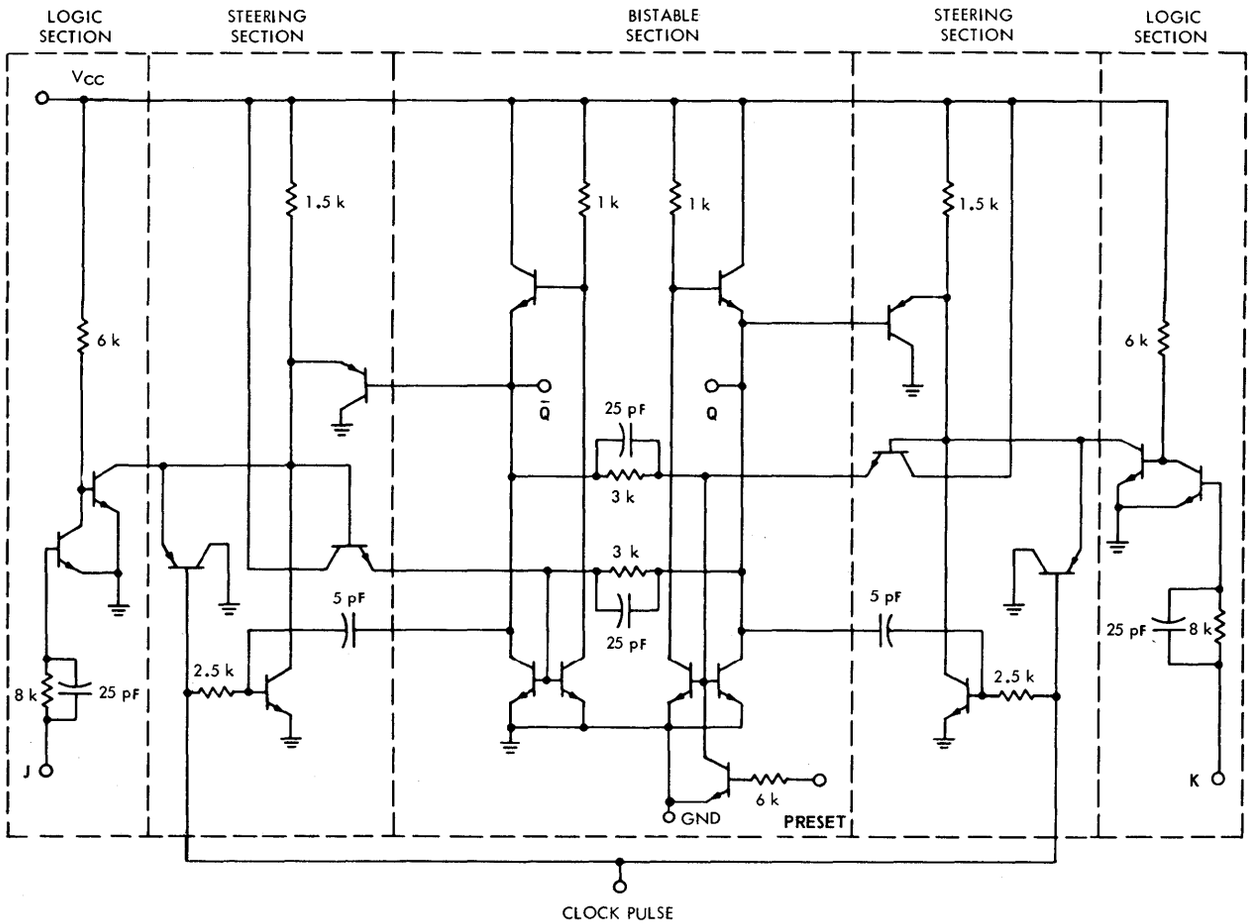
electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, preset, and clock	1, 2	V_{CC} = 3 V	1.5		3	V
			V_{CC} = 4 V	1.5		4	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, preset, and clock	1, 2		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	3	N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	J, K, or preset input current	3	V_{in} = 2.7 V	0		0.5	mA
I_{in}	Clock input current	3	V_{in} = 2 V	0		1.25	mA
			V_{in} = 0.3 V, T_A = –55°C			–0.625	mA
			V_{in} = 0.3 V, T_A = 125°C			–0.475	mA
$I_{CC(av)}$	Average supply current (each flip-flop)	4	V_{CC} = 3 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		9		mA
			V_{CC} = 4 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		13		mA

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ V, N + = N– = 0

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, $f = 1$ MHz *J and K Input:* $V_{in} = V_{CC}$ *Preset Input:* $V_{in} = 0$	20	30	ns
t_r	Rise Time			20	45	ns
t_s	Storage Time			40	60	ns
t_f	Fall Time			25	40	ns
$t_{set(1)}$	Time to Set a Logical 1: J or K	23	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, $f = 1$ MHz *J and K Input:* $V_{in(1)} = 2.5$ V, $V_{in(0)} = 0$, $t_r = t_f = 50$ ns	50		ns
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		ns
t_{preset}	Preset Time	24	*Clock Input:* $V_{in} = 0$ *Preset Input:* $V_{in} = 2.5$ V, $t_f = 50$ ns	75		ns

schematic (each flip-flop)



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

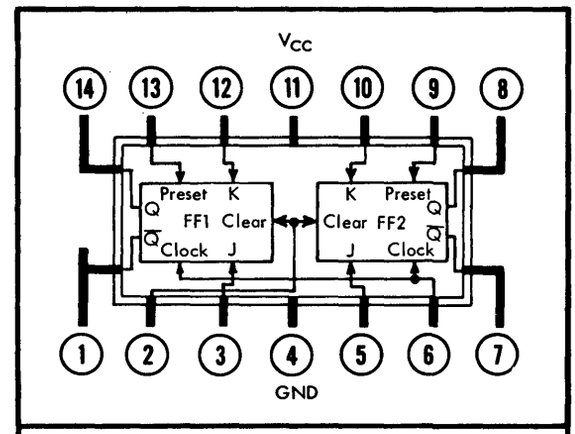
logic

TRUTH TABLE
EACH FLIP-FLOP

t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse



positive logic

High input to preset sets Q to logical 1

High input to clear sets Q1 and Q2 to logical 0

recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+	10
Maximum Fan-out From Each Output Into Negative Loads, N–	10
Fall Time of Clock Pulse $t_{f(clock)}$	20 to 150 ns
Minimum Width of Clock Pulse $t_{p(clock)}$	50 ns
Rise Time of Clock Pulse $t_{r(clock)}$	10 to 500 ns

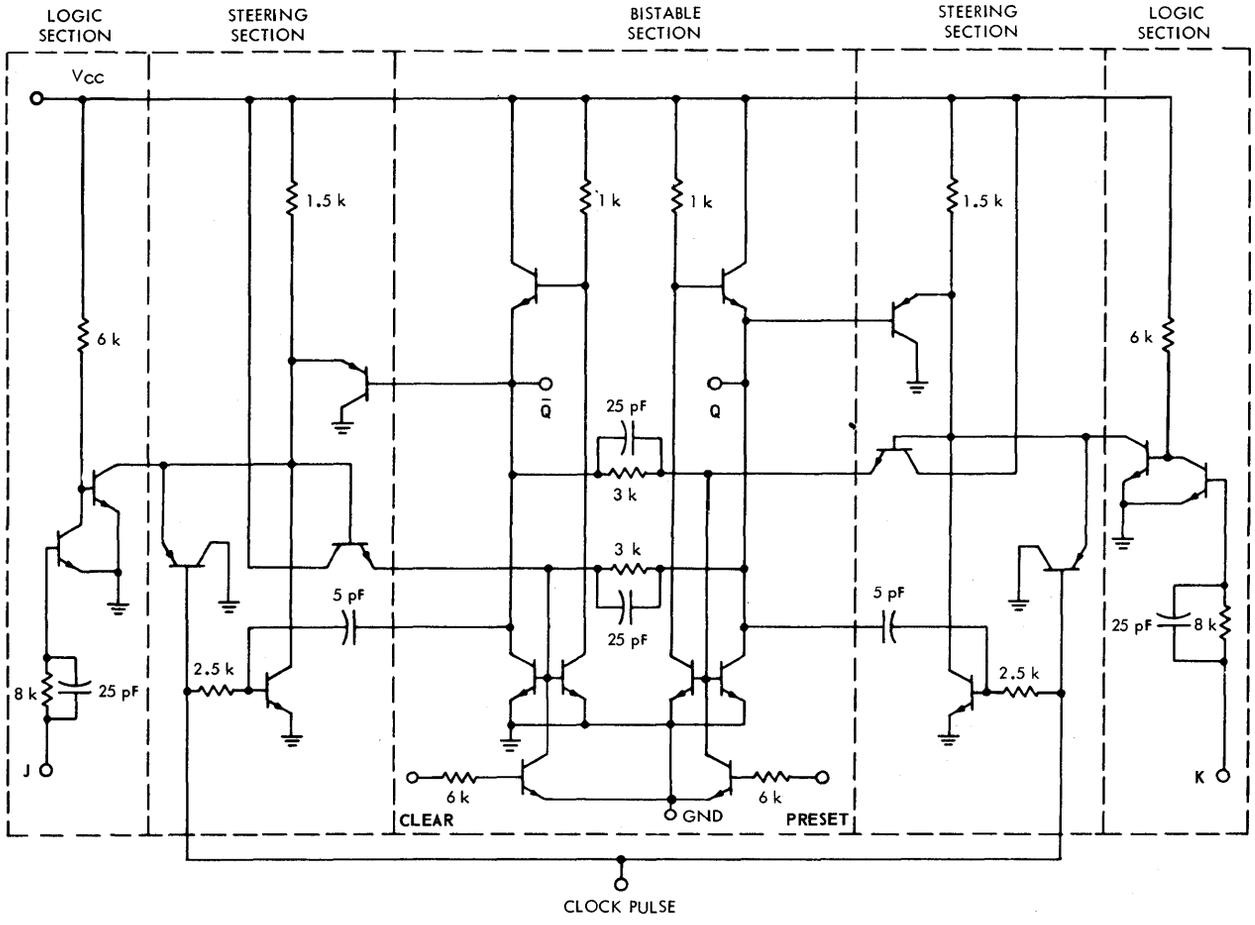
electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, preset, clock and clear	1, 2	V_{CC} = 3 V	1.5		3	V
			V_{CC} = 4 V	1.5		4	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, preset, clock and clear	1, 2		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	3	N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	J, K, or preset input current	3	V_{in} = 2.7 V	0		0.5	mA
I_{in}	Clock input current	3	V_{in} = 2 V	0		2.5	mA
			V_{in} = 0.3 V, T_A = –55°C			–1.25	mA
			V_{in} = 0.3 V, T_A = 125°C			–0.95	mA
I_{in}	Clear input current	3	V_{in} = 2.7 V	0		1	mA
$I_{CC(av)}$	Average supply current (each flip-flop)	4	V_{CC} = 3 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		9		mA
			V_{CC} = 4 V, N+ = N– = 0, Toggle = 1 MHz, T_A = 25°C		13		mA

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ V, N + = N– = 0

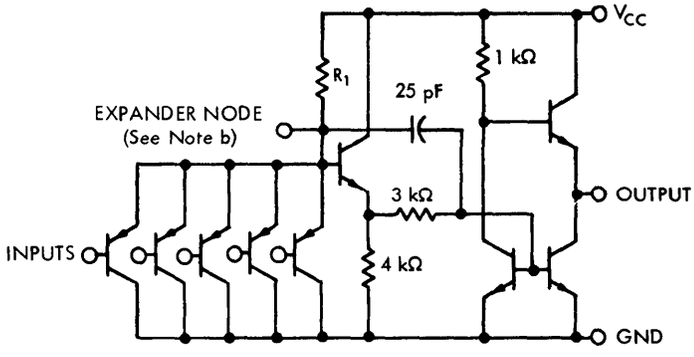
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, $f = 1$ MHz *J and K Input:* $V_{in} = V_{CC}$ *Preset Input:* $V_{in} = 0$ *Clear Input:* $V_{in} = 0$	20	30	ns
t_r	Rise Time			20	45	ns
t_s	Storage Time			40	60	ns
t_f	Fall Time			25	40	ns
$t_{set(1)}$	Time to Set a Logical 1: J or K	23	*Clock Input:* $V_{in} = 2.5$ V, $t_f = 20$ ns, $t_p = 500$ ns, $f = 1$ MHz *J or K Input:* $V_{in(1)} = 2.5$ V, $V_{in(0)} = 0$, $t_r = t_f = 50$ ns	50		ns
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		ns
t_{preset}	Preset Time	24	*Clock Input:* $V_{in} = 0$ *Preset Input:* $V_{in} = 2.5$ V, $t_f = 50$ ns	75		ns
t_{clear}	Clear Time	24	*Clock Input:* $V_{in} = 0$ *Clear Input:* $V_{in} = 2.5$ V, $t_f = 50$ ns	100		ns

schematic (each flip-flop)



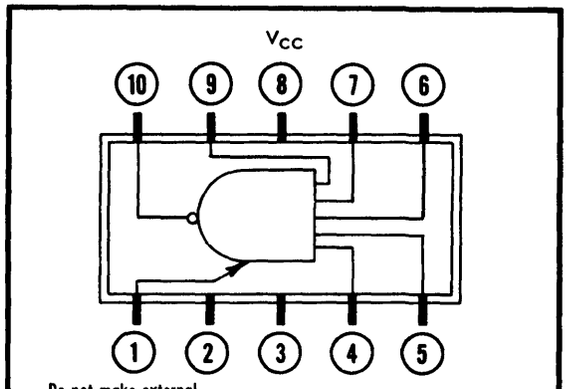
NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

schematic



NOTES: a. Component values shown are nominal.

b. Four SN5320 expanders may be fanned into one SN5310 to provide a total fan-in of 25. If expander is not used, leave pin (1) open.



positive logic

$10 = \overline{4 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 1}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out Into Positive Loads, N+ 10
Maximum Fan-out Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(1)X}$	Input voltage required at expander node (pin (1)) to ensure logical 0 (on level) at output	6	V_{CC} = 3 V, T_A = –55°C	2.35		3	V
			V_{CC} = 3 V T_A = 125°C	1.9		3	V
			V_{CC} = 4 V, T_A = –55°C	3.15		4	V
			V_{CC} = 4 V, T_A = 125°C	2.7		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{in(0)X}$	Input voltage required at expander node (pin (1)) to ensure logical 1 (off level) at output	8	T_A = –55°C	0		1.5	V
			T_A = 125°C	0		0.95	V

CAUTION:

This device was formerly TYPE SN531. Pin numbers of the SN5310 have been renumbered in accordance with TO-89. The electrical functions of the SN531 and the SN5310 are in the same physical location. See **pin identification,** *page 2004, for SN531 pin numbers.*

electrical characteristics (continued)

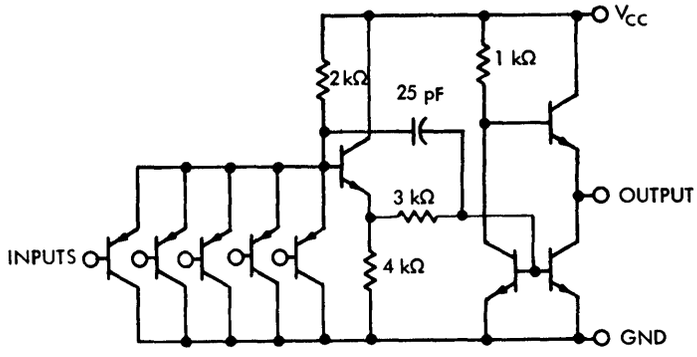
(unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C			0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	9	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA
R_1	Resistance value of R_1	10	T_A = –55°C	1.24		2.6	kΩ
			T_A = 125°C	1.7		3.25	kΩ

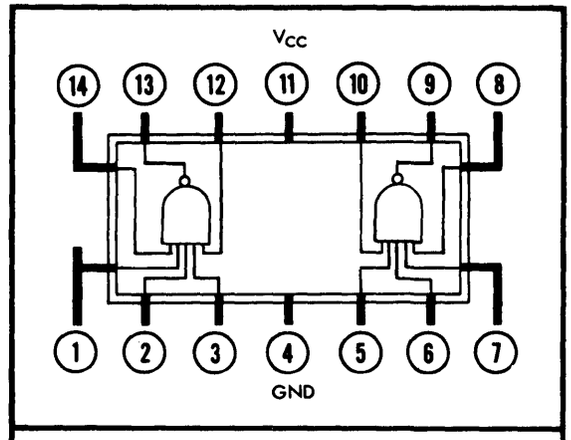
switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N–= 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	35	45	ns
t_r	Rise Time			40	50	ns
t_s	Storage Time			25	45	ns
t_f	Fall Time			30	40	ns
t_{pd}	Propagation Delay Time	26		30		ns

schematic (each gate)



Component values shown are nominal



positive logic

$9 = \overline{5 \cdot 6 \cdot 7 \cdot 8 \cdot 10}$ $13 = \overline{1 \cdot 2 \cdot 3 \cdot 12 \cdot 14}$

recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+	10
Maximum Fan-out From Each Output Into Negative Loads, N–	10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

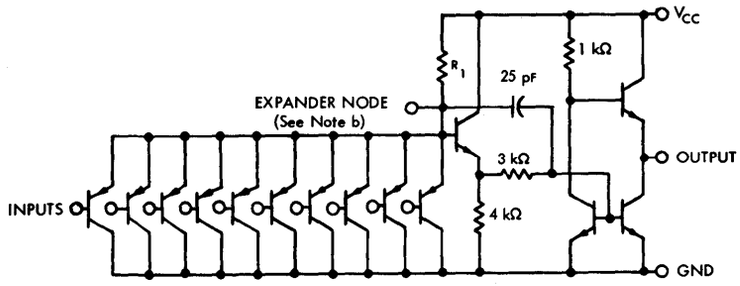
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	9	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	20	30	ns
t_r	Rise Time			25	45	ns
t_s	Storage Time			25	45	ns
t_f	Fall Time			25	40	ns
t_{pd}	Propagation Delay Time	26		25		ns

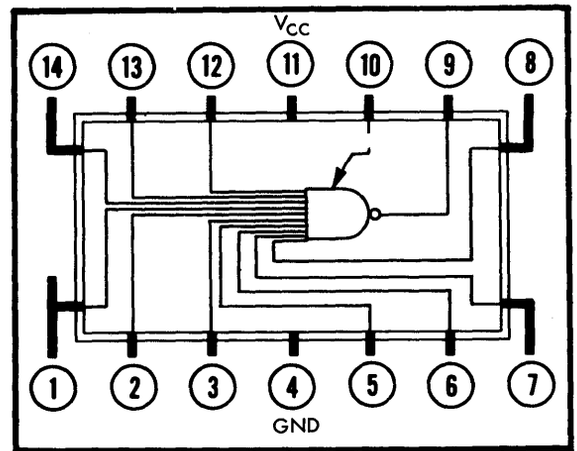
TYPE SN5315
10-INPUT EXPANDABLE NAND/NOR GATE

schematic



NOTES: a. Component values shown are nominal.

b. Three SN5320 expanders may be fanned into one SN5315 to provide a total fan-in of 25. If expander is not used leave pin (10) open.



positive logic

$9 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 8 \cdot 12 \cdot 13 \cdot 14}$

recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out Into Positive Loads, N+	10
Maximum Fan-out Into Negative Loads, N–	10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(1)X}$	Input voltage required at expander node (pin (10)) to ensure logical 0 (on level) at output	6	V_{CC} = 3 V, T_A = –55°C	2.35		3	V
			V_{CC} = 3 V, T_A = 125°C	1.9		3	V
			V_{CC} = 4 V, T_A = –55°C	3.15		4	V
			V_{CC} = 4 V, T_A = 125°C	2.7		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{in(0)X}$	Input voltage required at expander node pin (pin (10)) to ensure logical 1 (off level) at output	8	T_A = –55°C	0		1.5	V
			T_A = 125°C	0		0.95	V

electrical characteristics (continued)

(unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current	9	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA
R_1	Resistance value of R_1	10	T_A = –55°C	1.24		2.6	kΩ
			T_A = 125°C	1.7		3.25	kΩ

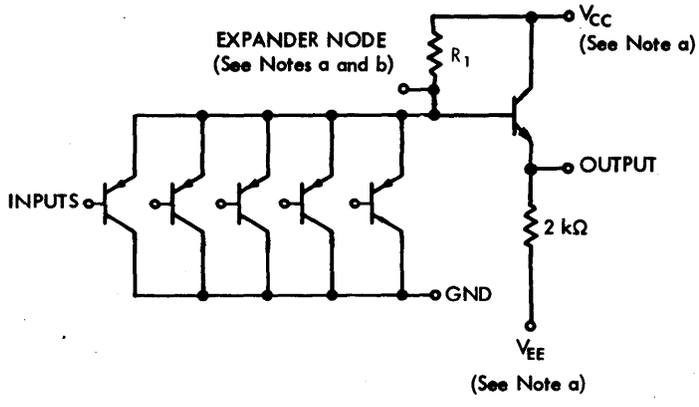
switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	35	45	ns
t_r	Rise Time			40	50	ns
t_s	Storage Time			25	45	ns
t_f	Full Time			30	40	ns
t_{pd}	Propagation Delay Time	26		30		ns

TYPE SN5320
5-INPUT EXPANDABLE AND/OR GATE

ALSO USABLE AS 5-INPUT EXPANDER

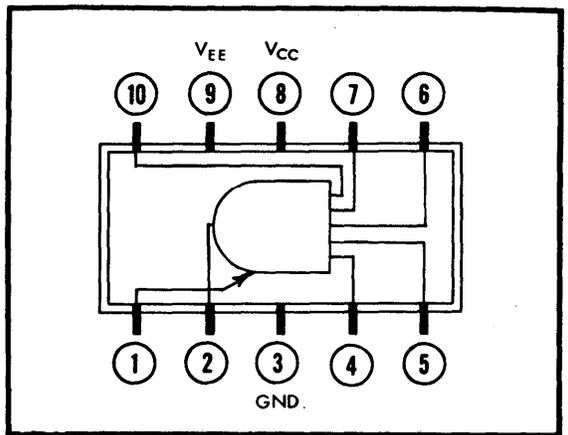
schematic



NOTES: a. When used as an expander for the SN5310, SN5315 or another SN5320, leave V_{CC} and V_{EE} terminals open.

b. Three expanders may be fanned into one SN5315 or 4 expanders may be fanned into one SN5310 or SN5320 to provide a total fan-in of 25.

c. Component values shown are nominal.



positive logic

$2 = 4 \cdot 5 \cdot 6 \cdot 7 \cdot 10$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Supply Voltage V_{EE} . . . . . –3 V
Maximum Fan-out Into Positive Loads, N+ 4
Maximum Fan-out Into Negative Loads, N– 4

NOTE: For cascading capabilities see **design characteristics**, page 2.

electrical characteristics

(unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V, V_{EE} = –3 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure off level at output	11	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 (on level) at output	12		0		0.3	V
$V_{out(0)}$	Logical 0 output voltage (on level)	12	V_{CC} = 3 V, V_{in} = 0.3 V, N– = 4 (I_{sink} = 1 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 0.3 V, N– = 4 (I_{sink} = 0.76 mA), T_A = 125°C	0		0.3	V
$V_{out(0)X}$	Expander node output voltage (off level) with logical 0 at any input	13	V_{CC} = 4 V, V_{in} = 0.3 V, T_A = –55°C			1.5	V
			V_{CC} = 4 V, V_{in} = 0.3 V, T_A = 125°C			0.95	V
$V_{out(1)X}$	Expander node output voltage (on level) with logical 1 at all inputs	14	V_{CC} = 3 V, V_{in} = 1.7 V, T_A = –55°C	2.35			V
			V_{CC} = 3 V, V_{in} = 1.7 V, T_A = 125°C	1.9			V
			V_{CC} = 4 V, V_{in} = 2.5 V, T_A = –55°C	3.15			V
			V_{CC} = 4 V, V_{in} = 2.5 V, T_A = 125°C	2.7			V

CAUTION:

This device was formerly TYPE SN532. Pin numbers of the SN5320 have been renumbered in accordance with TO-89. The electrical functions of the SN532 and the SN5320 are in the same physical location. **See pin identification,** *page 2004, for SN532 pin numbers.*

electrical characteristics, continued

(unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V, V_{EE} = –3 V)

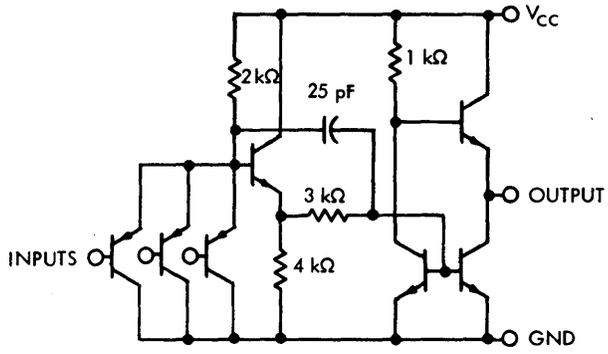
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{(1)}$	Voltage difference from input to output when logical 1 level is applied to all inputs	11	V_{CC} = 3 V, V_{in} = 1.7 V, N+ = 4 (I_{load} = –2 mA)			0.4	V
			V_{CC} = 4 V, V_{in} = 2.5 V, N+ = 4 (I_{load} = –2 mA)			0.4	V
I_{in}	Input current (each input)	12	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level V_{CC} supply current (each gate)	15	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		2.60		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		3.1		mA
$I_{EE(on)}$	On level V_{EE} supply current (each gate)	15	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.7		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.7		mA
$I_{CC(off)}$	Off level V_{CC} supply current (each gate)	15	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		2.6		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		3.05		mA
$I_{EE(off)}$	Off level V_{EE} supply current (each gate)	15	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		2.6		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		3.05		mA
R_1	Resistance value of R_1	15	T_A = –55°C	1.24		2.6	kΩ
			T_A = 125°C	1.7		3.25	kΩ

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, V_{EE} = –3 V, N– = 1

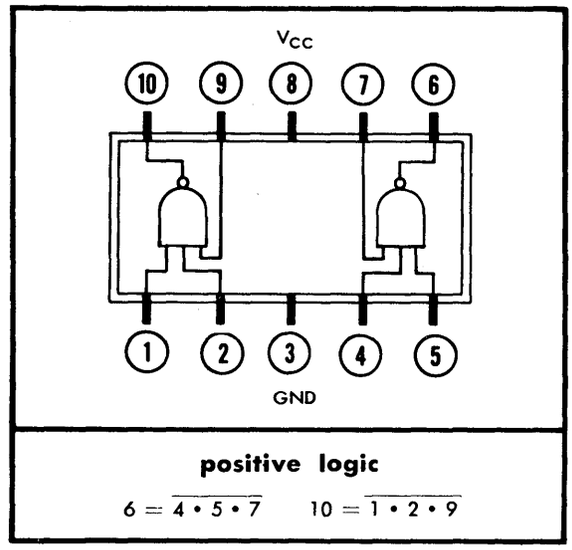
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_{d1}	Delay Time 1	27	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	5	10	ns
t_r	Rise Time			40	200	ns
t_{d2}	Delay Time 2			5	10	ns
t_f	Fall Time			75	100	ns
t_{pd}	Propagation Delay Time	26		5		ns

SN5330
DUAL 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



positive logic

$6 = \overline{4 \cdot 5 \cdot 7}$ $\quad 10 = \overline{1 \cdot 2 \cdot 9}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

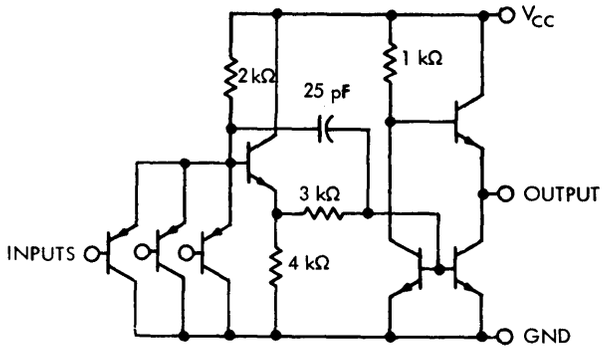
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4V	2.5		4	V
$V_{in(0)}$	Logica 0 input voltage required at any input terminal that will ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	9	V_{CC} = 3V, V_{in} = 0.3 V, N+ = N– + 0, T_A = 25°C		1.2		mA
			V_{CC} = 4V, V_{in} = 0.3 V, N+ = N– + 0, T_A = 25°C		1.6		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

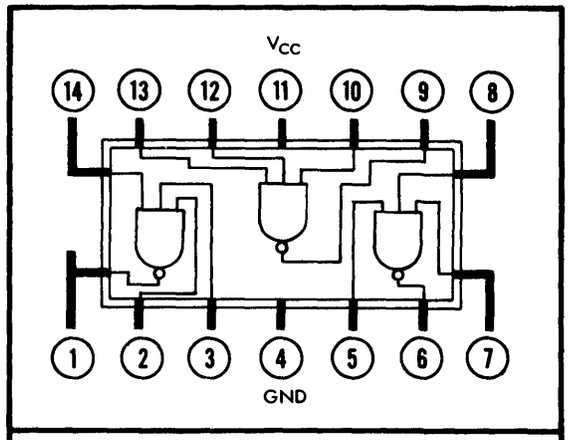
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	20	30	ns
t_r	Rise Time			25	45	ns
t_s	Storage Time			25	45	ns
t_f	Fall Time			25	40	ns
t_{pd}	Propagation Delay Time	26		25		ns

CAUTION:
This device was formerly TYPE SN533. Pin numbers of the SN5330 have been renumbered in accordance with TO-89. The electrical functions of the SN533 and the SN5330 are in the same physical location. *See* **pin identification**, *page 2004, for SN533 pin numbers.*

schematic (each gate)



Component values shown are nominal.



positive logic

$1 = \overline{2 \cdot 3 \cdot 14}$ $6 = \overline{5 \cdot 7 \cdot 8}$ $9 = \overline{10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+	10
Maximum Fan-out From Each Output Into Negative Loads, N–	10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

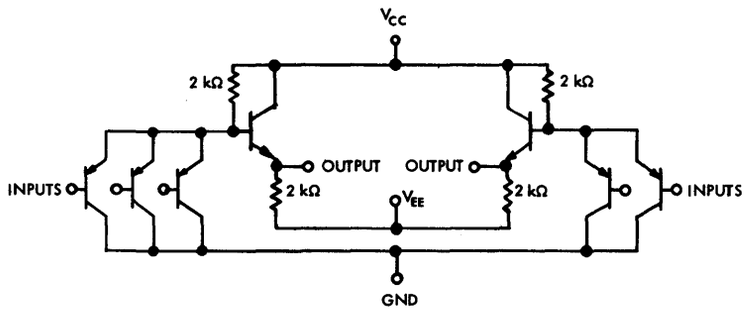
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	9	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

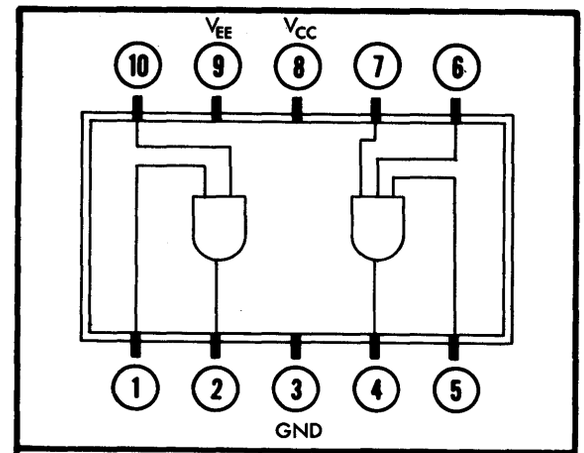
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	20	30	ns
t_r	Rise Time			25	45	ns
t_s	Storage Time			25	45	ns
t_f	Fall Time			25	40	ns
t_{pd}	Propagation Delay Time	26		25		ns

TYPE SN5340
DUAL AND/OR GATE

schematic



NOTES: a. Component values shown are nominal.
b. Do not connect pins (2) and (4) together.



positive logic

2 = 1 · 10 4 = 5 · 6 · 7

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Supply Voltage V_{EE} . . . . . –3 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 4
Maximum Fan-out From Each Output Into Negative Loads, N– 4

NOTE: For cascading capabilities see **design characteristics**, page 2.

electrical characteristics
(unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V, V_{EE} = –3 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 1 (off level) at output	11	V_{CC} = 3 V	1.7	3	V
			V_{CC} = 4 V	2.5	4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 0 (on level) at output	12		0	0.3	V
$\Delta V_{(1)}$	Voltage difference from input to output when logical 1 level is applied to all inputs	11	V_{CC} = 3 V, V_{in} = 1.7 V, N+ = 4 (I_{load} = –2 mA)		0.4	V
			V_{CC} = 4 V, V_{in} = 2.5 V, N+ = 4 (I_{load} = –2 mA)		0.4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	12	V_{CC} = 3 V, V_{in} = 0.3 V, N– = 4 (I_{sink} = 1 mA), T_A = –55°C	0	0.3	V
			V_{CC} = 3 V, V_{in} = 0.3 V, N– = 4 (I_{sink} = 0.76 mA), T_A = 125°C	0	0.3	V

CAUTION:

This device was formerly TYPE SN534. Pin numbers of the SN5340 have been renumbered in accordance with TO-89. The electrical functions of the SN534 and the SN5340 are in the same physical location. See **pin identification**, *page 2004, for SN534 pin numbers.*

electrical characteristics, continued

(unless otherwise noted T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V, V_{EE} = –3 V)

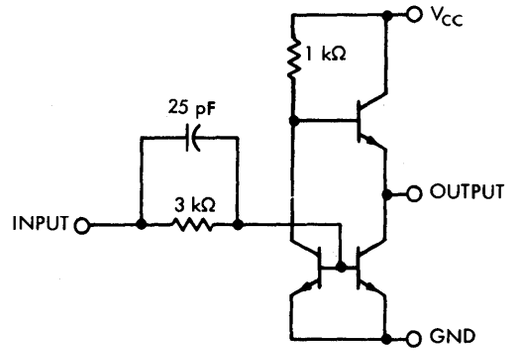
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{in}	Input current (each input)	12	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level V_{CC} supply current (each gate)	15	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		2.6		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		3.1		mA
$I_{EE(on)}$	On level V_{EE} supply current (each gate)	15	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.7		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.7		mA
$I_{CC(off)}$	Off level V_{CC} supply current (each gate)	15	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		2.6		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		3.05		mA
$I_{EE(off)}$	Off level V_{EE} supply current (each gate)	15	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		2.6		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		3.05		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

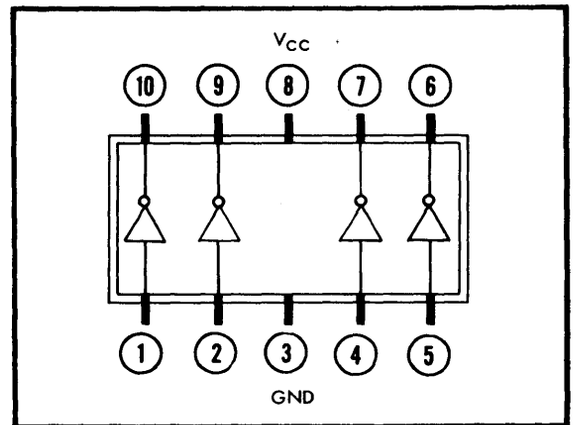
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_{d1}	Delay Time 1	27	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	5	10	ns
t_r	Rise Time			40	200	ns
t_{d2}	Delay Time 2			5	10	ns
t_f	Fall Time			75	100	ns
t_{pd}	Propagation Delay Time	26		5		ns

TYPE SN5350
QUADRUPLE INVERTER/DRIVER

schematic (each inverter)



Component values shown are nominal



positive logic

$6 = \overline{5}$ $\quad 9 = \overline{2}$

$7 = \overline{4}$ $\quad 10 = \overline{1}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V

Maximum Fan-out From Each Output Into Positive Loads, N+ 10

Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted, $T_A = -55°C$ to $125°C$, $V_{CC} = 3$ V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required to ensure logical 0 (on level) at output	16	$V_{CC} = 3$ V	1.5		3	V
			$V_{CC} = 4$ V	1.5		4	V
$V_{in(0)}$	Logical 0 input voltage required to ensure logical 1 (off level) at output	16		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	16	$V_{CC} = 3$ V, $V_{in} = 0.3$ V, N+ = 10 ($I_{load} = -5$ mA)	1.7		3	V
			$V_{CC} = 4$ V, $V_{in} = 0.3$ V, N+ = 10 ($I_{load} = -5$ mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	16	$V_{CC} = 3$ V, $V_{in} = 1.7$ V, N– = 10 ($I_{sink} = 2.5$ mA), $T_A = -55°C$	0		0.3	V
			$V_{CC} = 3$ V, $V_{in} = 1.7$ V, N– = 10 ($I_{sink} = 1.9$ mA), $T_A = 125°C$	0		0.3	V
I_{in}	Input current	16	$V_{CC} = 4$ V, $V_{in} = 2.7$ V, N+ = N– = 0			1	mA
$I_{CC(on)}$	On level supply current (each inverter)	16	$V_{CC} = V_{in} = 3$ V, N+ = N– = 0, $T_A = 25°C$		3.3		mA
			$V_{CC} = V_{in} = 4$ V, N+ = N– = 0, $T_A = 25°C$		4.5		mA

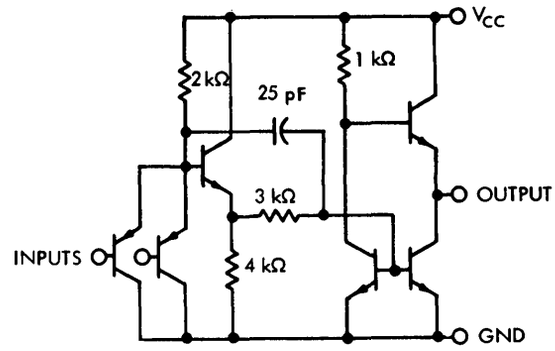
switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ V, N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* $V_{in} = 2.5$ V, f = 1 MHz, $t_p = 500$ ns, $t_r = t_f = 20$ ns	20	30	ns
t_r	Rise Time			25	45	ns
t_s	Storage Time			25	45	ns
t_f	Fall Time			25	40	ns
t_{pd}	Propagation Delay Time	26		25		ns

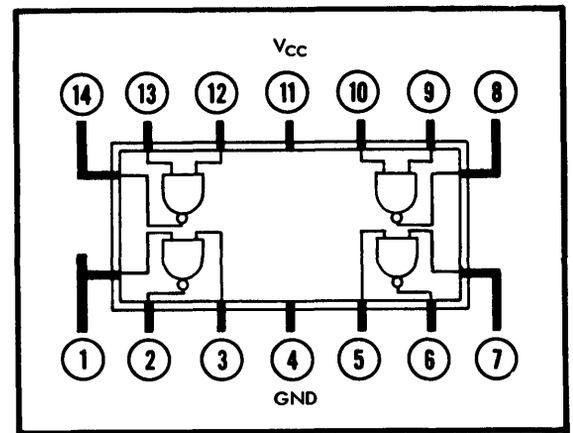
CAUTION:

This device was formerly TYPE SN535. Pin numbers of the SN5350 have been renumbered in accordance with TO-89. The electrical functions of the SN535 and the SN5350 are in the same physical location. See **pin identification,** *page 2004, for SN535 pin numbers.*

schematic (each gate)



Component values shown are nominal



positive logic

$2 = \overline{1 \cdot 3}$ $6 = \overline{5 \cdot 7}$ $8 = \overline{9 \cdot 10}$ $14 = \overline{12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

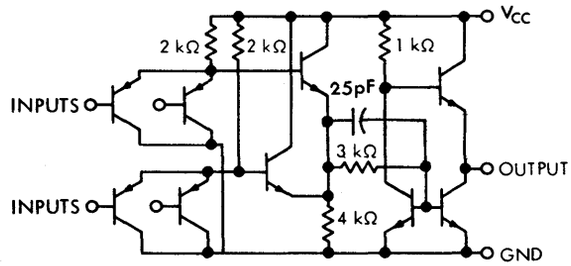
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	7	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10, (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10, (I_{sink} = 1.9 mA), T_A = – 125°C	0		0.3	V
I_{in}	Input current (each input)	7	V_{in} = 0.3 V, N+ = N– = 0, T_A = – 55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	9	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	9	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

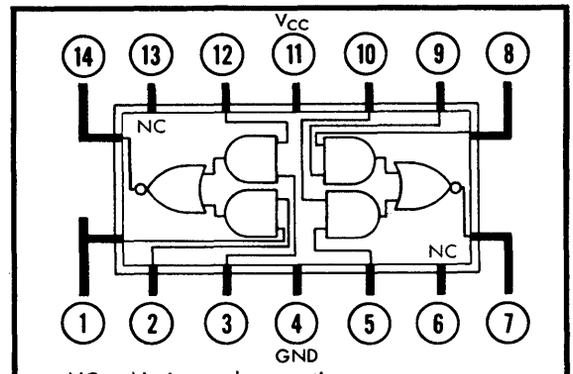
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f= 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns		20	30	ns
t_r	Rise Time				25	45	ns
t_s	Storage Time				25	45	ns
t_f	Fall Time				25	40	ns
t_{pd}	Propagation Delay Time	26			25		ns

TYPE SN5370
DUAL EXCLUSIVE-OR GATE

schematic (each gate)



Component values shown are nominal



NC — No internal connection.

positive logic

$7 = \overline{(5 \cdot 10)+(8 \cdot 9)}$ $14 = \overline{(1 \cdot 2)+(3 \cdot 12)}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 (on level) at output	17	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 (off level) at output	18		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	18	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	17	V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 3 V, V_{in} = 1.7 V, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	18	V_{in} = 0.3 V, N+ = N– = 0, T_A = –55°C			–0.25	mA
			V_{in} = 0.3 V, N+ = N– = 0, T_A = 125°C			–0.19	mA
$I_{CC(on)}$	On level supply current (each gate)	17	V_{CC} = V_{in} = 3 V, N+ = N– = 0, T_A = 25°C		3.3		mA
			V_{CC} = V_{in} = 4 V, N+ = N– = 0, T_A = 25°C		4.5		mA
$I_{CC(off)}$	Off level supply current (each gate)	18	V_{CC} = 3 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.2		mA
			V_{CC} = 4 V, V_{in} = 0.3 V, N+ = N– = 0, T_A = 25°C		1.6		mA

switching characteristics, T_A = 25°C, V_{CC} = 3.5 V, N– = 1

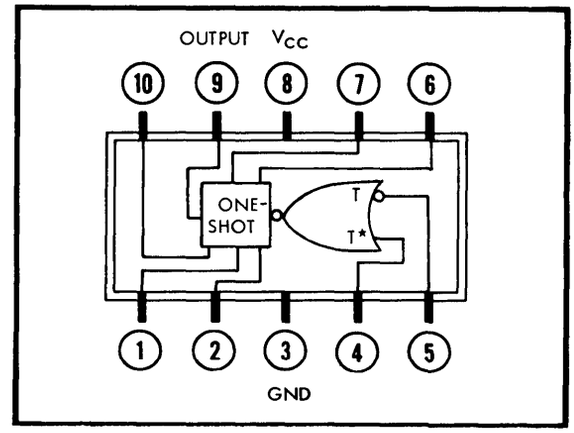
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	25	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 500 ns, t_r = t_f = 20 ns	30	60	ns
t_r	Rise Time			30	60	ns
t_s	Storage Time			100	200	ns
t_f	Fall Time			100	200	ns
t_{pd}	Propagation Delay Time	26		65		ns

logic

TRUTH TABLE

positive logic				
T		T★		OUTPUT
t_n	t_{n+1}	t_n	t_{n+1}	
1	1	..	..	INHIBITED (logical 1)
..	..	0	0	INHIBITED (logical 1)
0	0	1	0	ONE-SHOT (logical 0 for $t_{p\ ns}$)
0	1	1	1	ONE-SHOT (logical 0 for $t_{p\ ns}$)

t_n = bit time before change in input levels
t_{n+1} = bit time after change in input levels



recommended operating conditions

Supply Voltage V_{CC}	3 V to 4 V
Maximum Fan-out Into Positive Loads, N+	10
Maximum Fan-out Into Negative Loads, N–	10
Minimum Set-Up Time, $t_{set\text{-}up}$†	400 ns

electrical characteristics (unless otherwise noted, T_A = –55°C to 125°C, V_{CC} = 3 V to 4 V)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at T or T★ input terminal	19	V_{CC} = 3 V	1.7		3	V
			V_{CC} = 4 V	2.5		4	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at T or T★ terminal	19		0		0.3	V
$V_{out(1)}$	Logical 1 output voltage (off level)	20	V_{CC} = 3 V, N+ = 10 (I_{load} = –5 mA)	1.7		3	V
			V_{CC} = 4 V, N+ = 10 (I_{load} = –5 mA)	2.7		4	V
$V_{out(0)}$	Logical 0 output voltage (on level)	20	V_{CC} = 3 V, $V_{③}$ = 0.3 V, pin ⑩ open, N– = 10 (I_{sink} = 2.5 mA), T_A = –55°C	0		0.3	V
			V_{CC} = 4 V, $V_{③}$ = 0.3 V, pin ⑩ open, N– = 10 (I_{sink} = 1.9 mA), T_A = 125°C	0		0.3	V
I_{in}	Input current (each input)	19	V_{in} = 2.7 V, N+ = N– = 0			0.5	mA
$I_{CC(av)}$	Average supply current	21	V_{CC} = 3 V, N+ = N– = 0, Duty cycle = 50%, T_A = 25°C		4.8		mA
			V_{CC} = 4 V, N+ = N– = 0, Duty cycle = 50%, T_A = 25°C		6.3		mA

†This is the minimum time necessary for the input signal to dwell before the triggering transition begins and applies when pin ⑥ is shorted to pin ⑦ and pin ② is shorted to pin ⑩. Set-up time begins only after the occurrence of the 10% point of the output fall time.
‡Pin ⑥ shorted to pin ⑦ and pin ② shorted to pin ⑩ unless otherwise noted.

CAUTION:

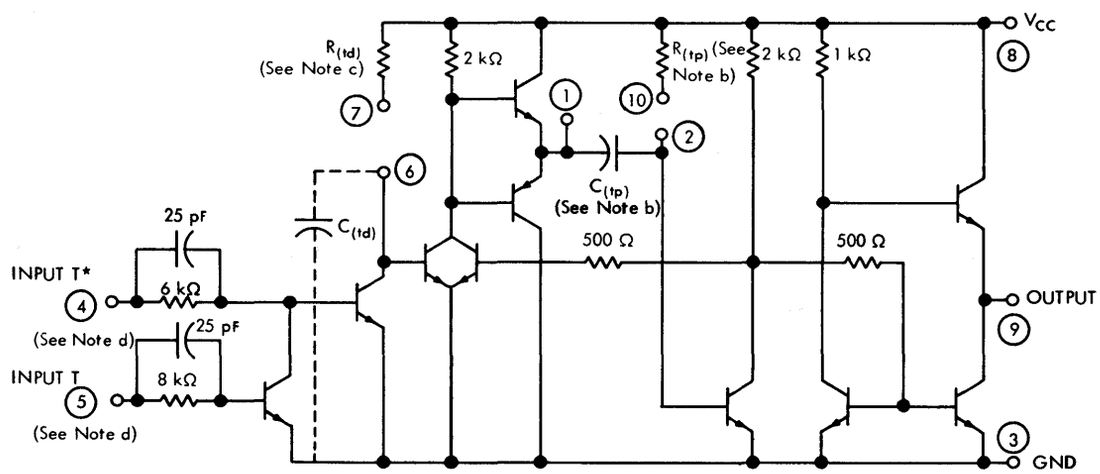
Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See **pin identification,** *page 2004, for former pin numbers.*

switching times, T_A = 25°C, V_{CC} = 3.5 V, fan-out N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_{d1}	Delay Time after Positive-going Transition at T (pin 5)	28	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 400 ns, $t_r = t_f$ = 20 ns		90	130	ns
t_{d2}	Delay Time after Negative-going Transition at T★ (pin 4)				90	130	ns
t_r	Rise Time				35	60	ns
t_f	Fall Time				35	60	ns
t_p	Output Pulse Width	28	*Input:* V_{in} = 2.5 V, f = 1 MHz, t_p = 400 ns, $t_r = t_f$ = 20 ns	100	250	400	ns

‡Pin 6 shorted to pin 7 and pin 2 shorted to pin 10 unless otherwise noted.

schematic



NOTES: a. Component values shown are nominal.

b. Output pulse width t_p is proportional to $R_{(tp)}C_{(tp)}$. Output pulse width may be modified using pins 1, 2, 8, and 10 to change effective values of of $R_{(tp)}$ and $C_{(tp)}$. Nominal value of internal $R_{(tp)}$ is 8 kΩ and $C_{(tp)}$ is 25 pF. Value of modified $R_{(tp)}$ should be maintained between 6 kΩ and 15 kΩ.

CAUTION:

When the effective value of $C_{(tp)} \geq 0.1\ \mu F$, a 560-Ω resistor must be connected in series with the external portion of $C_{(tp)}$ (between pins 1 and 2).

c. Delay time (t_d) may be modified using pins 3, 6, 7, and 8 to change effective values of $R_{(td)}$ and $C_{(td)}$. Nominal value of internal $R_{(td)}$ is 2 kΩ. Value of modified $R_{(td)}$ should be maintained between 2 kΩ and 10 kΩ.

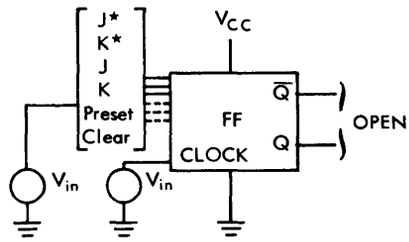
d. T triggers on a positive transition to logical 1 level, and T★ triggers on a negative transition to logical 0 level. When triggering with T input, hold T★ at logical 1. When triggering with T★ input, hold T at logical 0.

CAUTION:

Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See **pin identification,** *page 2004, for former pin numbers.*

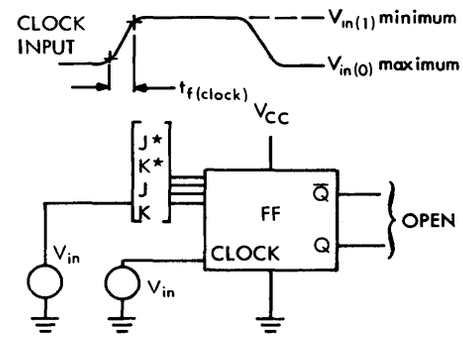
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †



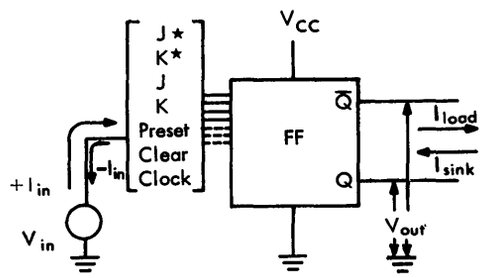
1. Each input tested separately with unused inputs at worst case levels.
2. The flip-flop is tested for performance in accordance with truth table.
3. Preset and clear tested with $V_{in(clock)} = 0$.

FIGURE 1



1. The flip-flop is tested for ripple action with the following conditions:
   Clock input: $V_{in(1)}$ minimum, $V_{in(0)}$ maximum, $t_f = 150$ ns (maximum).
   All other inputs: $V_{in(1)}$ minimum.

FIGURE 2



1. Each input tested individually for input current.
2. Each output tested individually for $V_{out(1)}$ and $V_{out(0)}$.

FIGURE 3

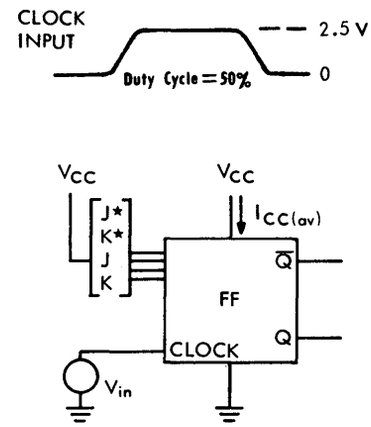
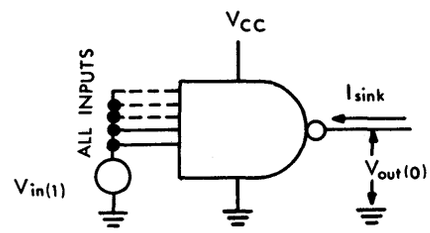


FIGURE 4



1. All inputs tested simultaneously.

FIGURE 5

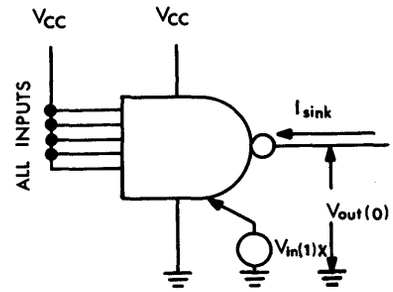
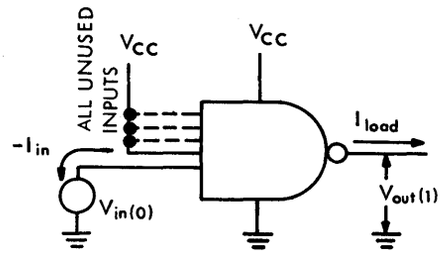


FIGURE 6

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†(continued)



1. Each input tested separately.

FIGURE 7

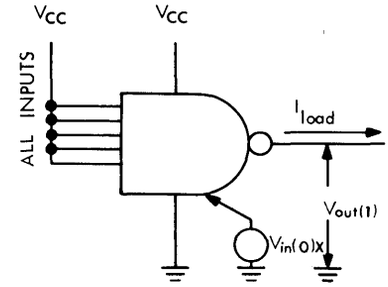
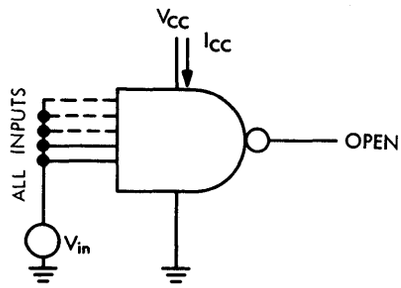
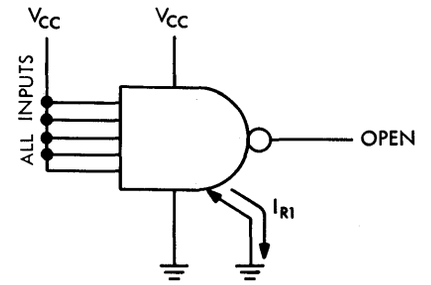


FIGURE 8



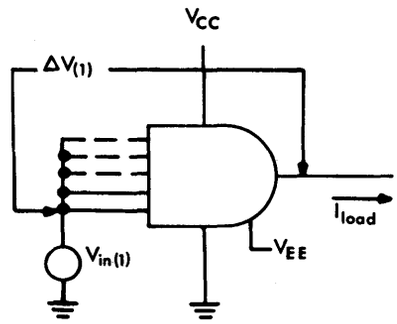
1. *Test on-level and off-level currents.*

FIGURE 9



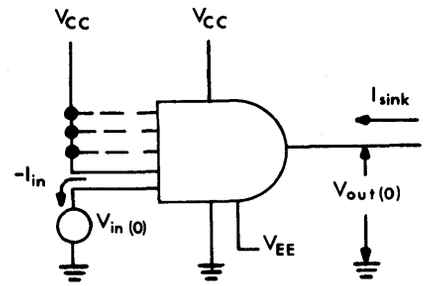
1. $R_1 = \dfrac{V_{CC}}{I_{R1}}$

FIGURE 10



1. All inputs tested simultaneously.
2. SN5320 expander node is open.

FIGURE 11



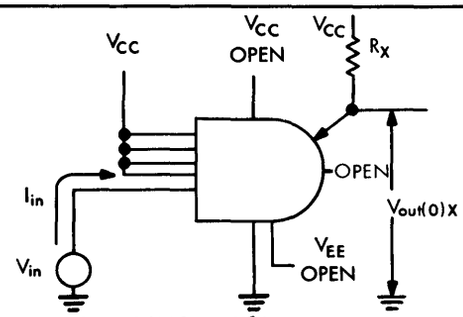
1. Each input tested separately.
2. SN5320 expander node is open.

FIGURE 12

† Arrows indicate actual direction of current flow

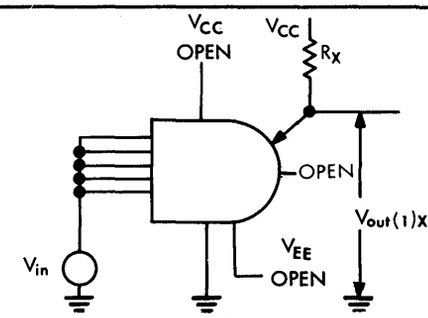
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†(continued)



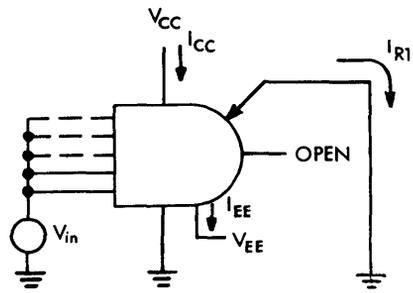
1. $R_X = 1.24\ k\Omega$ at $-55°C$.
2. $R_X = 1.7\ k\Omega$ at $125°C$.
3. Each input tested separately.
4. R_X is worst-case equivalent of R_1 in the SN5310, SN5315, or SN5320.

FIGURE 13



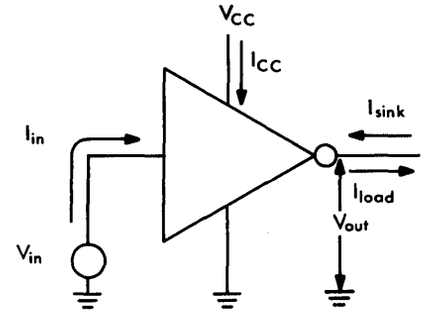
1. $R_X = 2.6\ k\Omega$ at $-55°C$.
2. $R_X = 3.25\ k\Omega$ at $125°C$.
3. All inputs tested simultaneously.
4. R_X is worst-case equivalent of R_1 in the SN5310, SN5315 or SN5320.

FIGURE 14



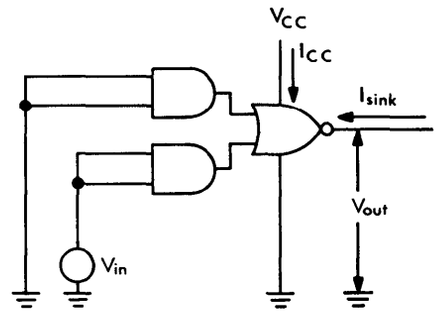
1. I_{CC} and I_{EE} on-level and off-level currents are tested with expander node open.
2. $R_1 = \frac{V_{CC}}{I_{R1}}$

FIGURE 15



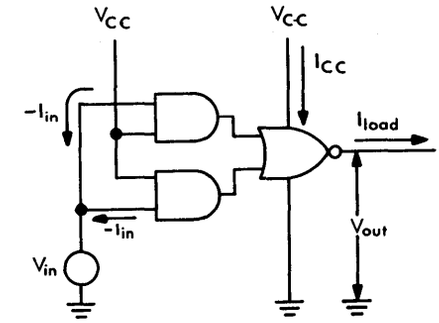
1. Each inverter is tested separately.

FIGURE 16



1. Each AND section tested separately.

FIGURE 17



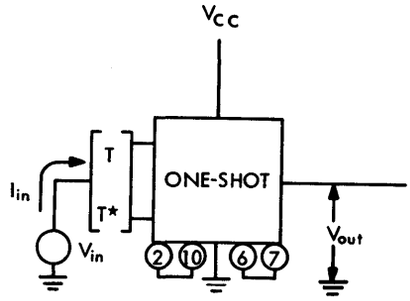
1. Each input pair is tested separately for $V_{out(1)}$.
2. Each input tested separately for I_{in}.

FIGURE 18

† Arrows indicate actual direction of current flow

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each input tested separately.
2. With minimum $V_{in(1)}$ and maximum $V_{in(0)}$, and the unused input at the worst-case level, the one-shot output is verified.

FIGURE 19

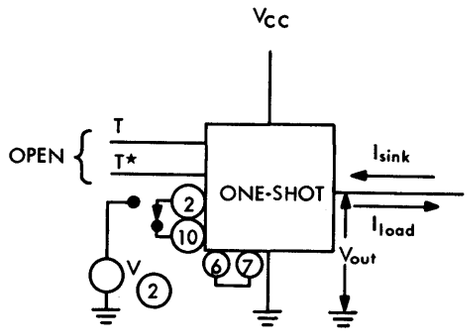
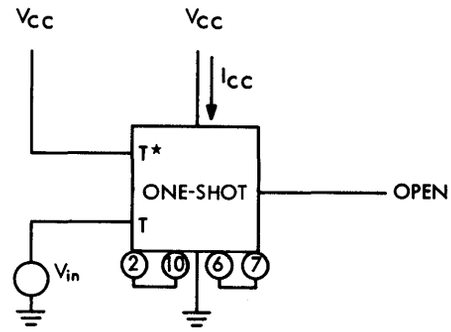


FIGURE 20



1. I_{CC} is measured with a 50% duty cycle.

FIGURE 21

CAUTION:

Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See **pin identification,** *page 2004, for former pin numbers.*

switching characteristics

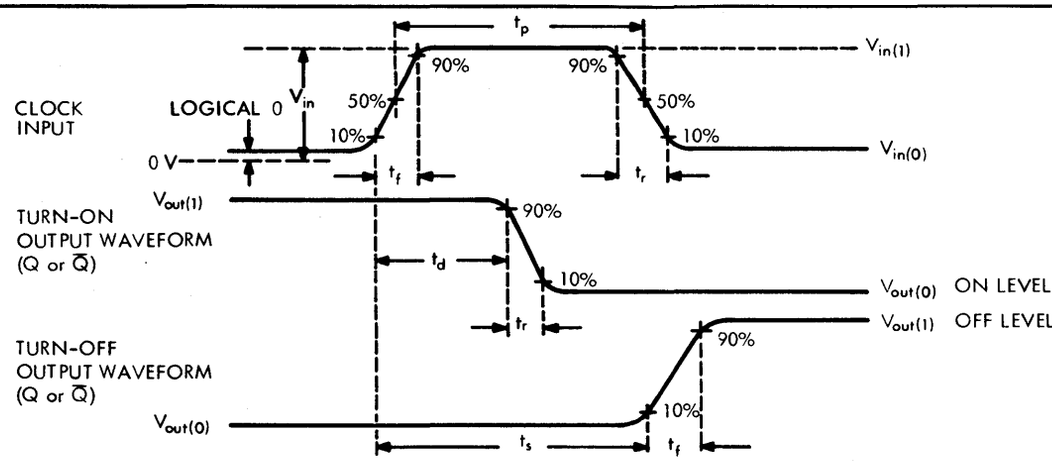


FIGURE 22. CLOCK PULSE AND OUTPUT VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

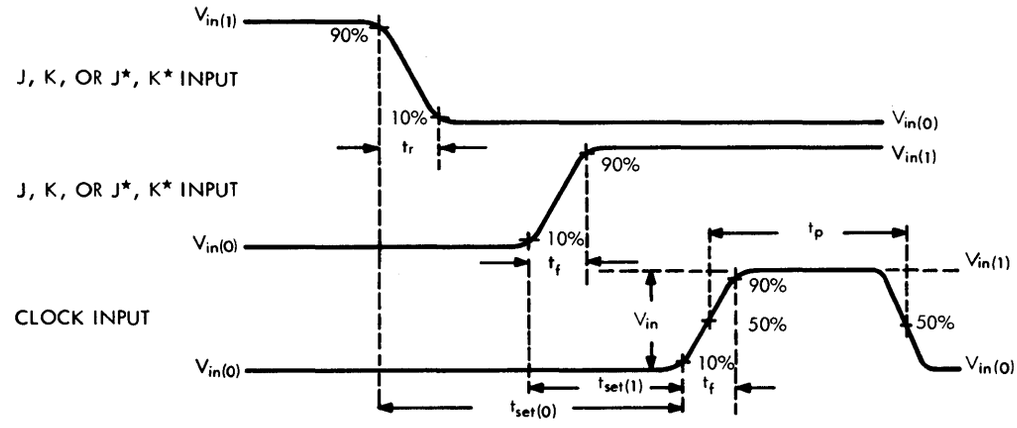
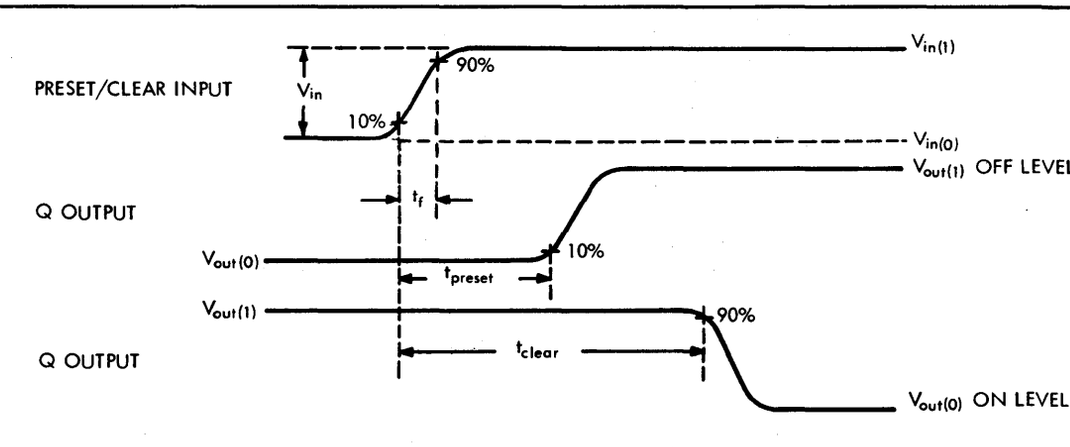


FIGURE 23. TIME TO SET A LOGICAL LEVEL VOLTAGE WAVEFORMS



1. $V_{in(clock)} = 0$

FIGURE 24. PRESET/CLEAR TIME VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

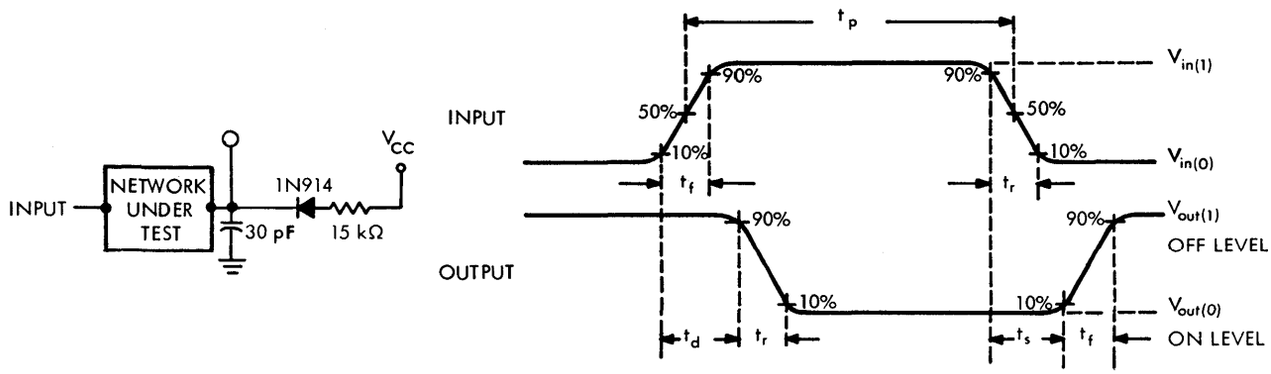
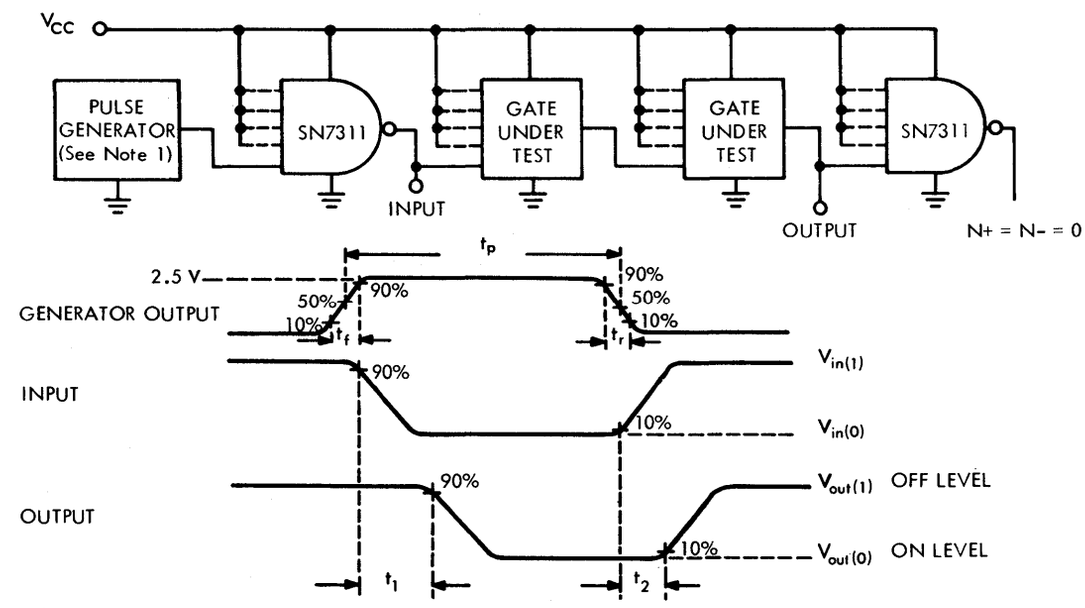


FIGURE 25. NAND/NOR GATE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS



NOTES: 1. The generator has the following characteristics: $t_r = t_f = 20$ ns, $t_p = 500$ ns, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.

2. Propagation delay: $t_{pd} = \frac{t_1 + t_2}{4}$

FIGURE 26. GATE PROPAGATION DELAY TEST CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

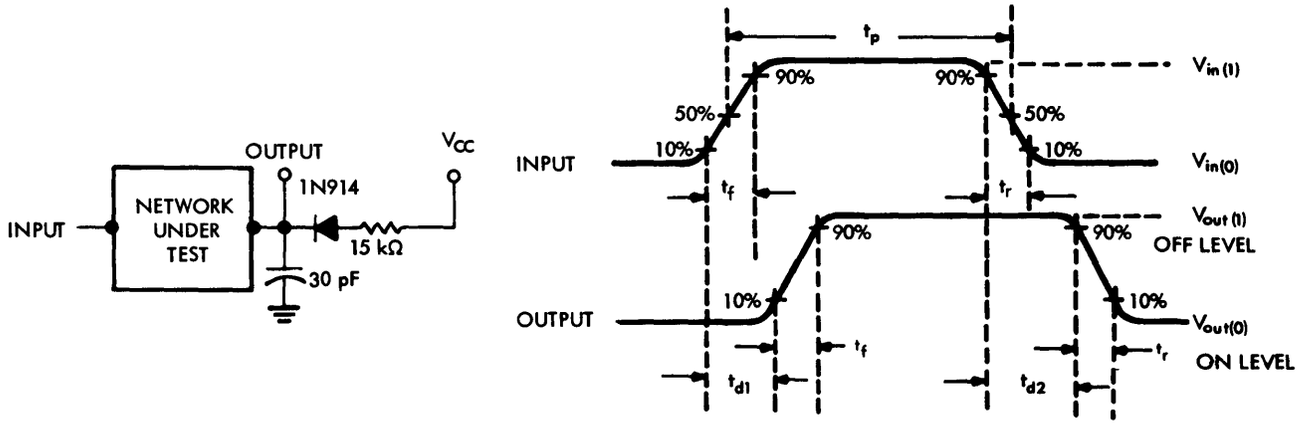


FIGURE 27. AND/OR GATE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

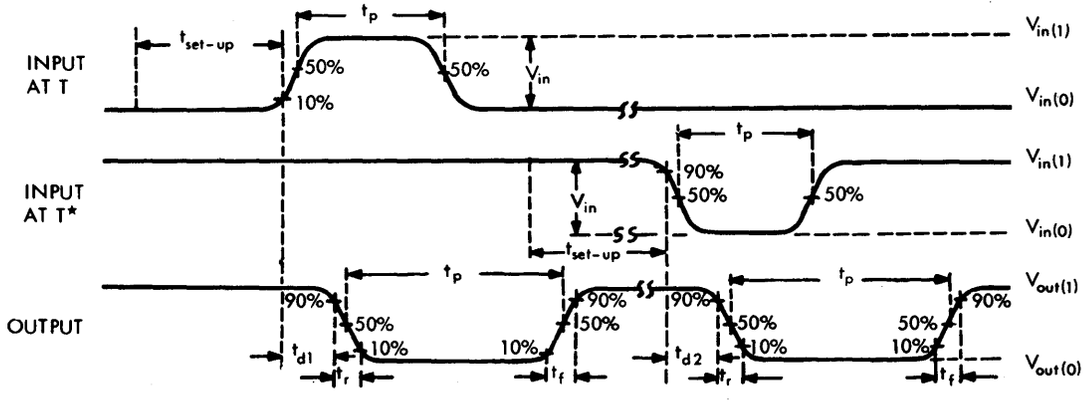


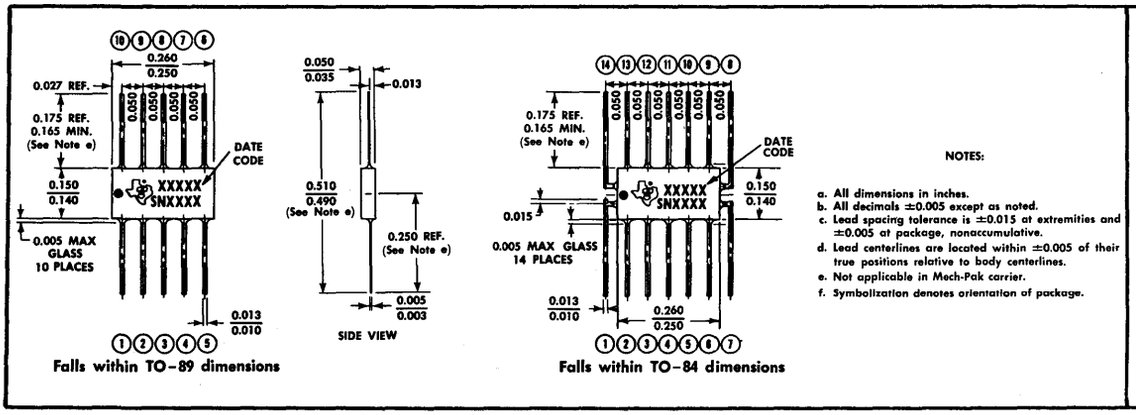
FIGURE 28. ONE-SHOT VOLTAGE WAVEFORMS

SERIES 53
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

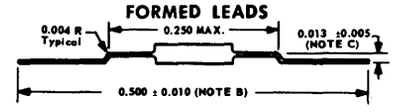
general

Series 53 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 53 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.



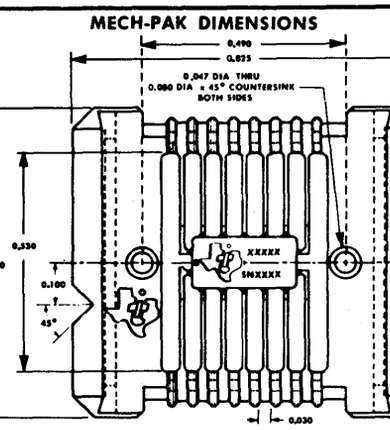
NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

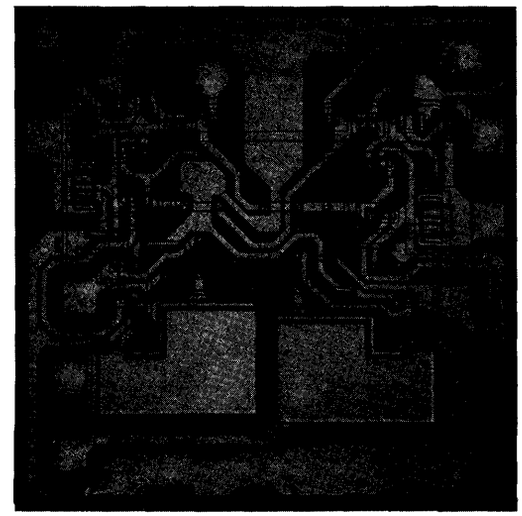
‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

SERIES 15 930
BULLETIN NO. DL-S 668840, NOVEMBER, 1966
REPLACES BULLETIN NO. DL-S 668129, FEBRUARY 1966

DIODE-TRANSISTOR LOGIC (DTL) NETWORKS FOR DIGITAL SYSTEMS

application

The series 15 930 networks are designed for use in medium to high-speed digital applications, including data handling, computer and control systems. Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C.



TYPE SN15 950 PULSE-TRIGGERED BINARY BAR

features

LOW SYSTEM COST

- **multifunction gates offering low cost per logic function**
- **electrically designed specifically for monolithic integrated-circuit technology**

PERFORMANCE

- **high speed**
- **high d-c noise margins**
- **low power dissipation**
- **good fan-out capability**

EASE OF DESIGN

- **familiar logic configuration (DTL)**
- **single-ended output — dot-OR logic**
- **complete family for design flexibility**
- **single power supply**

description

Series 15 930 is a complete family of diode-transistor logic (DTL) which is most attractive when high performance and low cost per function are necessities to system design.

The basic family consists of NAND gates, an expander, a buffer, a power gate, master-slave flip-flops, a pulse-triggered binary and a monostable multivibrator. Dual, triple, and quadruple multi-function gates are available to minimize system package count.

This line features a unique combination of high speed, high d-c noise margin, and low power dissipation. The single-ended output lends itself readily to performing dot-OR logic thus reducing the number of different type functional blocks in a system.

CONTENTS

†Patented by Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

typical operating characteristics, T_A = −55°C to 125°C, supply voltage V_{CC} = 4.5 V to 5.5 V

Speed:	Gate Propagation Delay	25 ns
	Monostable Multivibrator Propagation Delay	20 ns
	Flip-Flop Clock Rate (SN15 931, SN15 945, SN15 948)	7 MHz
	Pulse-Triggered Binary Clock Rate	20 MHz
Fan-Out Capability:	Standard Gates (SN15 930, SN15 946, SN15 962)	8
	Buffer (SN15 932)	25
	Power Gate (SN15 944)	27
	Monostable Multivibrator (SN15 951)	10
	Flip-Flops: SN15 931	7
	SN15 945	10
	SN15 948	9
	Pulse-Triggered Binary	8
D-C Margin:	At logical 1	500 mV
	At logical 0	500 mV
Average Power Dissipation:	Per Gate	5 mW
	Per Flip-Flop	20 mW

design characteristics

Series 15 930 is a complete line of high-speed, high-noise-margin, low-power-dissipation, saturated DTL logic. The circuitry is a modification of the conventional DTL in that it utilizes only one power supply and provides a nonsaturating offset transistor in place of one of the offset diodes.

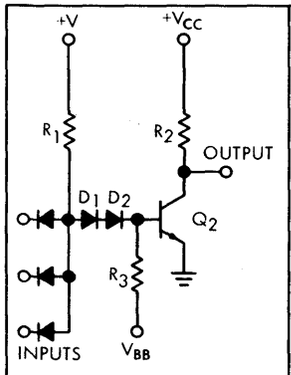


Figure A — Conventional DTL

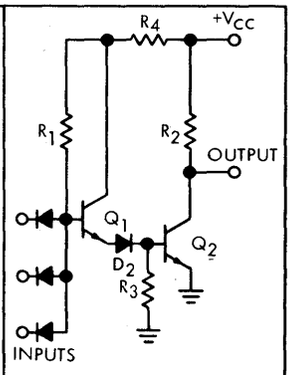


Figure B — Series 15 930

Replacing the offset diode D_1 with transistor Q_1 offers both the manufacturer and the customer a number of advantages:

1. Elimination of the V_{BB} power supply makes one more pin available for multifunction capability, which in turn reduces system package count.
2. Reduction of size of resistor R_3 from 20 kΩ to 5 kΩ invites a substantial reduction in the overall size of the monolithic chip and improves yields. Both of these factors contribute heavily to reducing manufacturing costs.
3. Reduction of turn-off current transients on signal lines is accomplished because the stored charge on the output transistor Q_2 is removed locally by R_3 rather than through diodes D_1 and D_2 onto the input signal lines. These transients are also reduced during switching by the offset transistor Q_1 which operates in the unsaturated mode. This technique eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.
4. The offset transistor Q_1 provides additional drive current to the output transistor Q_2 without requiring high input currents when the input is in the low state. High input currents would limit fan-out of the driving gates. The additional drive to the output transistor invites the use of a smaller base resistor R_3 and relaxes the h_{FE} requirement of the output transistor thus producing higher manufacturing yields.

In order to drive high-fan-out or high-capacity loads, a buffer is available which has a modified double-ended output. This output has a high-sink-current capability when in the ON state and a low-impedance emitter-follower output in the OFF state.

The master-slave flip-flops have AND gate inputs to the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure C):

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

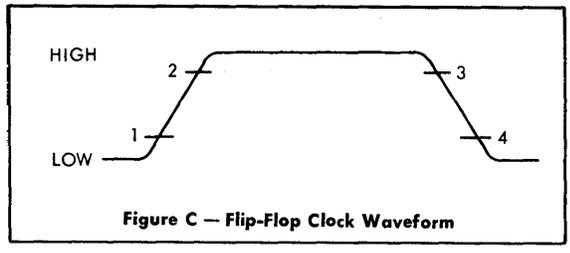


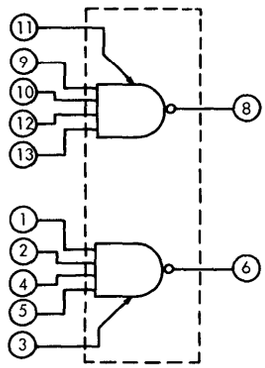
Figure C — Flip-Flop Clock Waveform

The pulse-triggered binary has two 70-pF capacitors in the clock line which provide an input-differentiating network for high-speed clocking applications.

standard line summary

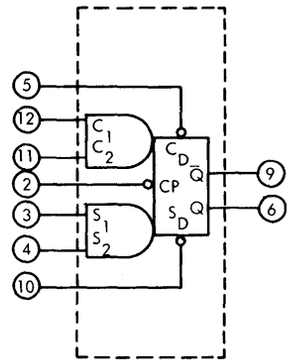
Input and output pin numbers are shown for reference. For all networks shown V_{CC} is pin (14) (unless otherwise noted) and GND is pin (7). See referenced page for complete pin configuration.

SN15 930 . . . . . See Page 3005
SN15 932 (Buffer) . . . . . See Page 3009
SN15 944 (Power Gate). . . . See Page 3012



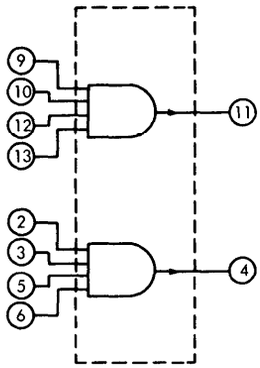
DUAL 4-INPUT NAND/NOR GATES

SN15 931 . . . . . See Page 3007
SN15 945 . . . . . See Page 3014
SN15 948 . . . . . See Page 3019



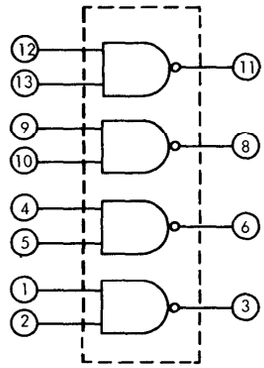
FLIP-FLOPS WITH SET AND CLEAR

SN15 933 . See Page 3011
(No V_{CC} Terminal)



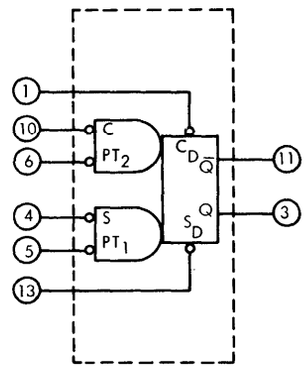
DUAL 4-INPUT EXPANDER

SN15 946 . See Page 3017



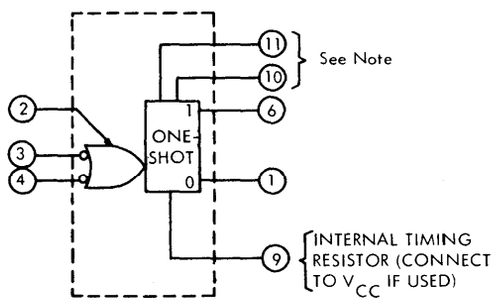
QUADRUPLE 2-INPUT NAND/NOR GATE

SN15 950 . See Page 3022



PULSE-TRIGGERED BINARY

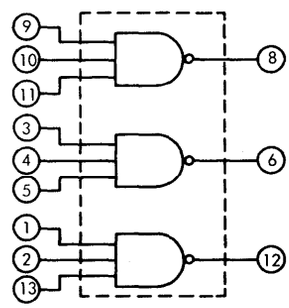
SN15 951 . . . . . See Page 3024



NOTE: External capacitance is added between pins (10) and (11). External resistance bypasses internal timing resistor if connected from (10) to V_{CC}.

MONOSTABLE MULTIVIBRATOR

SN15 962 . . . . See Page 3026



TRIPLE 3-INPUT NAND/NOR GATE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	+8 V
Continuous Output Sink Current (SN15 930, SN15 931, SN15 945, SN15 946, SN15 948, SN15 962)	30 mA
Continuous Output Sink Current (SN15 950, SN15 951)	50 mA
Continuous Output Sink Current (SN15 932, SN15 944)	150 mA
Current Out of Input Terminal	–10 mA
Current Into Input Terminal (except SN15 950 and SN15 951 pin (10))	1 mA
Current Into Input Terminal (SN15 950 and SN15 951 pin (10))	5 mA
Operating Free-Air Temperature Range (See Note 2)	–55°C to 125°C
Storage Temperature Range	–65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies for networks operating at V_{CC} = 5.5 V, all inputs† at 5.5 V, and the following output sink current:

SN15 930†, SN15 946, SN15 950, SN15 962	12 mA
SN15 931	10.6 mA
SN15 932†	36 mA
SN15 944†	40 mA
SN15 945	15.2 mA
SN15 948	13.6 mA
SN15 951	15 mA

†Expander modes open

logic definition

Series 15 930 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input current requirements

Weighted values of input current requirements reflect worst-case conditions for T_A = –55°C to 125°C and V_{CC} = 4.5 V to 5.5 V. Each gate input requires that no more than –1.6 mA flow out of the input at a logical 0 input voltage level; therefore, one input load is –1.6 mA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS

NETWORK	TYPE	INPUT	NUMBER OF LOADS
GATES AND EXPANDER	SN15 930, SN15 932, SN15 933, SN15 944, SN15 946, SN15 962	Each Input	1
FLIP-FLOPS	SN15 931	Each Input (Synchronous or Asynchronous)	⅔
		Clock	2
	SN15 945 and SN15 948	Synchronous Inputs	⅔
		Asynchronous and Clock Inputs	2
PULSE-TRIGGERED BINARY	SN15 950	Synchronous or Asynchronous	1½
MONOSTABLE MULTIVIBRATOR	SN15 951	Each Input	2

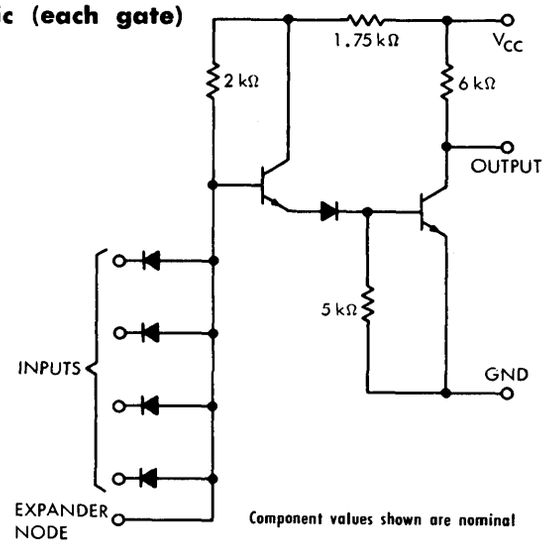
output drive capability

Weighted values of fan-out reflect the ability of an output to sink current (into the output terminal) under recommended operating conditions and are specified as positive values. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

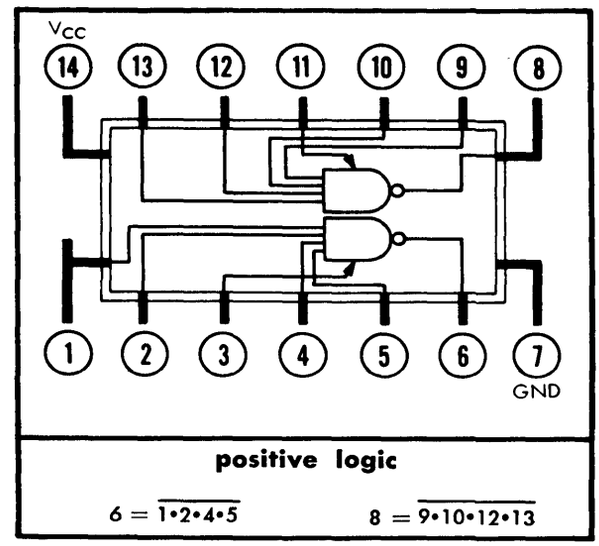
WEIGHTED VALUES OF FAN-OUT

NETWORK	TYPE	OUTPUT	LOADS
GATES	SN15 930, SN15 946, SN15 962	Each Output	8
BUFFER	SN15 932	Each Output	25
POWER GATE	SN15 944	Each Output	27
FLIP-FLOPS	SN15 931	Q or $\overline{Q}$	7
	SN15 945	Q or $\overline{Q}$	10
	SN15 948	Q or $\overline{Q}$	9
PULSE-TRIGGERED BINARY	SN15 950	Q or $\overline{Q}$	8
MONOSTABLE MULTIVIBRATOR	SN15 951	Each Output	10

schematic (each gate)



Component values shown are nominal



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 11.4 mA, T_A = −55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 10.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 V, V_{in} = 1.1 V, I_{load} = −0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_{in} = 1.4 V, I_{load} = −0.12 mA, T_A = −55°C	2.5		V
			V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = −0.12 mA, T_A = 125°C	2.5		V

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage at expander input node, $V_{in\,x}$	3	V_{CC} = 4.5 V, $V_{in\,x}$ = 1.8 V, I_{load} = −0.12 mA, T_A = 25°C	2.6		V
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 25°C and −55°C		− 1.6	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 125°C		− 1.5	mA
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 V, T_A = 25°C		50	μA
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 V, V_{out} = 0, T_A = 25°C	−0.6	−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = −55°C		−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = 125°C		−1.3	mA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 V, T_A = 25°C		6.5	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 V, T_A = 25°C		5.5	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$t_{pd(0)}$	Propogation delay time to logical 0 level	51	R_1 = 400 Ω, C_L = 50 pF	10	30	ns
$t_{pd(1)}$	Propogation delay time to logical 1 level		R_1 = 3.9 kΩ, C_L = 30 pF	25	80	ns

† Expander nodes are open unless otherwise noted.

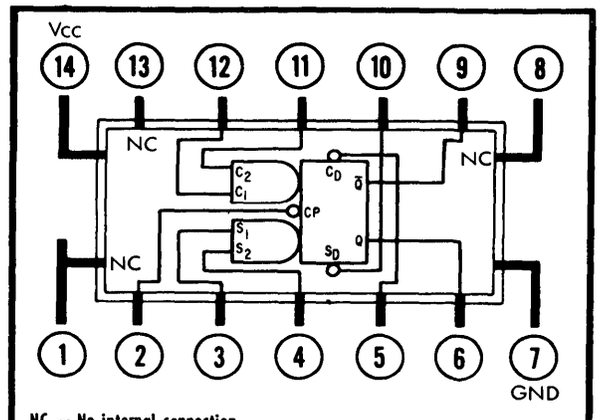
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 7

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	10	V_{CC} = 4.5 V, $V_{CP(S)}$ = 0.95 V, I_{sink} = 10.6 mA, T_A = 25°C	0.4	V
			V_{CC} = 4.5 V, $V_{CP(S)}$ = 1.1 V, I_{sink} = 10 mA, T_A = –55°C	0.4	V
			V_{CC} = 4.5 V, $V_{CP(S)}$ = 0.75 V, I_{sink} = 9.5 mA, T_A = 125°C	0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	11	V_{CC} = 4.5 V, V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6	V
			V_{CC} = 4.5 V, V_1 = 2.1 V, V_2 = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5	V
			V_{CC} = 4.5 V, V_1 = 1.7 V, V_2 = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_{CC} = 4.5 V, V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6	V
			V_{CC} = 4.5 V, V_1 = 2.1 V, V_2 = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5	V
			V_{CC} = 4.5 V, V_1 = 1.7 V, V_2 = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5	V
$I_{CP(0)}$	Logical 0 level clock-input forward current	13	V_{CC} = 5.5 V, V_{in} = 1.1 V, T_A = 25°C	–3.4	mA
			V_{CC} = 5.5 V, V_{in} = 1.4 V, T_A = –55°C	–3.4	mA
			V_{CC} = 5.5 V, V_{in} = 0.8 V, T_A = 125°C	–3	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	14	V_{CC} = 5.5 V, V_{CP} = 4 V, T_A = 25°C and –55°C	20	μA
			V_{CC} = 5.5 V, V_{CP} = 4 V, T_A = 125°C	30	μA

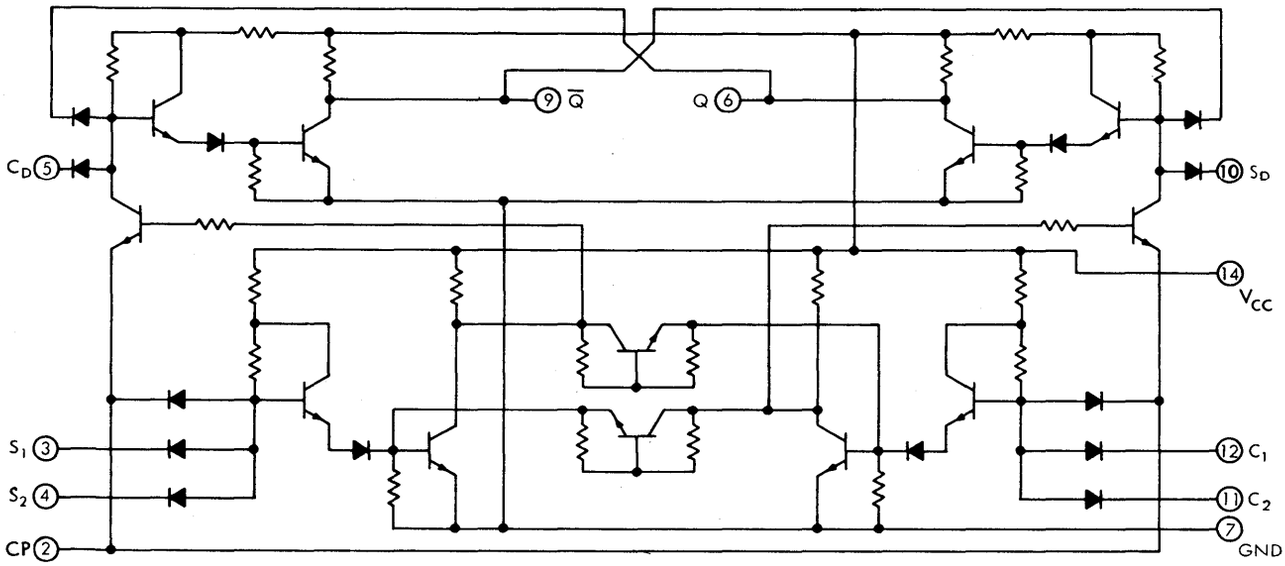
electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	16	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and −55°C		−1.07	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		−1	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	17	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	18	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and −55°C		−1.2	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		−1.1	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = 5 V, T_A = 25°C		11	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 V, T_A = 25°C		14.5	mA

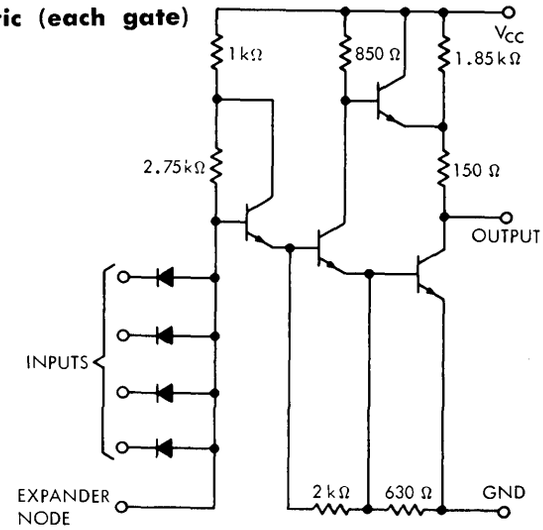
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	R_1 = 400 Ω, C_L = 50 pF	35	75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ, C_L = 30 pF	35	75	ns

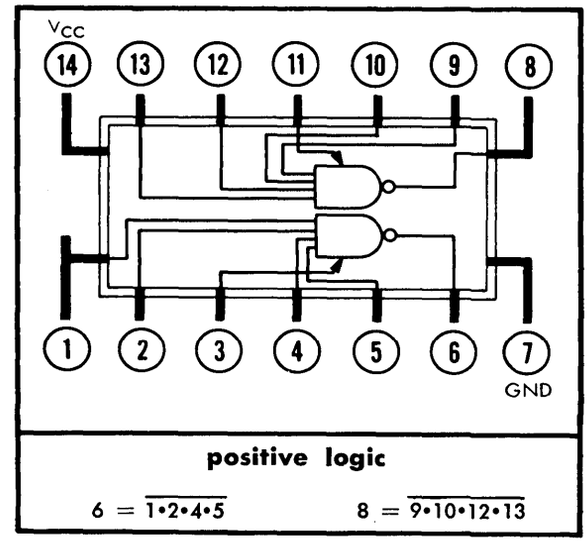
schematic



schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Fan-Out From Each Output 25

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 36 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 34 mA, T_A = −55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 32 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 V, V_{in} = 1.1 V, I_{load} = −2.5 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_{in} = 1.4 V, I_{load} = −2 mA, T_A = −55°C	2.5		V
			V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = −4 mA, T_A = 125°C	2.5		V

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

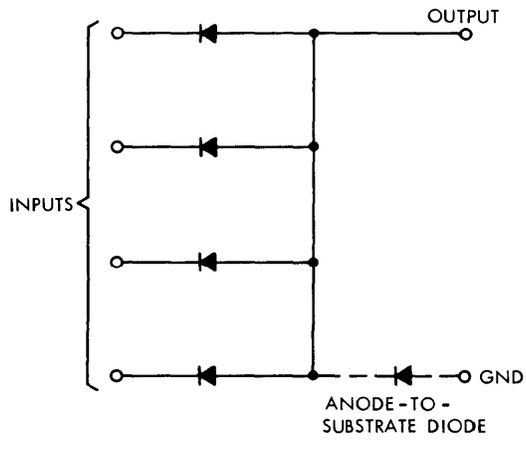
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage input at expander node, V_{inX}	3	V_{CC} = 4.5 V, V_{inX} = 1.8 V, I_{load} = −2.5 mA, T_A = 25°C	2.6		V
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 25°C and −55°C		−1.6	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 125°C		−1.5	mA
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 V, T_A = 25°C		50	μA
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 V, V_{out} = 0, T_A = 25°C	−18		mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = 125°C and −55°C	−16		mA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 V, T_A = 25°C		26.6	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 V, T_A = 25°C		6	mA

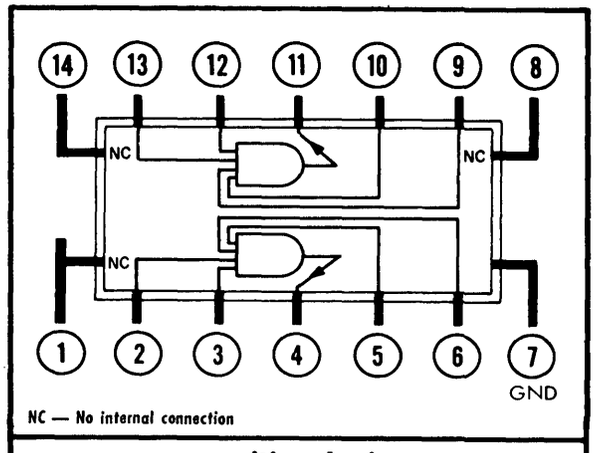
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	R_1 = 150 Ω, C_L = 500 pF	15	40	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 510 Ω, C_L = 500 pF	25	80	ns

† Expander nodes are open unless otherwise noted.

schematic (each expander)





positive logic

4 = 2•3•5•6 11 = 9•10•12•13

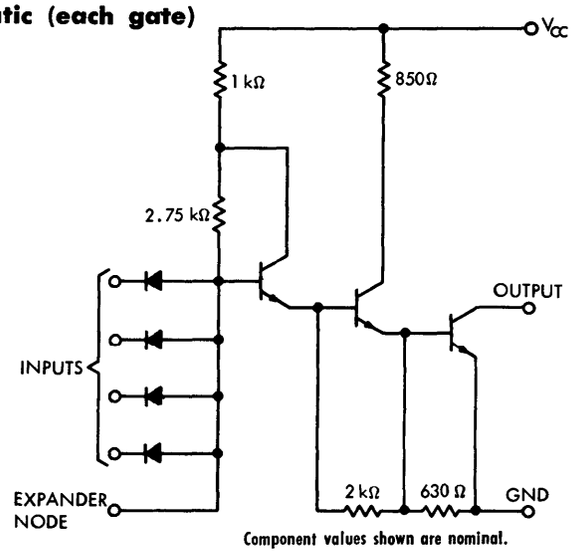
electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_F	Input diode forward voltage	21	I_{out} = 2 mA, T_A = 25°C	0.7	0.82	V
			I_{out} = 2 mA, T_A = –55°C	0.85	0.98	V
			I_{out} = 2 mA, T_A = 125°C	0.5	0.65	V
$I_{in\,R}$	Input diode reverse current	22	V_{in} = 4 V, T_A = 25°C		2	μA
			V_{in} = 4 V, T_A = –55°C		2	μA
			V_{in} = 4 V, T_A = 125°C		5	μA
$I_{out\,R}$	Anode-to-substrate reverse current	23	V_{out} = 4 V, T_A = 25°C and –55°C		10	μA
			V_{out} = 4 V, T_A = 125°C		25	μA

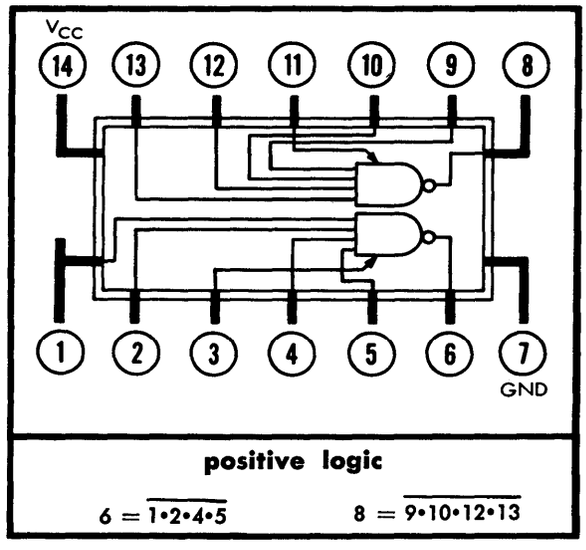
NOTE: A total of four expanders may be connected to an expandable gate to provide a fan-in of 20.

TYPE SN15 944
DUAL 4-INPUT NAND/NOR POWER GATE

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Fan-Out From Each Output 27

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 40 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 36 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 36 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	24	V_{CC} = 5.5 V, I_{sink} = 5 mA, T_A = 25°C	6		V
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current	5	$V_{CC} = 5.5\,V$, $V_{in} = 0$, $V_R = 4\,V$, $T_A = 25°C$ and $-55°C$		−1.6	mA
			$V_{CC} = 5.5\,V$, $V_{in} = 0$, $V_R = 4\,V$, $T_A = 125°C$		−1.5	mA
$I_{out(1)}$	Output reverse current (off level, worst-case voltage at any input)	25	$V_{CC} = 5.5\,V$, $V_{in} = 1.1\,V$, $V_{out} = 4.5\,V$, $T_A = 25°C$		100	μA
			$V_{CC} = 5.5\,V$, $V_{in} = 1.4\,V$, $V_{out} = 4.5\,V$, $T_A = -55°C$		50	μA
			$V_{CC} = 5.5\,V$, $V_{in} = 0.8\,V$, $V_{out} = 4.5\,V$, $T_A = 125°C$		200	μA
$I_{out(1)}$	Output reverse current (off level, worst-case voltage at expander input)	26	$V_{CC} = 5.5\,V$, $V_{in\,X} = 1.8\,V$, $V_{out} = 4.5\,V$, $T_A = 25°C$		100	μA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	$V_{CC} = 5\,V$, $T_A = 25°C$		20	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	$V_{CC} = 8\,V$, $T_A = 25°C$		6	mA

switching characteristics, $V_{CC} = 5\,V$, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 150\,\Omega$, $C_L = 100\,pF$	10	35	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 510\,\Omega$, $C_L = 20\,pF$	15	50	ns

† Expander nodes are open unless otherwise noted.

TYPE SN15 945
FLIP-FLOP WITH SET AND CLEAR

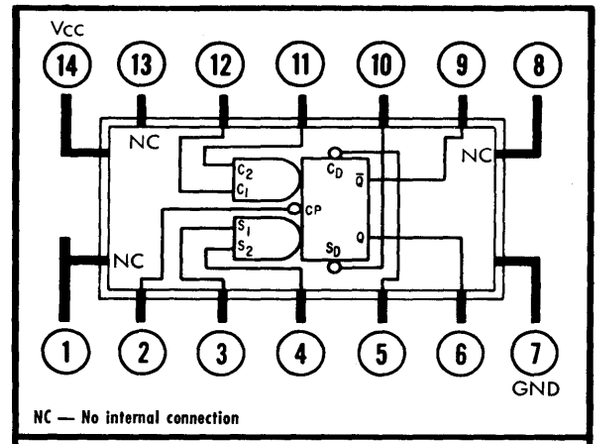
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 10

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	27 and 28	V_{CC} = 4.5 V, V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 4.5 V, I_{sink} = 15.2 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_1 = 1.4 V, V_2 = 2.1 V, V_3 = 4.5 V, I_{sink} = 14.6 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_1 = 0.8 V, V_2 = 1.7 V, V_3 = 4.5 V, I_{sink} = 13.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5		V
			V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	29	V_{CC} = 5.5 V, V_{in} = 1.1 V, V_{CP} = 0, T_A = 25°C		–3.2	mA
			V_{CC} = 5.5 V, V_{in} = 1.4 V, V_{CP} = 0, T_A = –55°C		–3.2	mA
			V_{CC} = 5.5 V, V_{in} = 0.8 V, V_{CP} = 0, T_A = 125°C		–2.8	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	30	V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25°C and –55°C		10	μA
			V_{CC} = 4 V, V_{CP} = 4 V, T_A = 125°C		20	μA

electrical characteristics (continued)

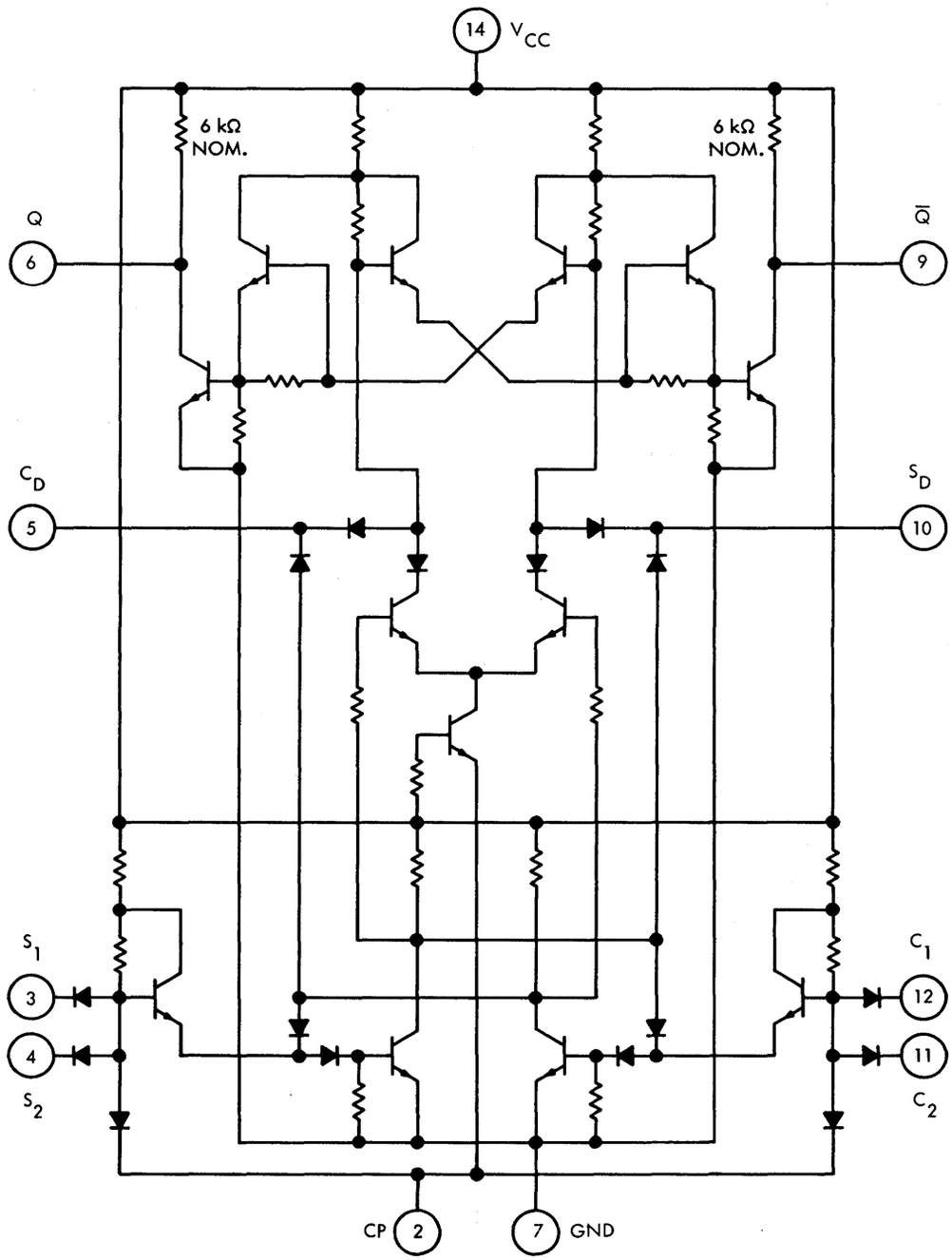
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	31	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 25°C and –55°C		–1.07	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 125°C		–1	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and –55°C		–2.4	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		–2.1	mA
I_{OS}	Short-circuit output current	18	V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 25°C and –55°C	–0.7	–1.33	mA
			V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 125°C	–0.625	–1.3	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = 5 V, T_A = 25°C		14	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 V, T_A = 25°C		16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	R_1 = 330 Ω, C_L = 50 pF		75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 2 kΩ, C_L = 30 pF		75	ns

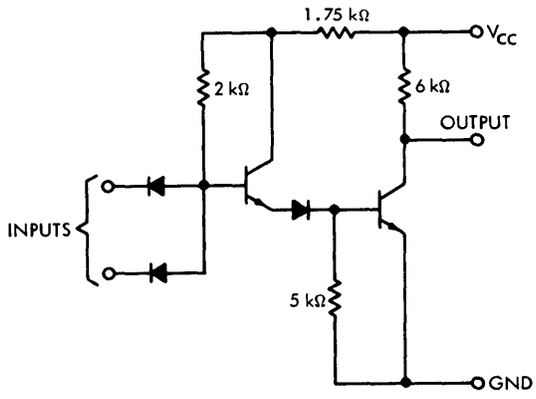
TYPE SN15 945
FLIP-FLOP WITH SET AND CLEAR

schematic

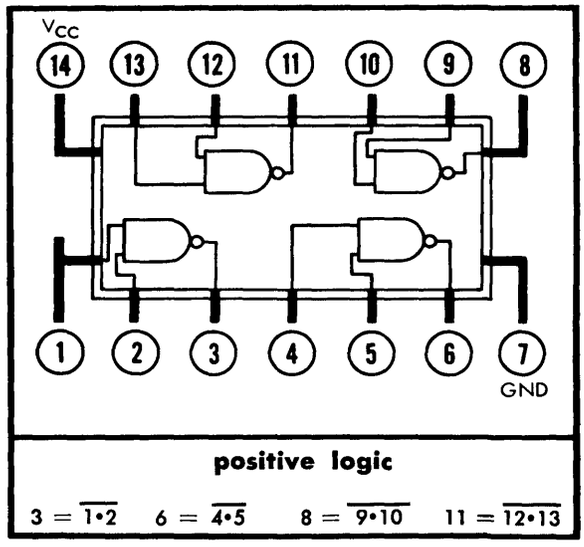


NOTE: Pins (1), (8), and (13) — no internal connection.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 11.4 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 10.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 V, V_{in} = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_{in} = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5		V
			V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5		V

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 25°C and −55°C		−1.6	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 125°C		−1.5	mA
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 V, T_A = 25°C		50	μA
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 V, V_{out} = 0, T_A = 25°C	−0.6	−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = −55°C		−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = 125°C		−1.3	mA
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	V_{CC} = 5 V, T_A = 25°C		13	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	V_{CC} = 8 V, T_A = 25°C		11	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	R_1 = 400 Ω, C_L = 50 pF	10	30	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ, C_L = 30 pF	25	80	ns

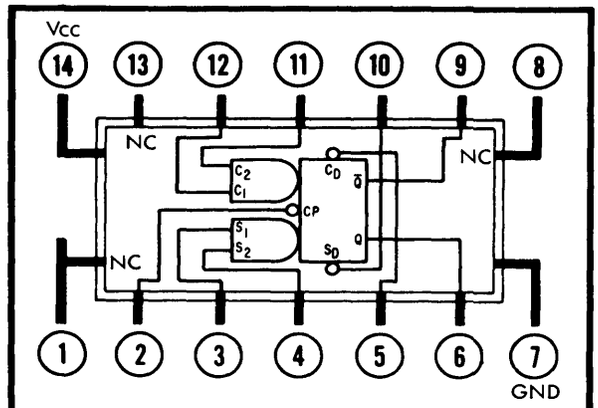
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 9

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	27 and 28	V_{CC} = 4.5 V, V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 4.5 V, I_{sink} = 13.6 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_1 = 1.4 V, V_2 = 2.1 V, V_3 = 4.5 V, I_{sink} = 13 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_1 = 0.8 V, V_2 = 1.7 V, V_3 = 4.5 V, I_{sink} = 12.3 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5		V
			V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	29	V_{CC} = 5.5 V, V_{in} = 1.1 V, V_{CP} = 0, T_A = 25°C		–2.56	mA
			V_{CC} = 5.5 V, V_{in} = 1.4 V, V_{CP} = 0, T_A = –55°C		–2.56	mA
			V_{CC} = 5.5 V, V_{in} = 0.8 V, V_{CP} = 0, T_A = 125°C		–2.2	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	30	V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25°C and –55°C		10	μA
			V_{CC} = 4 V, V_{CP} = 4 V, T_A = 125°C		20	μA

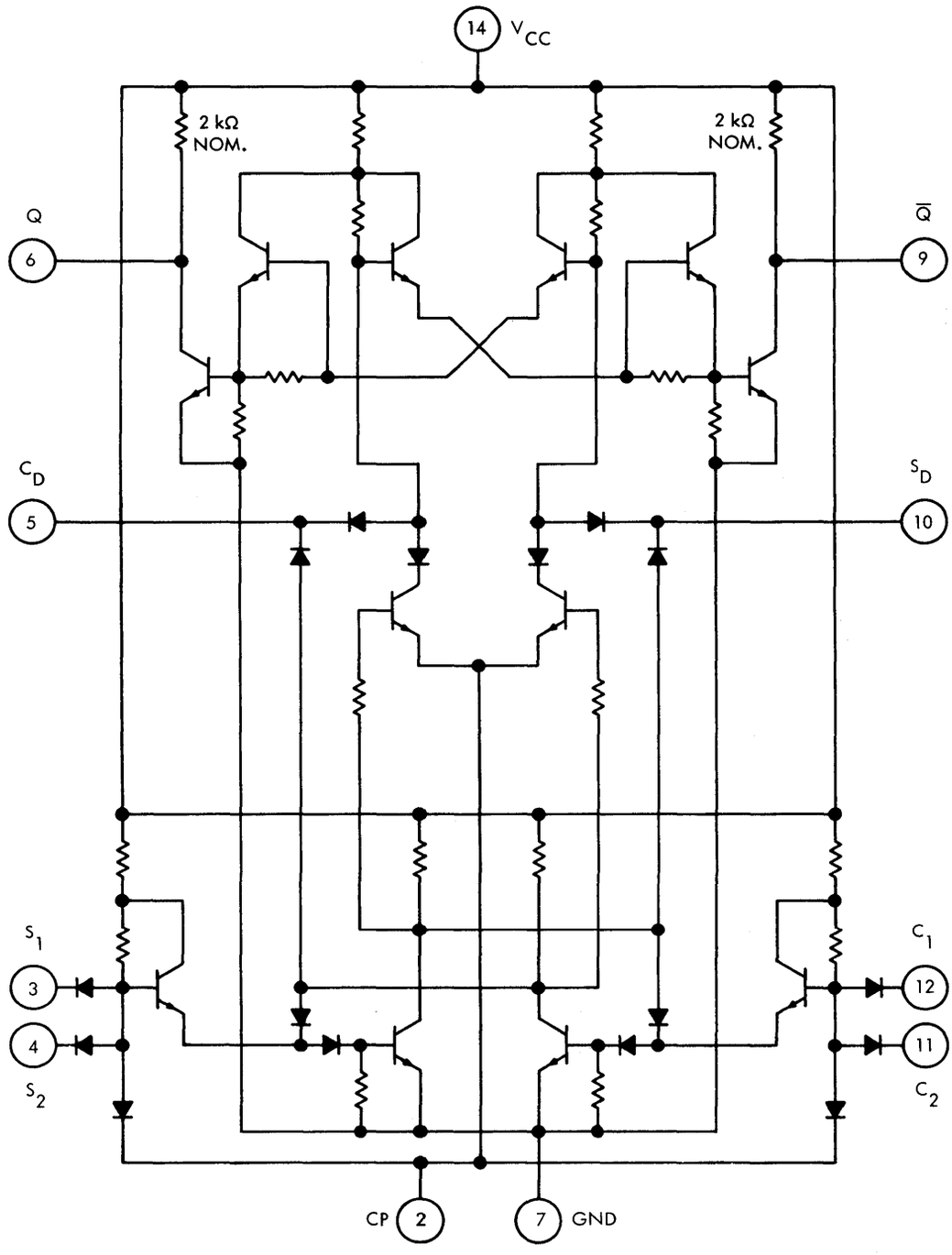
electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	31	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 25°C and –55°C		–1.07	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 125°C		–1	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and –55°C		–2.4	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		–2.1	mA
I_{OS}	Short-circuit output current	18	V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 25°C and –55°C	–2.1	–3.96	mA
			V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 125°C		–3.54	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = 5 V, T_A = 25°C		16.2	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 V, T_A = 25°C		16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	R_1 = 330 Ω, C_L = 50 pF	5	65	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 2 kΩ, C_L = 30 pF	5	75	ns

schematic



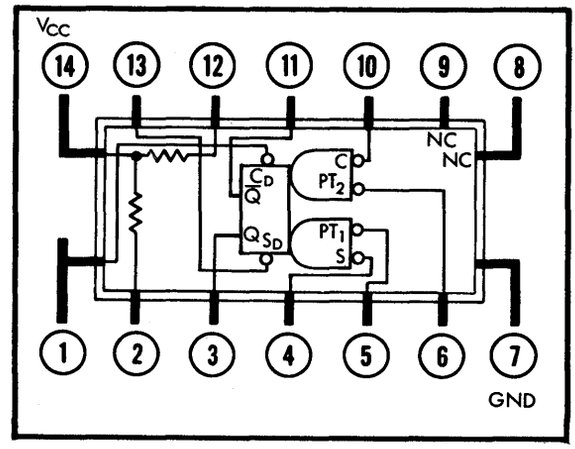
NOTE: Pins (1) (8) and (13) no internal connection.

logic

TRUTH TABLES

SYNCHRONOUS					
t_n PULSE INPUT				t_{n+1} OUTPUT	
S	C	PT_1	PT_2	Q	$\overline{Q}$
1	X	X	1	Qn	$\overline{Q}$n
X	1	1	X	Qn	$\overline{Q}$n
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S_D	C_D	Q	$\overline{Q}$
1	1	Qn	$\overline{Q}$n
0	1	0	1
1	0	1	0
0	0	1	1



NOTES:

1. X indicates that either a logical 1 or a logical 0 may be present.
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT_1 and PT_2 indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	34	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 11.4 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 10.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	35	V_{CC} = 4.5 V, V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 4.5 V, I_{load} = –1.5 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_1 = 1.4 V, V_2 = 2.1 V, V_3 = 4.5 V, I_{load} = –1.5 mA, T_A = –55°C	2.5		V
			V_{CC} = 4.5 V, V_1 = 0.8 V, V_2 = 1.7 V, V_3 = 4.5 V, I_{load} = –1.5 mA, T_A = 125°C	2.5		V
$I_{in\,PT}$	Pulse-triggered-input current	36	V_{CC} = 5.5 V, V_{in} = 8 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 8 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current at C or S	37	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and –55°C		–2.4	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		–2.25	mA
$I_{in(0)}$	Logical 0 level input current at C_D or S_D	37	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and –55°C		–1.82	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		–1.62	mA

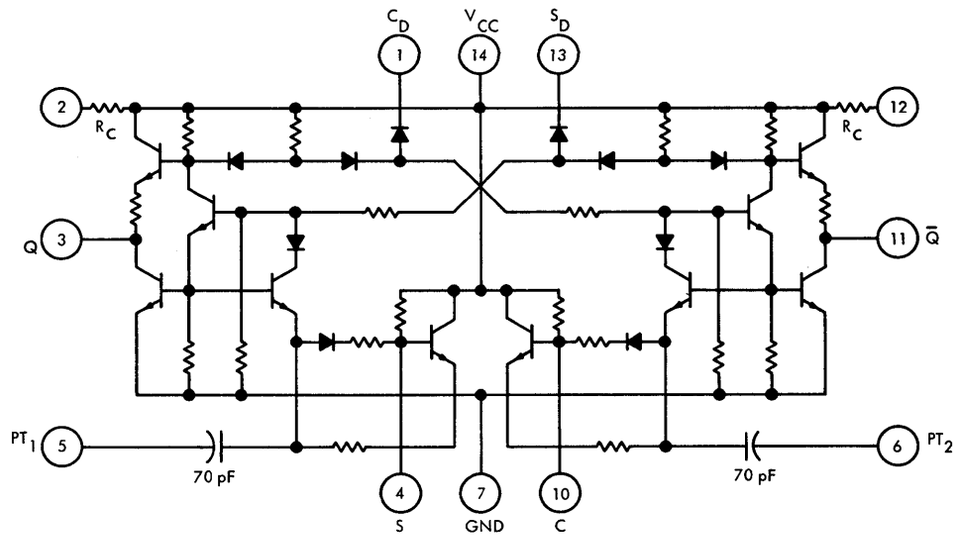
electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current at C_D or S_D	38	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
I_{RC}	Current through resistor R_C	39	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C	−4.22	−7.35	mA
I_{OS}	Short-circuit output current	40	V_{CC} = 5.5 V, V_{out} = 0, T_A = 25°C and −55°C	−15.7	−27	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = 125°C	−14.6	−26	mA
$I_{out(1)}$	Output reverse current (off level)	40	V_{CC} = 4.5 V, V_{out} = 4.5 V, T_A = 25°C		50	μA
$I_{CC(0)}$	Logical 0 level supply current	41	V_{CC} = 5 V, T_A = 25°C		8.7	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	42	V_{CC} = 8 V, T_A = 25°C		18.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	53	R_1 = 400 Ω, C_1 = 100 pF	5	32	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 3.9 kΩ, C_1 = 100 pF	5	25	ns

schematic



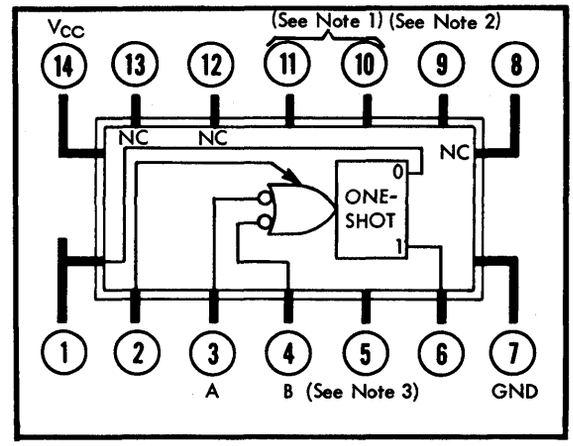
TYPE SN15 951
MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE

t_n INPUT		t_{n+1} INPUT		OUTPUT
A	B	A	B	
1	1	1	1	INHIBIT
1	1	1	0	ONE-SHOT
1	1	0	1	ONE-SHOT
1	1	0	0	ONE-SHOT
0	1	X	X	INHIBIT
1	0	X	X	INHIBIT
0	0	X	X	INHIBIT

NOTES: a. t_n = time before input transition.
b. t_{n+1} = time after input transition.
c. X indicates that either a logical 1 or a logical 0 may be present.



NOTES: 1. External resistor and capacitor may be used between pins (10), (11), and (14) to control one-shot pulse width.
2. To use the internal timing resistor, connect pin (9) to pin (14).
3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 10
Input Pulse Characteristics:
Minimum Negative-Going Transition . . . . . 1 V
Maximum Input Fall Time Per Volt . . . . . 25 ns/V
Maximum Duty Cycle 40%

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	43	V_{CC} = 4.5 V, I_{sink} = 15 mA, T_A = 25°C and –55°C		0.4	V
			V_{CC} = 4.5 V, I_{sink} = 14 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	44	V_{CC} = 4.5 V, I_{load} = –0.18 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, I_{load} = –0.18 mA, T_A = 125°C and –55°C	2.5		V
$I_{in(1)}$	Logical 1 level input current	45	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and –55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current	46	V_{CC} = 5.5 V, V_1 = 4 V, V_2 = 0, T_A = 25°C and –55°C	–1.6	–3.1	mA
			V_{CC} = 5.5 V, V_1 = 4 V, V_2 = 0, T_A = 125°C	–1.4	–3	mA

†Expander node is open unless otherwise noted.

electrical characteristics (continued)

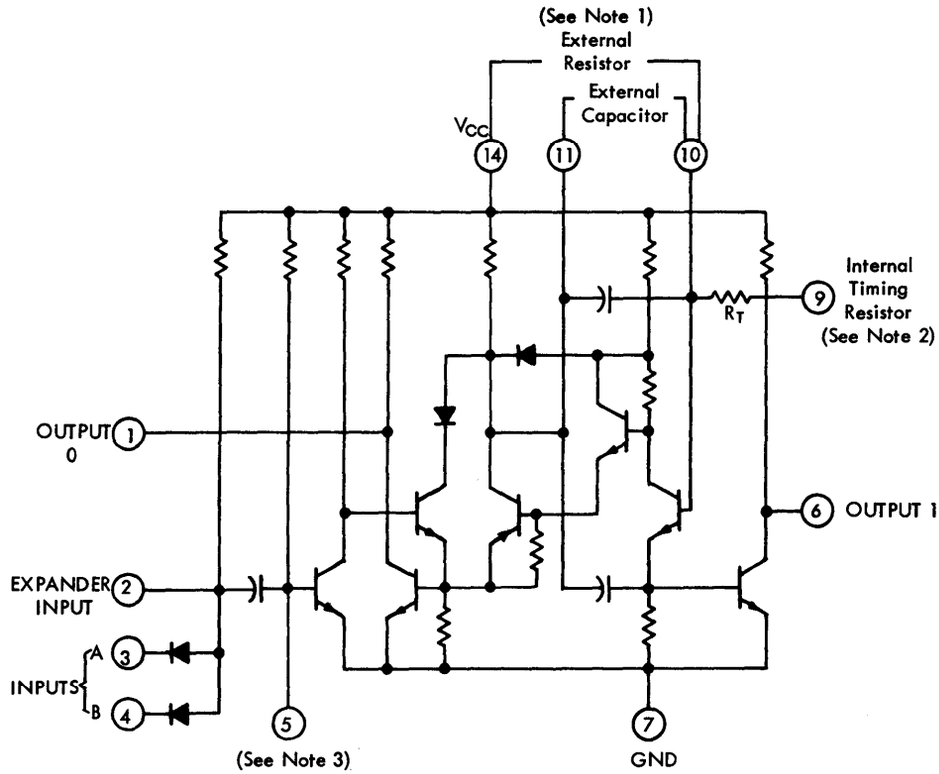
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
I_{RT}	Current through internal timing resistor R_T	47	$V_{CC} = 5.5$ V, $V_{in} = 5.5$ V, $T_A = 25°C$	0.5	0.75	mA
I_{SC}	Short-circuit current at expander node or pin (11)	48	$V_{CC} = 5.5$ V, $V_{in} = 0$, $T_A = 25°C$ and $-55°C$	−0.8		mA
			$V_{CC} = 5.5$ V, $V_{in} = 0$, $T_A = 125°C$	−0.75		mA
I_{CC}	Supply current	49	$V_{CC} = 5$ V, $T_A = 25°C$		9	mA
$I_{CC(max)}$	Supply current at maximum V_{CC}	50	$V_{CC} = 8$ V, $T_A = 25°C$		20	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	54	$R_1 = 300\,\Omega$, $C_L = 50$ pF		50	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level				50	ns
t_p	Pulse width			90	160	ns

†Expander node is open unless otherwise noted.

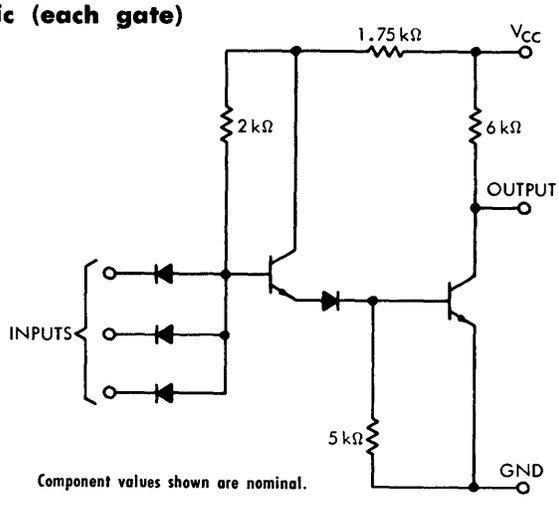
schematic



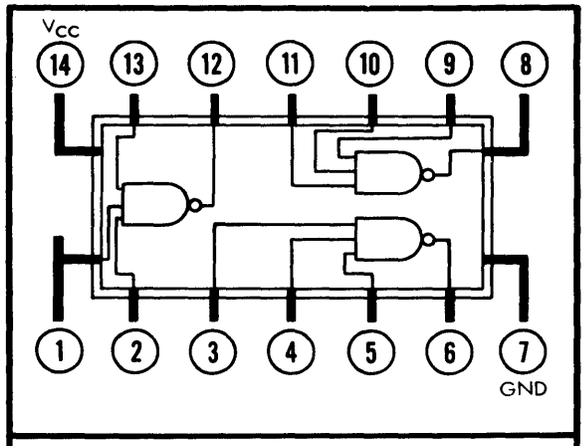
NOTES: 1. External resistor and capacitor may be used (as indicated above) between pins (10), (11), and (14) to control one-shot pulse width.
2. To use the internal timing resistor, connect pin (9) to pin (14).
3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

TYPE SN15 962
TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{3 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 11}$ $\quad 12 = \overline{1 \cdot 2 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 11.4 mA, T_A = –55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 10.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 V, V_{in} = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_{in} = 1.4 V, I_{load} = –0.12 mA, T_A = –55°C	2.5		V
			V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = –0.12 mA, T_A = 125°C	2.5		V

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	$V_{CC} = 5.5$ V, $V_{in} = 4$ V, $T_A = 25°C$ and $-55°C$		2	μA
			$V_{CC} = 5.5$ V, $V_{in} = 4$ V, $T_A = 125°C$		5	μA
$I_{in(0)}$	Logical 0 level input current	5	$V_{CC} = 5.5$ V, $V_{in} = 0$, $V_R = 4$ V, $T_A = 25°C$ and $-55°C$		−1.6	mA
			$V_{CC} = 5.5$ V, $V_{in} = 0$, $V_R = 4$ V, $T_A = 125°C$		−1.5	mA
$I_{out(1)}$	Output reverse current (off level)	6	$V_{CC} = V_{out} = 4.5$ V, $T_A = 25°C$		50	μA
I_{OS}	Short-circuit output current	7	$V_{CC} = 5.5$ V, $V_{out} = 0$, $T_A = 25°C$	−0.6	−1.34	mA
			$V_{CC} = 5.5$ V, $V_{out} = 0$, $T_A = -55°C$		−1.34	mA
			$V_{CC} = 5.5$ V, $V_{out} = 0$, $T_A = 125°C$		−1.3	mA
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	$V_{CC} = 5$ V, $T_A = 25°C$		9.75	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	$V_{CC} = 8$ V, $T_A = 25°C$		8.25	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$, $C_L = 50$ pF	10	30	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 3.9$ kΩ, $C_L = 30$ pF	25	80	ns

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

SN15 930, SN15 932, SN15 944, SN15 946, and SN15 962

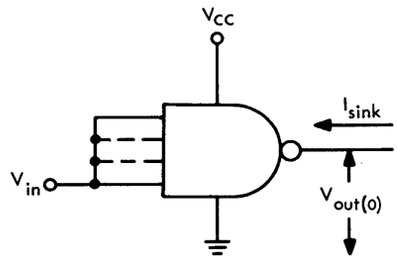
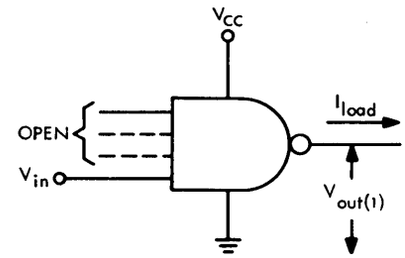


FIGURE 1 — $V_{out(0)}$

SN15 930, SN15 932, SN15 946, and SN15 962



1. Each input is tested separately.

FIGURE 2 — $V_{out(1)}$

SN15 930 and SN15 932

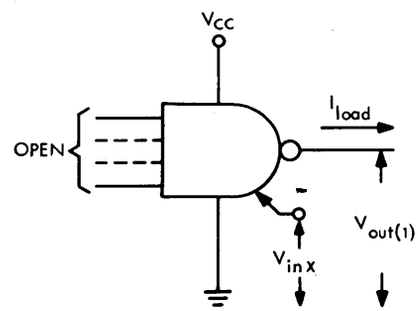
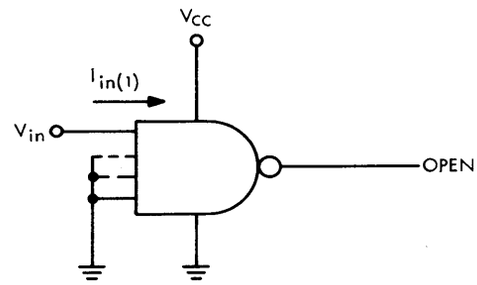


FIGURE 3 — $V_{out(1)}$

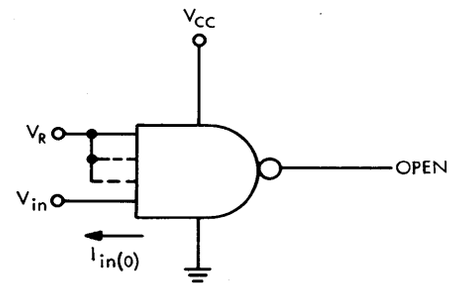
SN15 930, SN15 932, SN15 944, SN15 946, and SN15 962



1. Each input is tested separately.

FIGURE 4 — $I_{in(1)}$

SN15 930, SN15 932, SN15 944, SN15 946, and SN15 962



1. Each input is tested separately.

FIGURE 5 — $I_{in(0)}$

SN15 930, SN15 932, SN15 946, and SN15 962

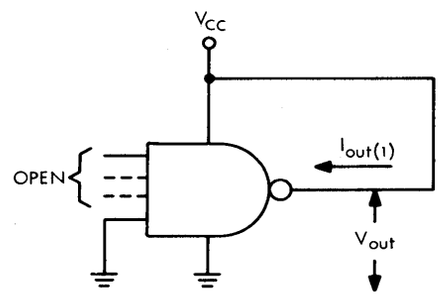


FIGURE 6 — $I_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 930, SN15 932, SN15 946, and SN15 962

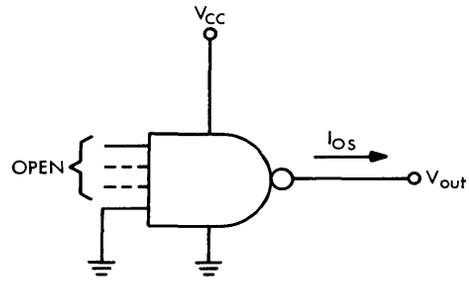


FIGURE 7 — I_{OS}

SN15 930, SN15 932, SN15 944, SN15 946, and SN15 962

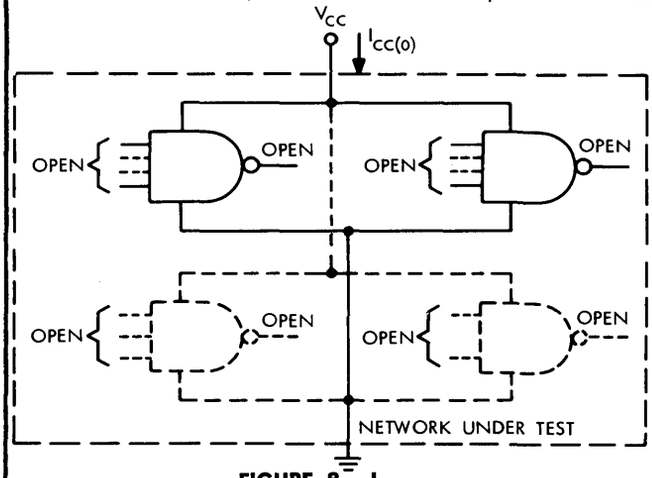


FIGURE 8 — $I_{CC(0)}$

SN15 930, SN15 932, SN15 944, SN15 946, and SN15 962

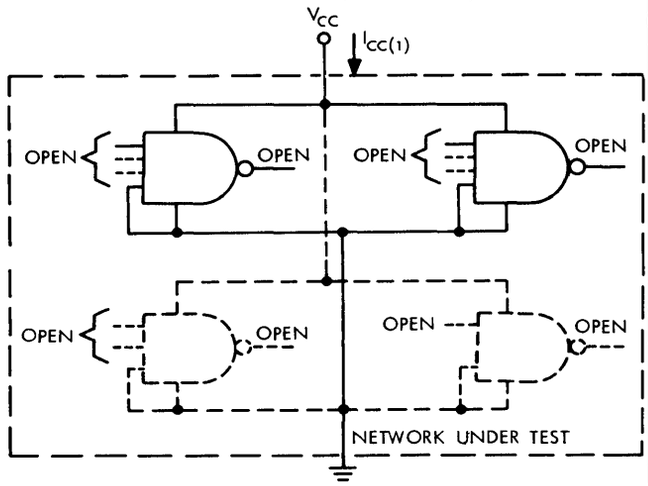
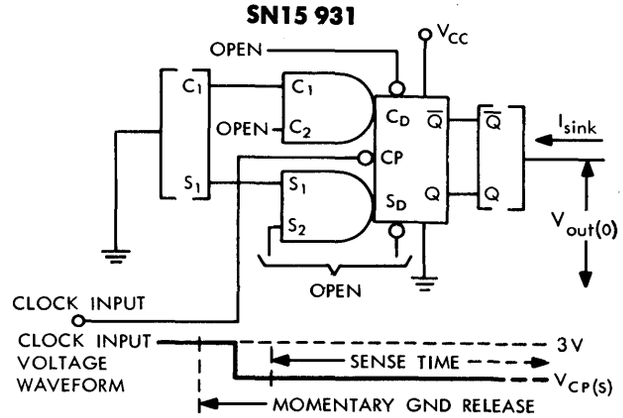


FIGURE 9 — $I_{CC(1)}$

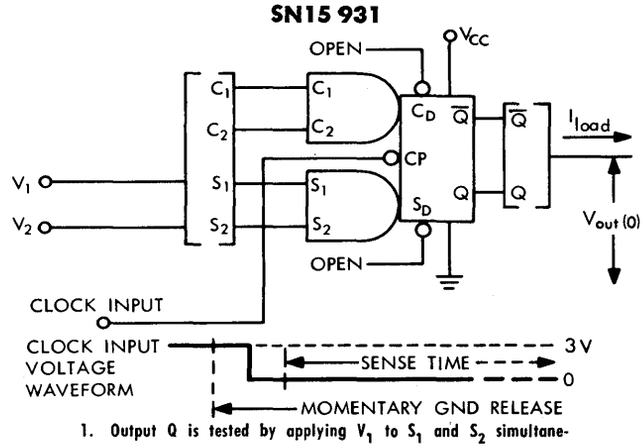
SN15 931



1. Output Q is tested by grounding S_1 and applying a momentary ground to $\overline{Q}$. I_{sink} is driven into Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and applying a momentary ground to Q. I_{sink} is driven into $\overline{Q}$.

FIGURE 10 — $V_{out(0)}$

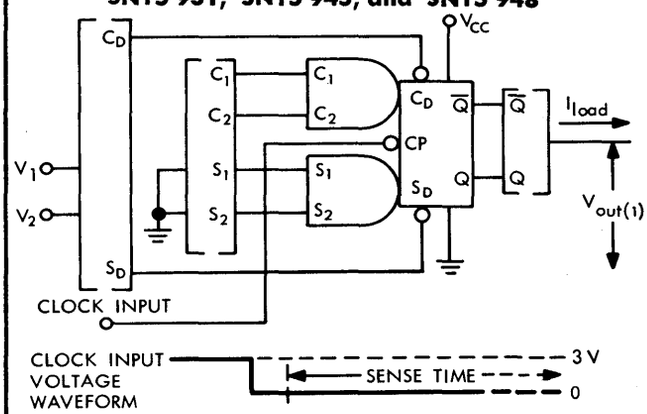
SN15 931



1. Output Q is tested by applying V_1 to S_1 and S_2 simultaneously, applying V_2 to C_1 and C_2 individually, and loading Q.
2. Output $\overline{Q}$ is tested by applying V_1 to C_1 and C_2 simultaneously, applying V_2 to S_1 and S_2 individually, and loading $\overline{Q}$.
3. Momentary ground is applied to output being tested.

FIGURE 11 — $V_{out(1)}$

SN15 931, SN15 945, and SN15 948



1. Output Q is tested by grounding S_1 and S_2, applying V_1 to C_D and V_2 to S_D, and loading Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and C_2, applying V_1 to S_D and V_2 to C_D, and loading $\overline{Q}$.

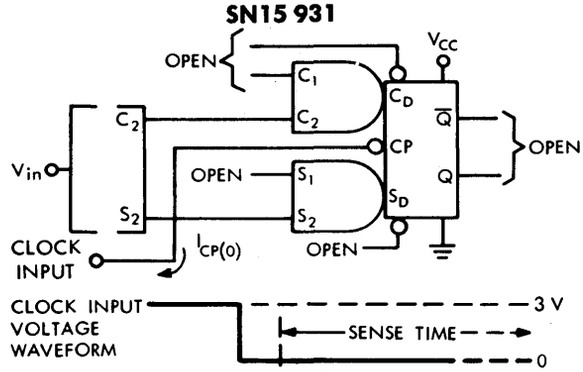
FIGURE 12 — $V_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 931



1. V_{in} is applied to each input separately.

FIGURE 13 — $I_{CP(0)}$

SN15 931

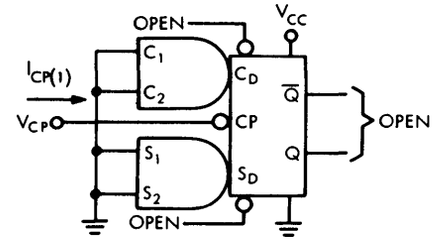
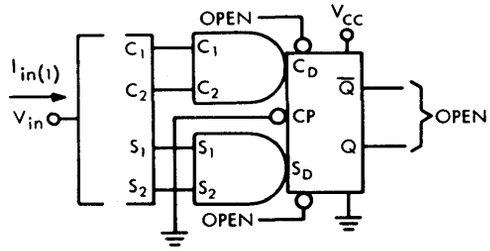


FIGURE 14 — $I_{CP(1)}$

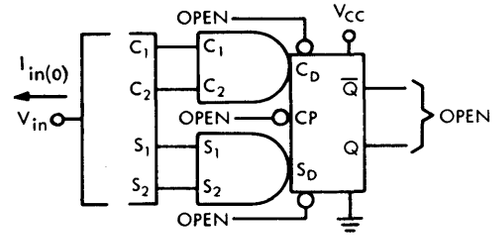
SN15 931, SN15 945 and SN15 948



1. V_{in} is applied to each input separately.

FIGURE 15 — $I_{in(1)}$

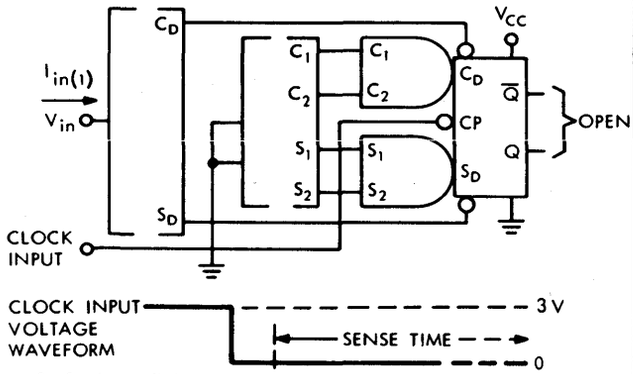
SN15 931



1. V_{in} is applied to each input separately.

FIGURE 16 — $I_{in(0)}$

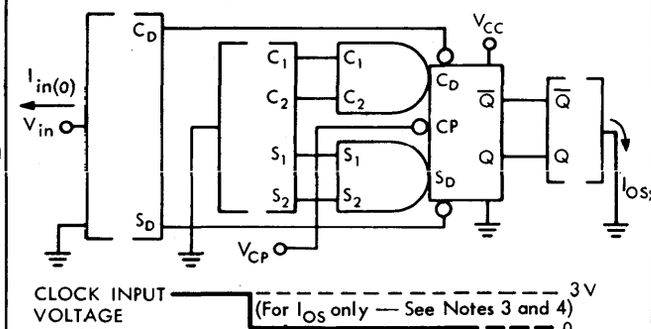
SN15 931



1. C_D input diode is tested by grounding S_1 and S_2 and applying V_{in} to C_D.
2. S_D input diode is tested by grounding C_1 and C_2 and applying V_{in} to S_D.

FIGURE 17 — $I_{in(1)}$

SN15 931 ($I_{in(0)}$) SN15 945 and SN15 948 (I_{OS})



1. Logical 0 level input current at C_D is tested with S_D, S_2, and $\overline{Q}$ grounded and CP open.
2. Logical 0 level input current at S_D is tested with C_D, C_2, and Q grounded and CP open.
3. Short-circuit output current at Q is tested by applying V_{in} to C_D and S_D, grounding C_1 and C_2, and applying clock input.
4. Short-circuit output current at $\overline{Q}$ is tested by applying V_{in} to C_D and S_D, grounding S_1 and S_2 and applying clock input.

FIGURE 18 — $I_{in(0)}$ and I_{OS}

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 931, SN15 945 and SN15 948

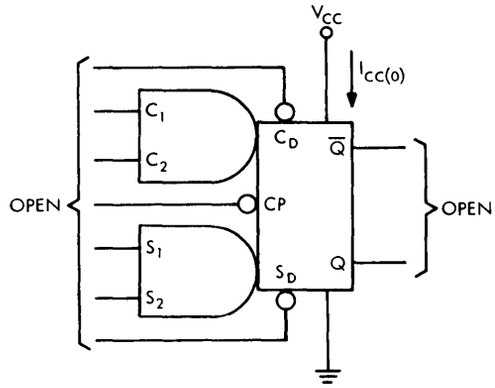


FIGURE 19 — $I_{CC(0)}$

SN15 931, SN15 945 and SN15 948

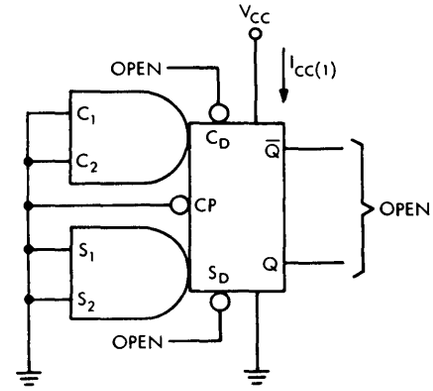
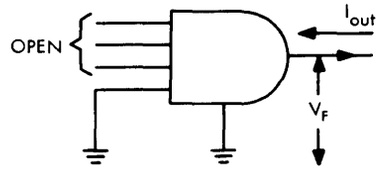


FIGURE 20 — $I_{CC(1)}$

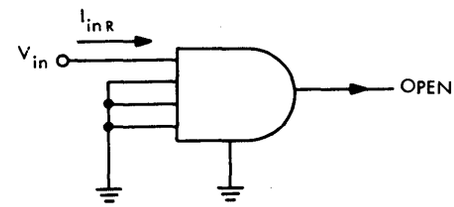
SN15 933



1. Each input is tested separately.

FIGURE 21 — V_F

SN15 933



1. Each input is tested separately.

FIGURE 22 — $I_{in\,R}$

SN15 933

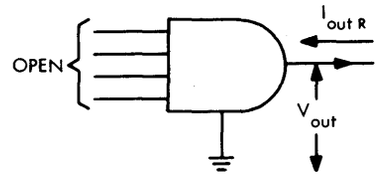


FIGURE 23 — $I_{out\,R}$

SN15 944

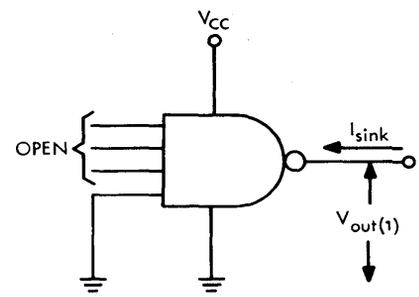


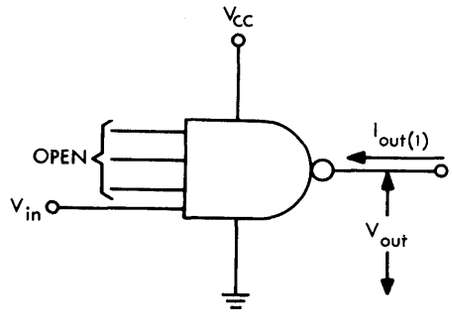
FIGURE 24 — $V_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

SN15 944



1. Each input is tested separately.

FIGURE 25 — $I_{out(1)}$

SN15 944

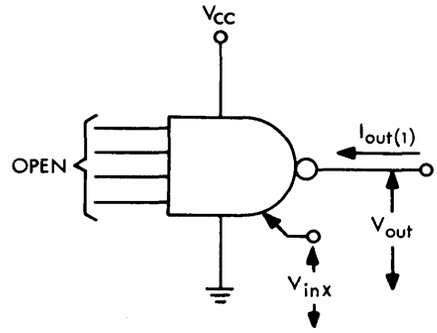
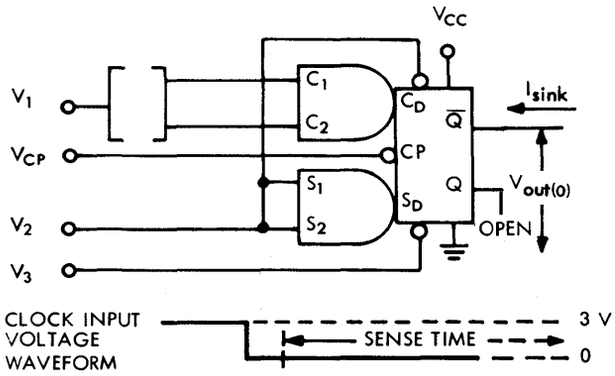


FIGURE 26 — $I_{out(1)}$

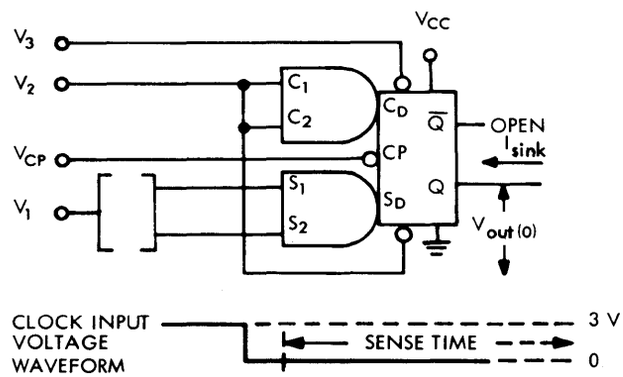
SN15 945 and SN15 948



1. Inputs C_1 and C_2 are tested separately.

FIGURE 27 — $V_{out(0)}$

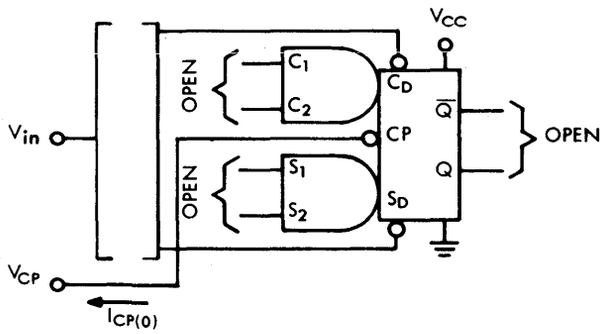
SN15 945 and SN15 948



1. Inputs S_1 and S_2 are tested separately.

FIGURE 28 — $V_{out(0)}$

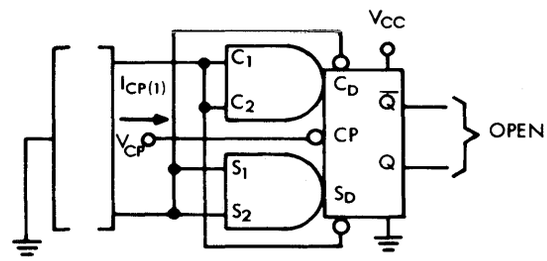
SN15 945 and SN15 948



1. V_{in} is applied to S_D or C_D separately.

FIGURE 29 — $I_{CP(0)}$

SN15 945 and SN15 948



1. Ground is applied separately to C_1,C_2 and S_D or to S_1,S_2 and C_D.

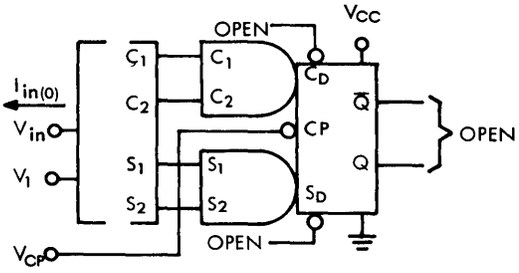
FIGURE 30 — $I_{CP(1)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

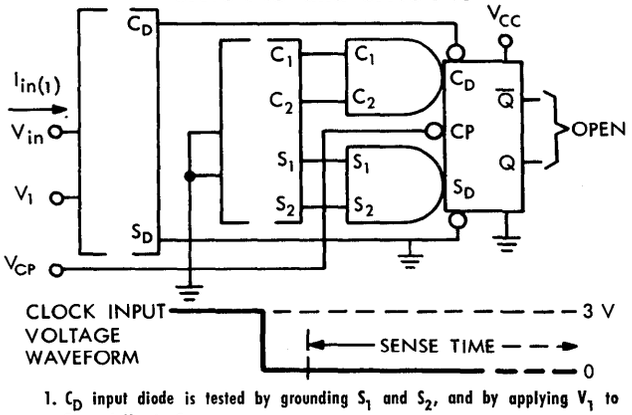
SN15 945 and SN15 948



1. Each synchronous input is tested separately by applying V_{in} to input under test and V_1 to the remaining gate input.

FIGURE 31 — $I_{in(0)}$

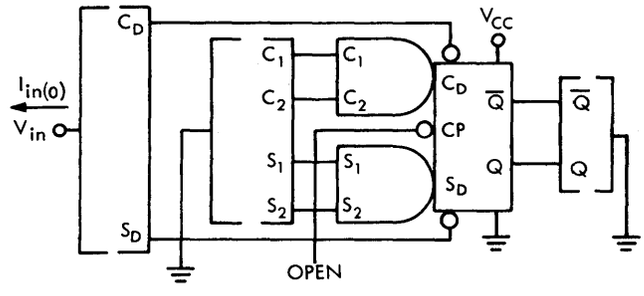
SN15 945 and SN15 948



1. C_D input diode is tested by grounding S_1 and S_2, and by applying V_1 to S_D and V_{in} to C_D.
2. S_D input diode is tested by grounding C_1 and C_2, and by applying V_1 to C_D and V_{in} to S_D.

FIGURE 32 — $I_{in(1)}$

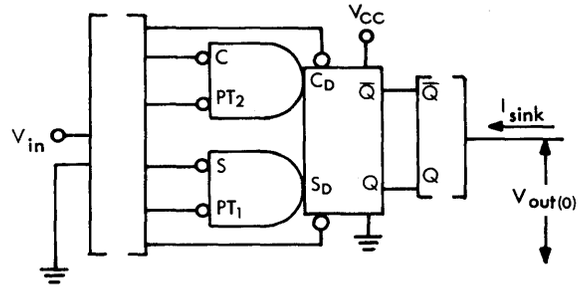
SN15 945 and SN15 948



1. C_D is tested with S_1 and S_2 grounded.
2. S_D is tested with C_1 and C_2 grounded.

FIGURE 33 — $I_{in(0)}$

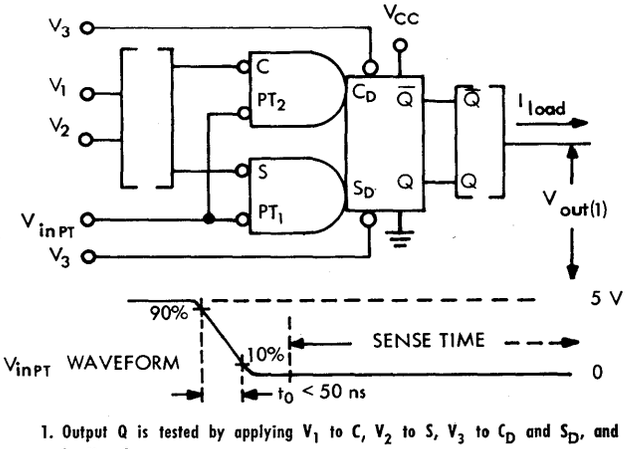
SN15 950



1. Output Q is tested by grounding C and C_D, applying V_{in} to S_D, and loading Q.
2. Output $\overline{Q}$ is tested by grounding S and S_D, applying V_{in} to C_D, and loading $\overline{Q}$.

FIGURE 34 — $V_{out(0)}$

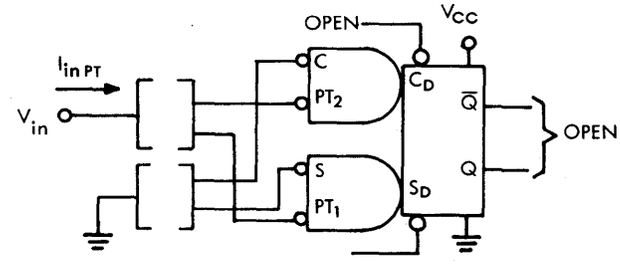
SN15 950



1. Output Q is tested by applying V_1 to C, V_2 to S, V_3 to C_D and S_D, and loading Q.
2. Output $\overline{Q}$ is tested by applying V_1 to S, V_2 to C, V_3 to C_D and S_D, and loading $\overline{Q}$.

FIGURE 35 — $V_{out(1)}$

SN15 950



1. Input PT_1 is tested by grounding S and applying V_{in} to PT_1.
2. Input PT_2 is tested by grounding C and applying V_{in} to PT_2.

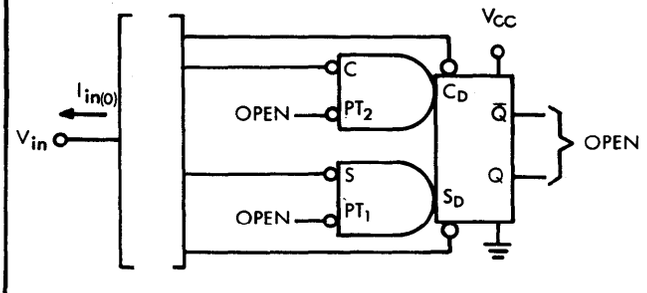
FIGURE 36 — $I_{in\,PT}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

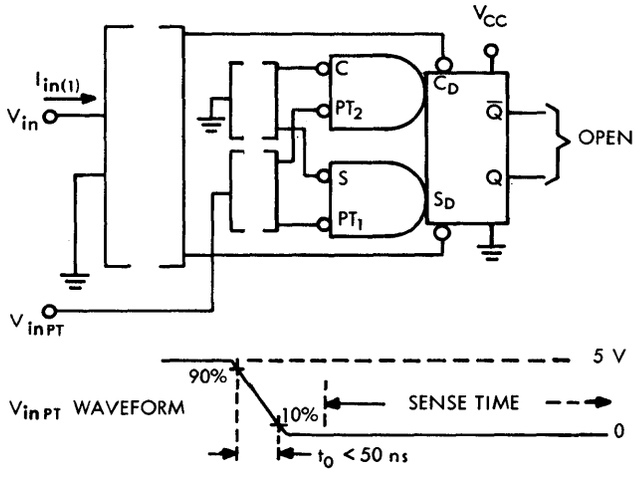
SN15 950



1. Each input is tested separately with all other inputs open-circuited.

FIGURE 37 — $I_{in(0)}$

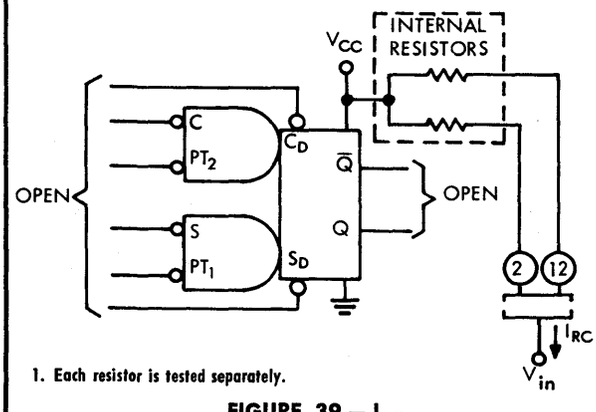
SN15 950



1. Each asynchronous input is tested separately.
2. When testing C_D ground S and apply V_{inPT} to PT_2.
3. When testing S_D ground C and apply V_{inPT} to PT_1.

FIGURE 38 — $I_{in(1)}$

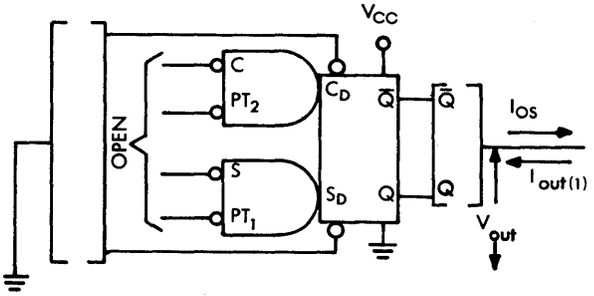
SN15 950



1. Each resistor is tested separately.

FIGURE 39 — I_{RC}

SN15 950



1. When testing output Q ground S_D.
2. When testing output $\overline{Q}$ ground C_D.

FIGURE 40 — I_{OS} and $I_{out(1)}$

SN15 950

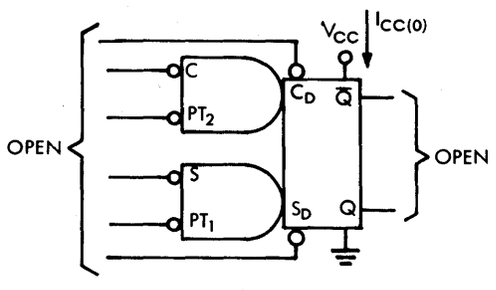


FIGURE 41 — $I_{CC(0)}$

SN15 950

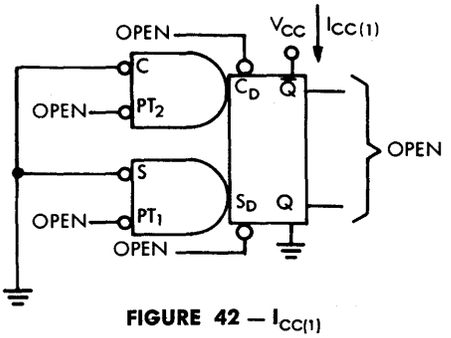


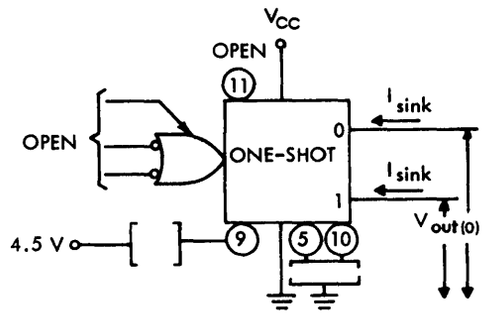
FIGURE 42 — $I_{CC(1)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

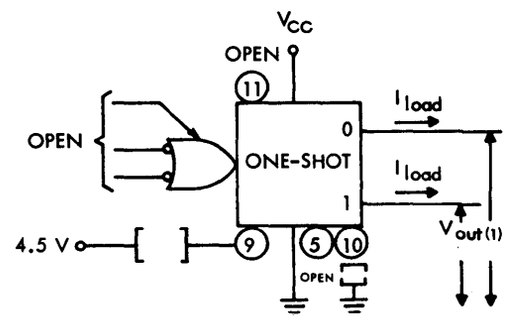
SN15 951



1. Output 0 is tested by applying ground separately to pins (5) and (10) and loading output 0.
2. Output 1 is tested by applying 4.5 V to pin (9) and loading output 1.

FIGURE 43 — $V_{out(0)}$

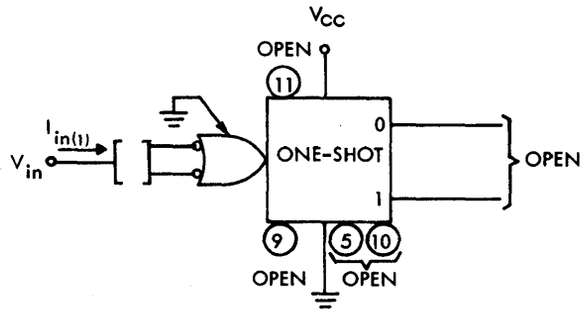
SN15 951



1. Output 0 is tested by applying 4.5 V to pin (9) and loading output 0.
2. Output 1 is tested by applying ground to pin (10) and loading output 1.

FIGURE 44 — $V_{out(1)}$

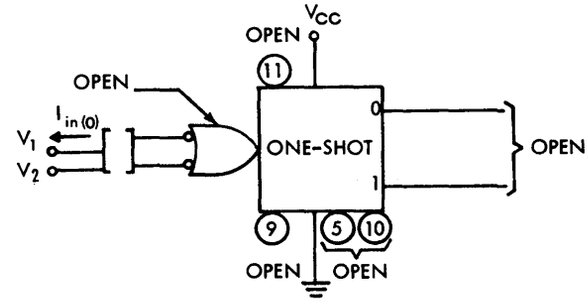
SN15 951



1. Each input is tested separately.

FIGURE 45 — $I_{in(1)}$

SN15 951



1. Each input is tested separately by applying V_2 to input under test and V_1 to the other input.

FIGURE 46 — $I_{in(0)}$

SN15 951

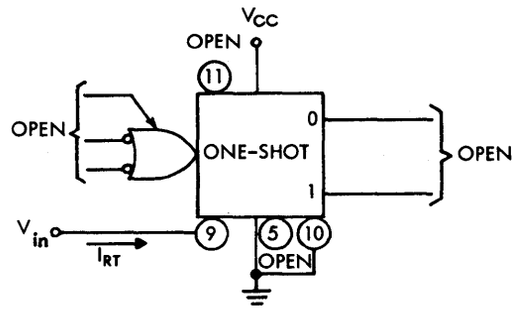


FIGURE 47 — I_{RT}

SN15 951

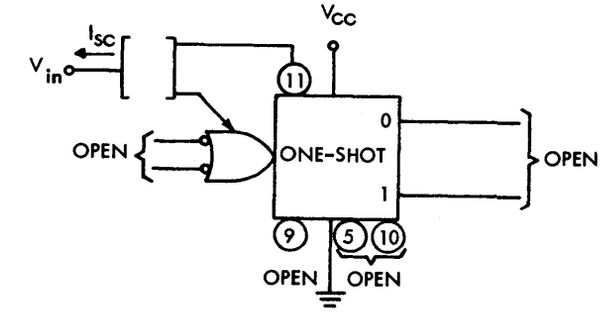


FIGURE 48 — I_{SC}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

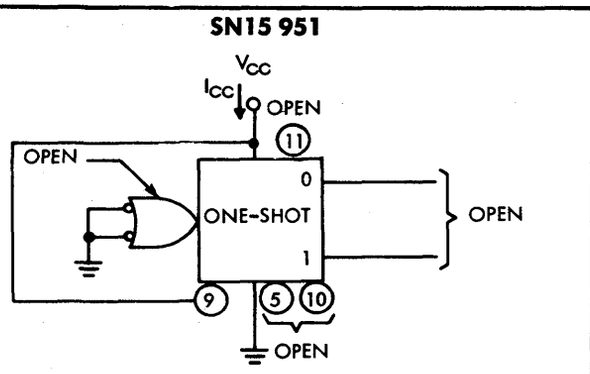


FIGURE 49 — I_{CC}

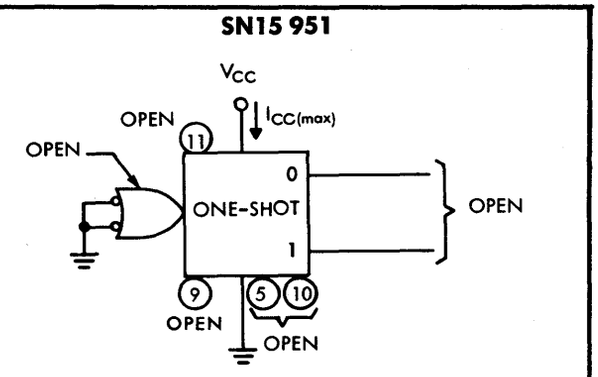
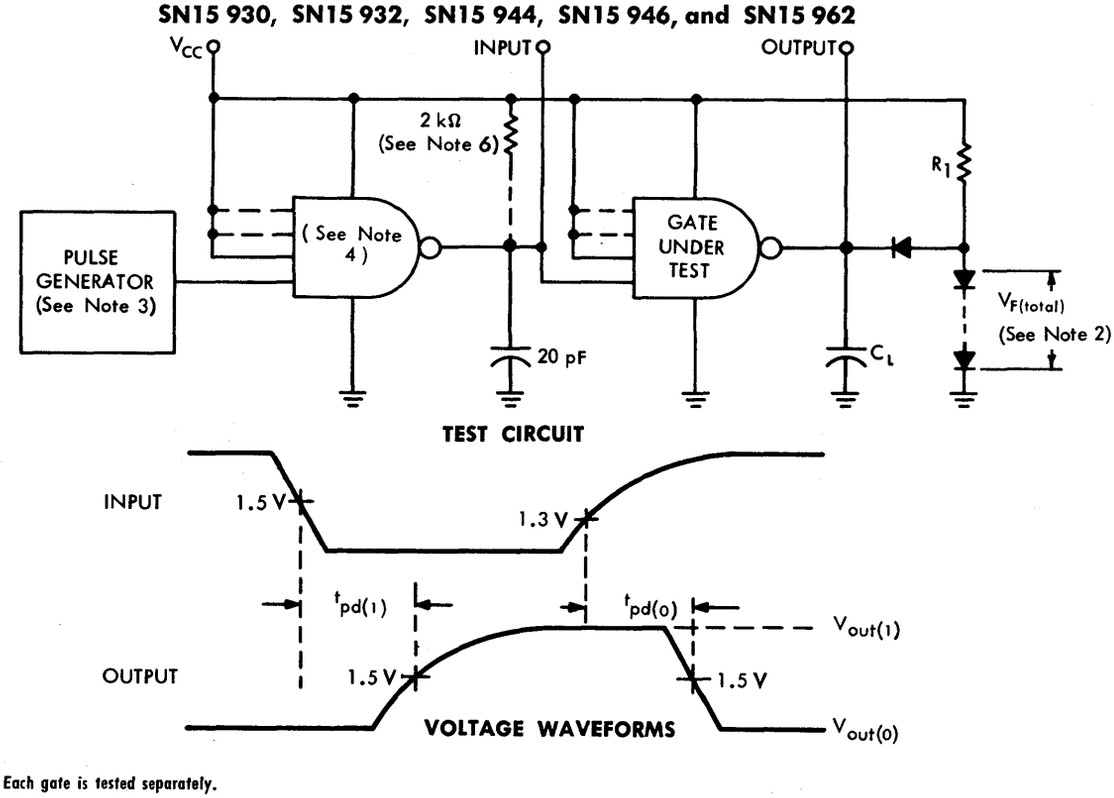


FIGURE 50 — $I_{CC(max)}$

†Arrows indicate actual direction of current flow.

switching characteristics



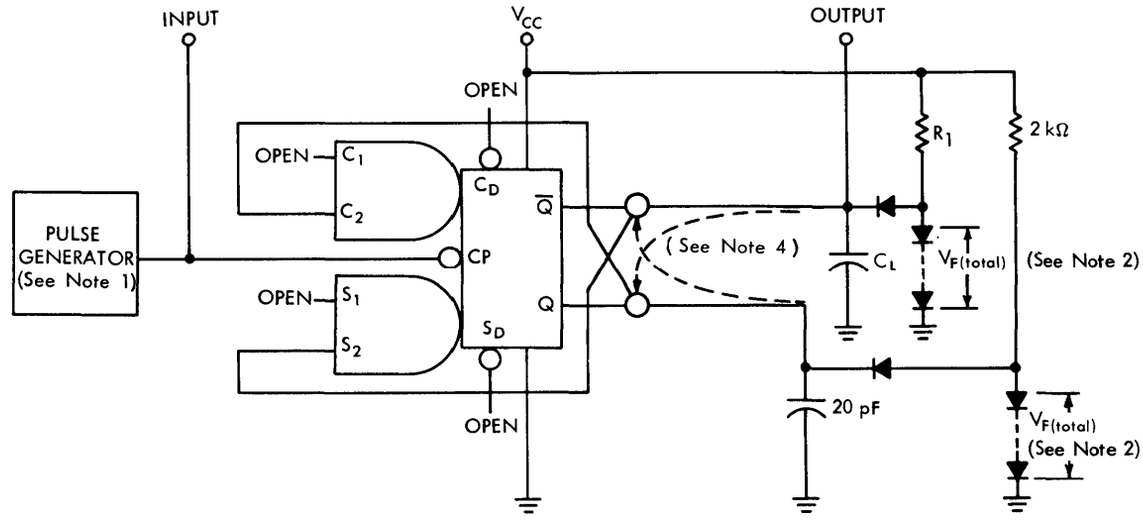
NOTES: 1. Each gate is tested separately.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)} = 1.9$ V to 2.5 V at 2 mA of current.
3. The generator has the following characteristics:
$V_{out} = 3$ V, $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_p = 300$ ns, PRR $= 1$ MHz, $Z_{out} \cong 50\ \Omega$.
4. The driving network is of the same type as the gate under test.
5. Voltage values are with respect to network ground terminal.
6. When testing the SN15 944, connect the 2-kΩ resistor as shown, omit all diodes, and connect resistor R_1 to capacitor C_L and output.

FIGURE 51 — GATE PROPAGATION DELAY

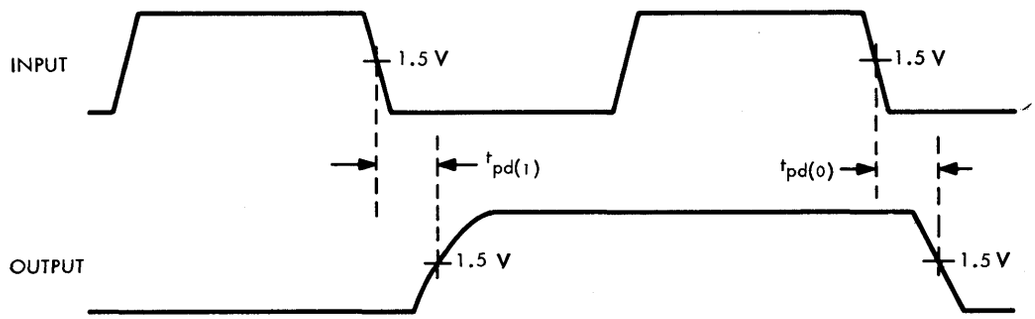
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SN15 931, SN15 945, and SN15 948



TEST CIRCUIT



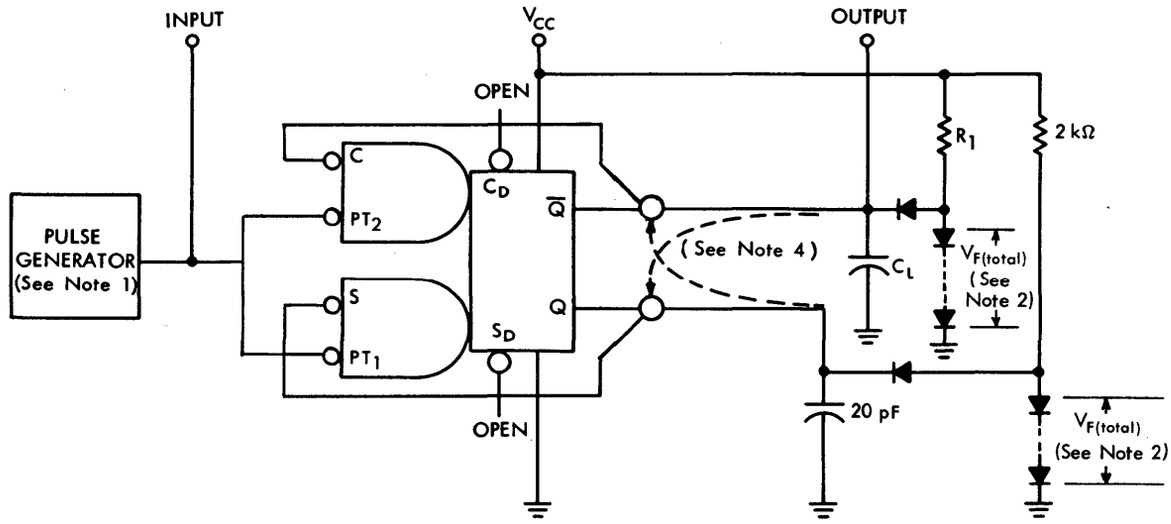
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
$V_{out} = 3$ V, $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_p = 300$ ns, PRR $= 1$ MHz, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)} = 1.9$ V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.
4. Test circuit shows loading when output $\overline{Q}$ is tested. When output Q is tested, loading is interchanged as indicated by the dotted lines.

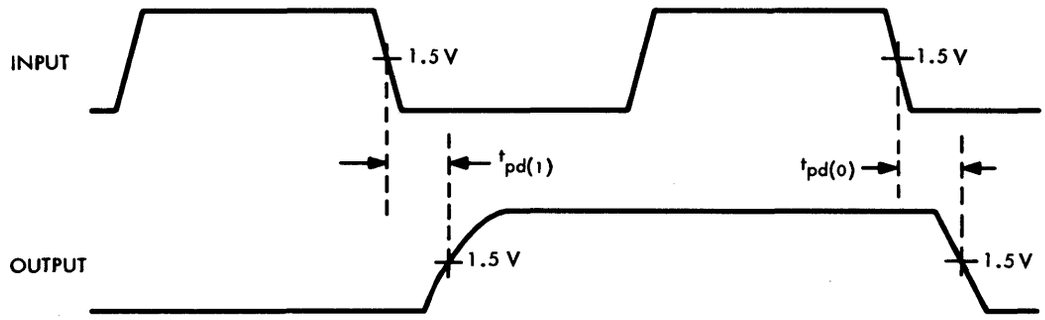
FIGURE 52 — FLIP-FLOP PROPAGATION DELAY

switching characteristics (continued)

SN15 950



TEST CIRCUIT



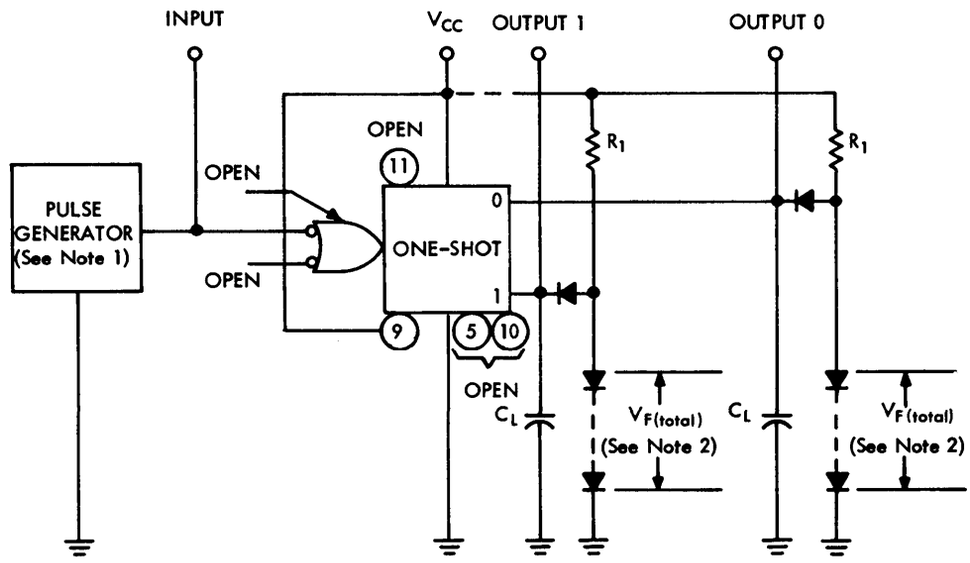
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
V_{out} = 3 V, $t_r \leq$ 15 ns, $t_f \leq$ 15 ns, t_p = 300 ns, PRR = 1 MHz, $Z_{out} \simeq$ 50 Ω.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)}$ = 1.9 V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.
4. Test circuit shows loading when output $\overline{Q}$ is tested. When output Q is tested, loading is interchanged as indicated by the dotted lines.

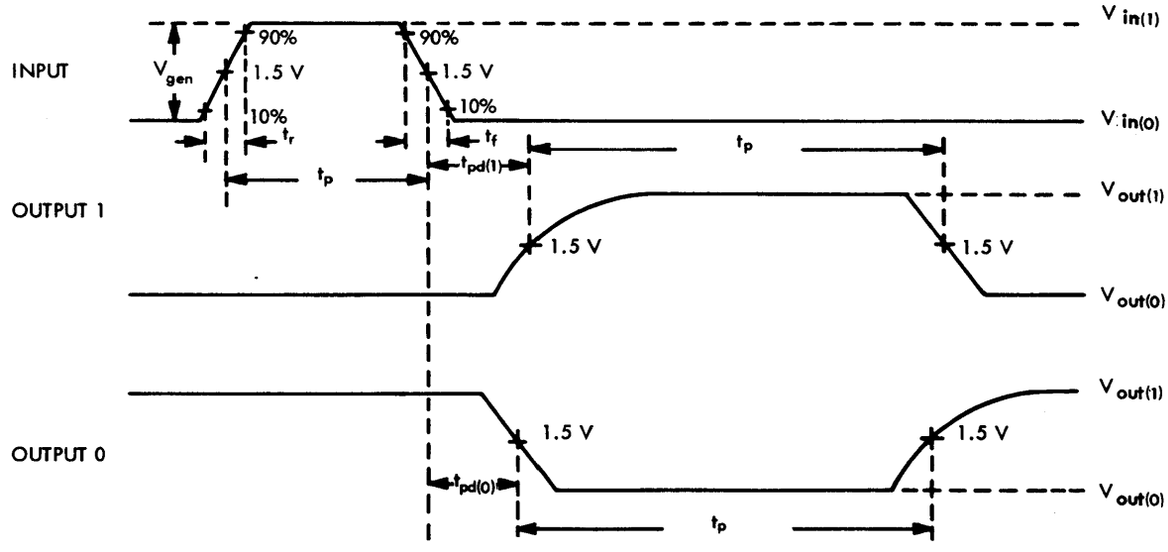
FIGURE 53 — PULSE-TRIGGERED BINARY PROPAGATION DELAY

switching characteristics (continued)

SN15 951



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
V_{gen} = 3 V, t_r = 15 ns, t_f = 15 ns, t_p = 300 ns, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)}$ = 1.9 V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.

FIGURE 54 — MONOSTABLE MULTIVIBRATOR PROPAGATION DELAY AND PULSE WIDTH

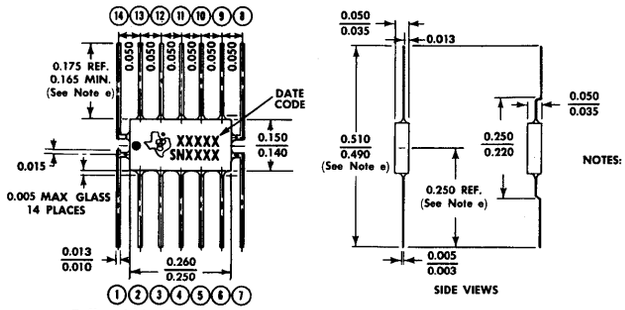
SERIES 15 930
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

general

SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 15 930 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pack carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE

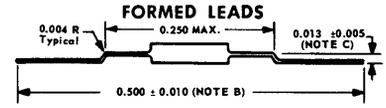


NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

FORMED LEADS



NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

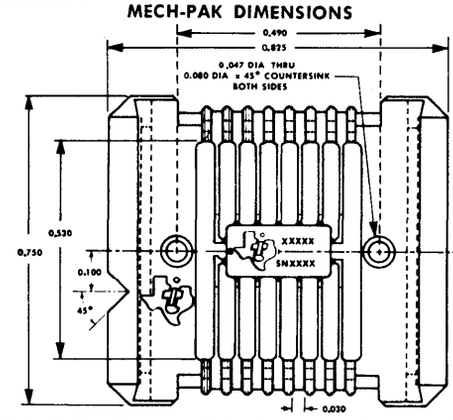
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inches thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPES SN521A, SN522A
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TYPES SN521A, SN522A
BULLETIN NO. DL-S 633468, JANUARY 1963
REVISED OCTOBER 1966

SERIES 52 OPERATIONAL AMPLIFIERS
for application in
Military & Industrial Control Systems • Analog-to-Digital Convertors • Analog Computers
Improved Version of SN521 and SN522

description

Each of these networks is a general-purpose operational amplifier. The SN521A single-ended amplifier has both inverting and noninverting inputs. The SN522A, in addition to both types of inputs, features a single-ended output with higher output current drive capability.

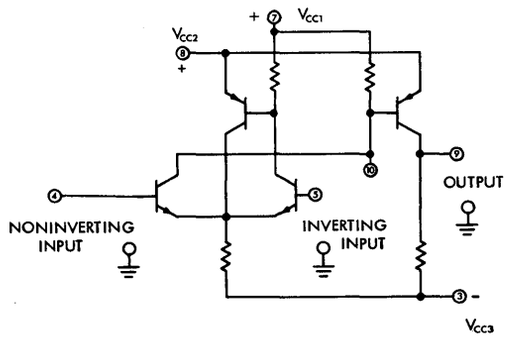
The SN521A and SN522A, two of Texas Instruments Series 52 catalog line integrated circuits, offer higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.

typical operating characteristics and conditions

Open-loop voltage gain	62 db
Common-mode rejection	60 db
Dynamic output voltage range	±2.5 v
Frequency response	DC to 50 kc
Operating ambient temperature range	–55°C to 125°C
Supply voltages: V_{CC1}	+10 v
V_{CC2}	+6 v
V_{CC3}	–9 v

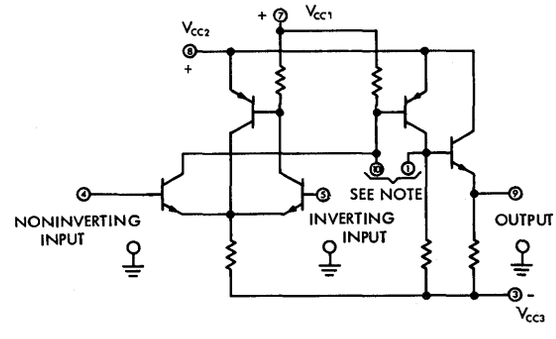
circuit diagrams

CIRCUIT DIAGRAM SN521A



NOTES: PIN ⑩ IS FOR FREQUENCY SHAPING
PINS ①, ②, AND ⑥ — NO INTERNAL CONNECTION

CIRCUIT DIAGRAM SN522A



NOTES: PINS ⑩ AND ① ARE FOR FREQUENCY SHAPING
PINS ② AND ⑥ — NO INTERNAL CONNECTION

†Patented by Texas Instruments

absolute maximum ratings

Supply Voltages: V_{CC1} . . . . . +15 v
V_{CC2} . . . . . +10 v
V_{CC3} . . . . . −15 v
Input Voltage (Common-Mode) . . . . . ± 4 v
Operating Ambient Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

electrical characteristics over operating ambient temperature range (unless otherwise noted)

All measurements shown are with amplifier in the open-loop condition and with the following supply voltages: V_{CC1} = +10 v ± 0.2 v; V_{CC2} = +6 v ± 0.2 v; V_{CC3} = −9 v ± 0.2 v.

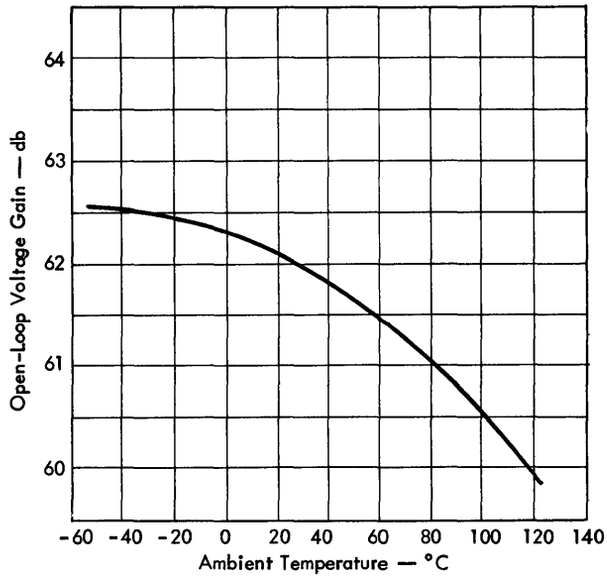
	SN521A			SN522A			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Voltage Gain, Open Loop Output Voltage, E_o = 1 v rms; f = 1 kc	54	62		54	62		db
Common Mode Rejection Output Voltage, E_o = 1 v rms; f = 1 kc	50	60		50	60		db
Dynamic (Linear) Output Voltage Range Peak or dc with output open-circuited (Note 1) T_A = 25°C	±2.5			±2.5			v
Peak or dc with external load resistance of: (Important: See Note 2)							
R_L = 2000 Ω, T_A = 25°C					±2.7		v
R_L = 8000 Ω, T_A = 25°C		±4.1					v
Input Resistance Noninverting input; with inverting input shorted to ground, T_A = 25°C	6	12		6	12		kΩ
Inverting input; with noninverting input shorted to ground, T_A = 25°C	30	100		30	100		kΩ
Output Resistance; T_A = 25°C	5	10			0.16	0.40	kΩ
Input Current; either input; T_A = 25°C		2			2		μa
Output Offset Voltage Both inputs with 510 Ω ±1% to ground; T_A = 25°C		−0.5	±2		−0.5	±2	v
D-C Drift referred to Input Both inputs with 510 Ω ±1% to ground		8	25		8	25	μv/C°
Frequency Response Half-Power Point (−3 db); T_A = 25°C	30	50		30	50		kc
Unity Gain (0 db); T_A = 25°C		10			10		Mc
Power Drain; no external load, T_A = 25°C		28			72		mw

NOTES: 1. The open-circuit condition of the amplifier is defined as that condition in which the external load resistance applied between the output of the circuit and ground is equal to or greater than 200 kΩ.

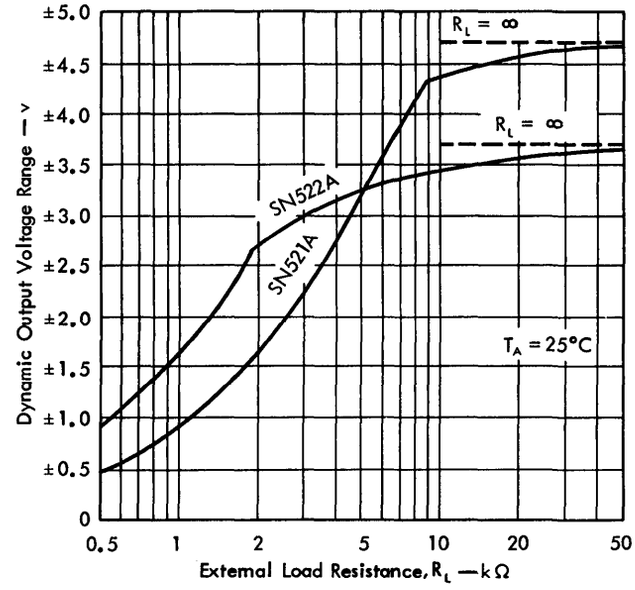
2. Under no circumstances are either of these networks to be operated with an external load of less than 200 Ω between the output of the amplifier and ground. Permanent damage to the semiconductor network may occur if this rule is not followed.

TYPICAL CHARACTERISTICS

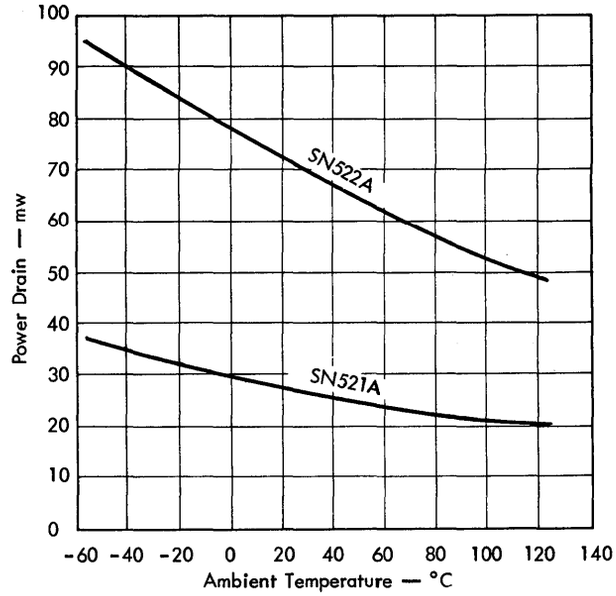
OPEN-LOOP VOLTAGE GAIN
vs
AMBIENT TEMPERATURE



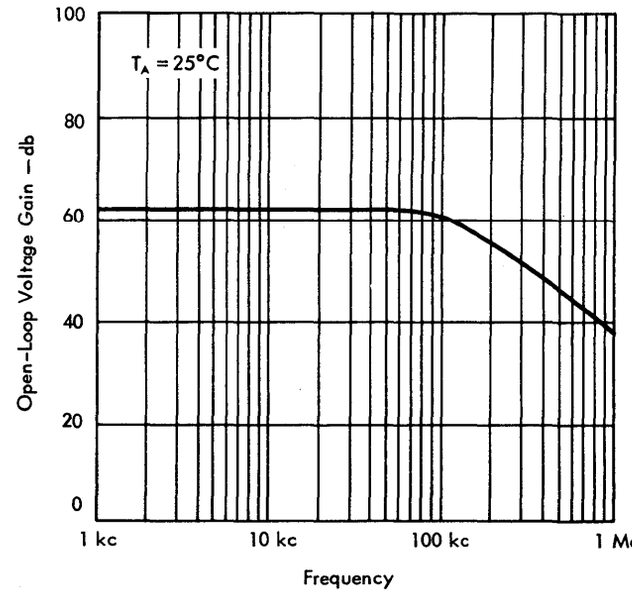
DYNAMIC OUTPUT VOLTAGE RANGE
vs
EXTERNAL LOAD RESISTANCE



OPEN-LOOP POWER DRAIN
vs
AMBIENT TEMPERATURE



OPEN-LOOP VOLTAGE GAIN
vs
FREQUENCY



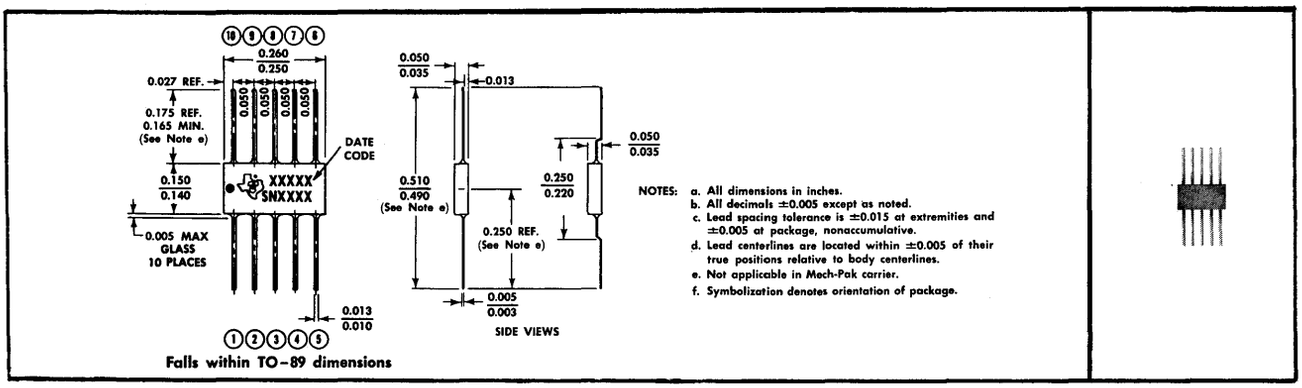
TYPES SN521A, SN522A
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

mechanical data

These operational amplifiers are mounted in glass-to-metal hermetically sealed welded packages meeting TO-89. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. Both are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

ORDERING INSTRUCTIONS

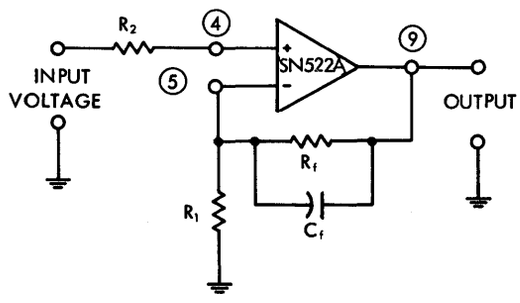
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPICAL APPLICATION

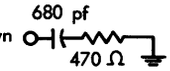
noninverting operational amplifier



TYPICAL FEEDBACK COMPONENTS AND ASSOCIATED CLOSED-LOOP GAIN

GAIN	R_1, kΩ	R_2, kΩ	R_f, kΩ	C_f, pf
2	10.0	5.1	10.0	33
6	6.2	5.1	31.0	10
10	5.6	5.1	51.0	10

conditions

Pin ⑦ ; V_{CC1} = +10 v
Pin ⑧ ; V_{CC2} = +6 v
Pin ③ ; V_{CC3} = −9 v
Frequency Shaping Network; connect the network as shown 

between pin ① and ground.

TYPE SN523A GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN523A
BULLETIN NO. DL-S 668494, MARCH 1966
REPLACES ENGINEERING SPEC. DATED AUGUST 1964

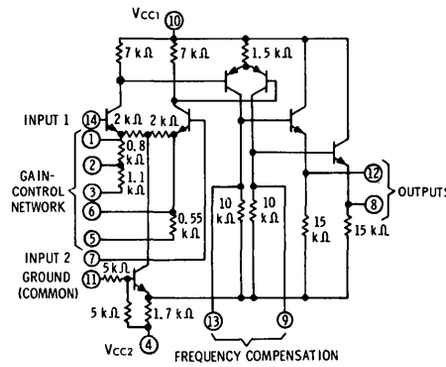
SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

description

The SN523A, offering differential inputs and differential emitter-follower outputs, incorporates a resistance network in the emitters of the input stage to facilitate gain adjustment. From the wide range of total resistance available, a particular value may be selected by connecting the resistor-network pins in a configuration which produces the desired gain. Maximum-gain configuration is with pin ① shorted to pin ⑥.

The SN523A, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

SCHEMATIC DIAGRAM

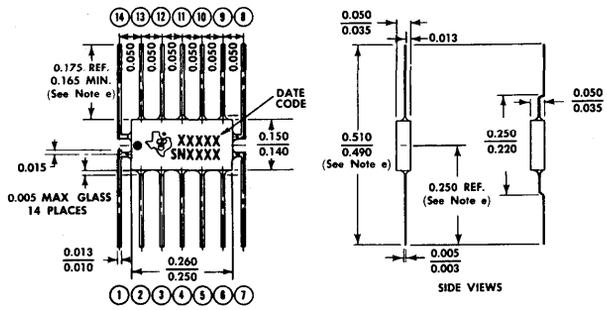
mechanical data

The SN523A is mounted in a glass-to-metal hermetically sealed welded package meeting TO-84. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN523A is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

ORDERING INSTRUCTIONS

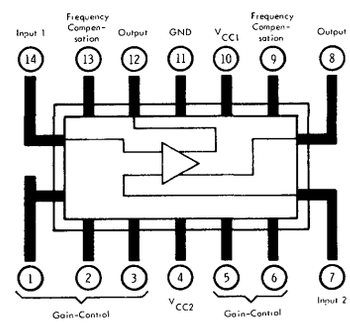
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

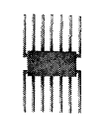
OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



Falls within TO-84 dimensions

NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.





†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 24% nickel, and 17% cobalt.

TYPE SN523A
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . ±6 V
Input Voltage (Either Input, See Note 1) . . . . . ±10 V
Duration of Short-Circuit Output Current . . . . . 5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . . 300 mW
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. Derate linearly to 120 mW at 125°C free-air temperature at the rate of 1.8 mW/deg.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			2.2	12	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = −55°C to 125°C		9		μV/deg
V_{CMO}	Common-mode output offset voltage			500		mV
I_{in}	Input current			5		μA
I_{DI}	Differential-input offset current			0.5	2	μA
V_{OM}	Maximum peak-to-peak output voltage	Differential output, f = 1 kc/s		24		V
		Differential output, f = 1 kc/s, T_A = −55°C to 125°C	20			V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_{VD}	Differential voltage gain	f = 1 kc/s		4000		
		f = 1 kc/s, T_A = −55°C to 125°C	2500			
		f = 1 kc/s, pins ① and ⑥ open		135		
		f = 1 kc/s, pin ① shorted to pin ⑥, pin ⑥ open		830		
		f = 1 kc/s, pin ② shorted to pin ⑤, pins ① and ⑥ open		465		
		f = 1 kc/s, pin ③ shorted to pin ⑤, pins ① and ⑥ open		325		
		f = 1 kc/s, pin ② shorted to pin ⑥, pin ① open		680		
CMRR	Common-mode rejection ratio	f = 1 kc/s		90		dB
BW	Bandwidth (−3 dB)		70	180		kc/s
Z_{in}	Input impedance	f = 1 kc/s	5	15		kΩ
Z_{out}	Output impedance	f = 1 kc/s		200		Ω
P_T	Total power dissipation			100		mW

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading; pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

letter symbol and parameter definitions

V_{DI} — That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

V_{CMO} — That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} — The current into either input of the amplifier.

I_{DI} — The difference in the currents into the two input terminals when the output is balanced.

V_{OM} — The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} — The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR — The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW — The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

Z_{in} — The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} — The impedance between the output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS§

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

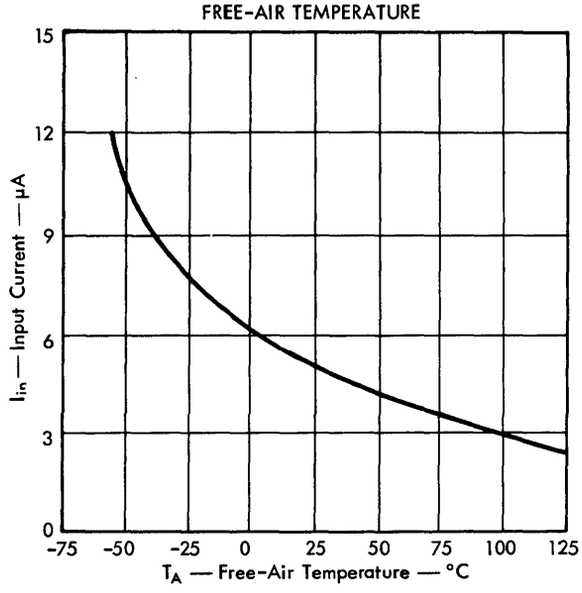


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

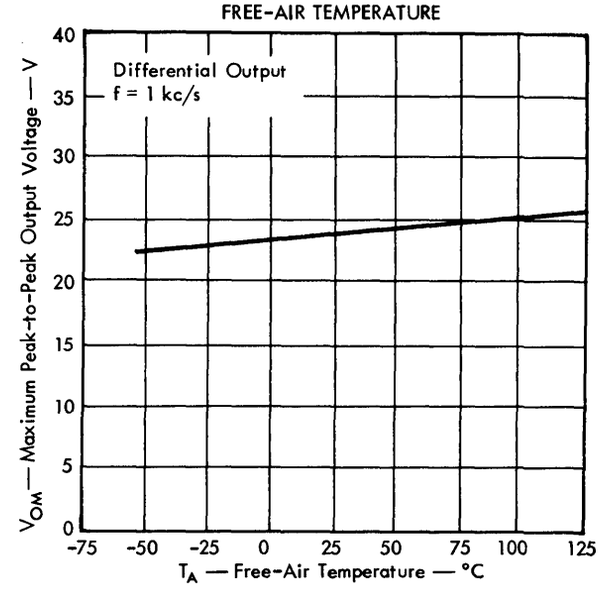


FIGURE 2

SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

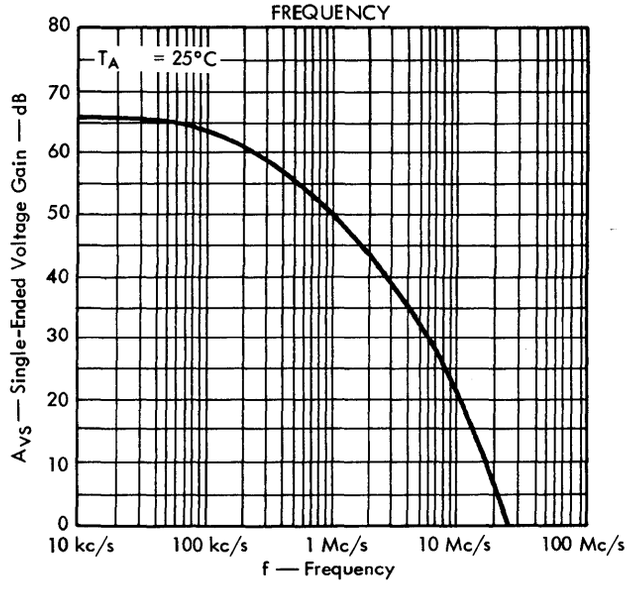


FIGURE 3

DIFFERENTIAL VOLTAGE GAIN
vs
SUPPLY VOLTAGE

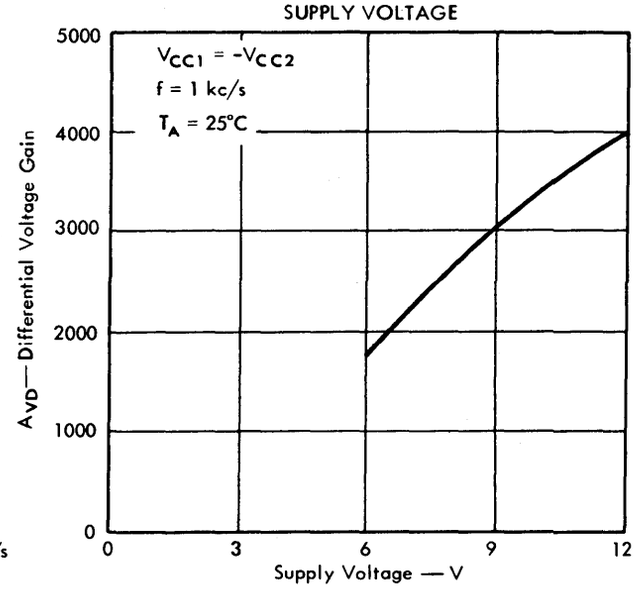


FIGURE 4

§Unless otherwise noted, test conditions are:
$V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

TYPICAL CHARACTERISTICS§

DIFFERENTIAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

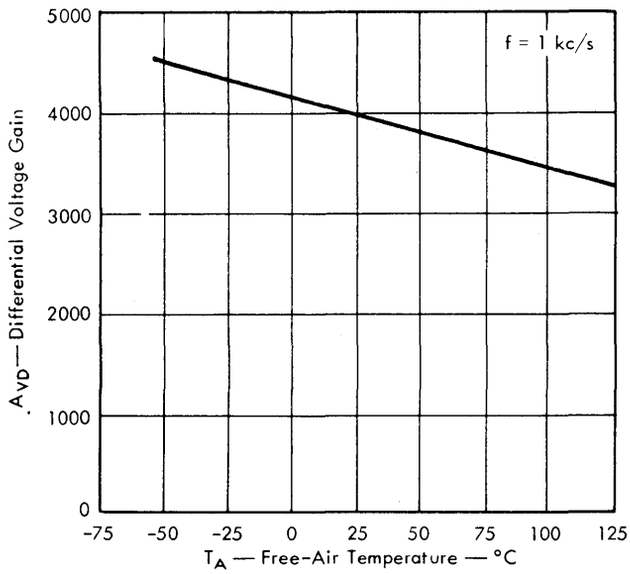


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

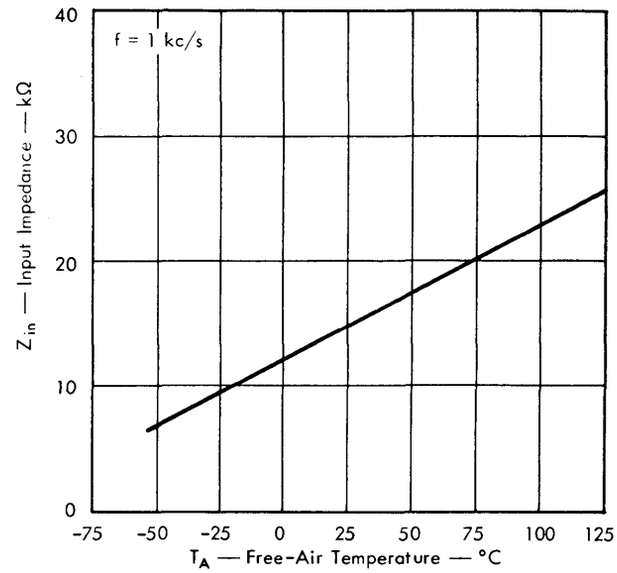


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

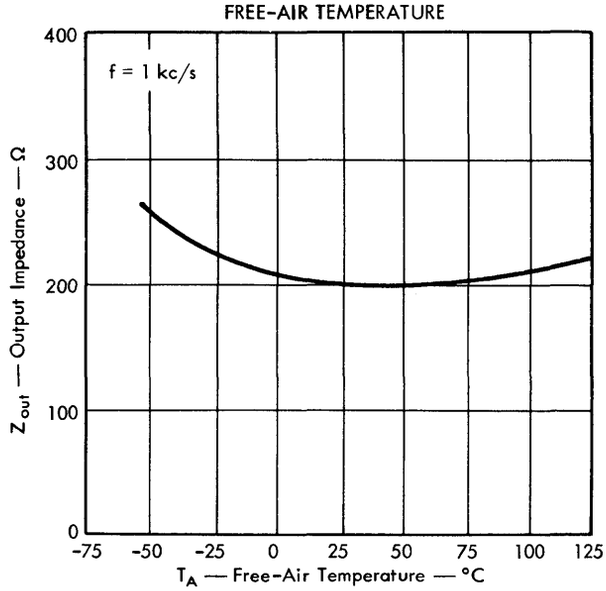


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

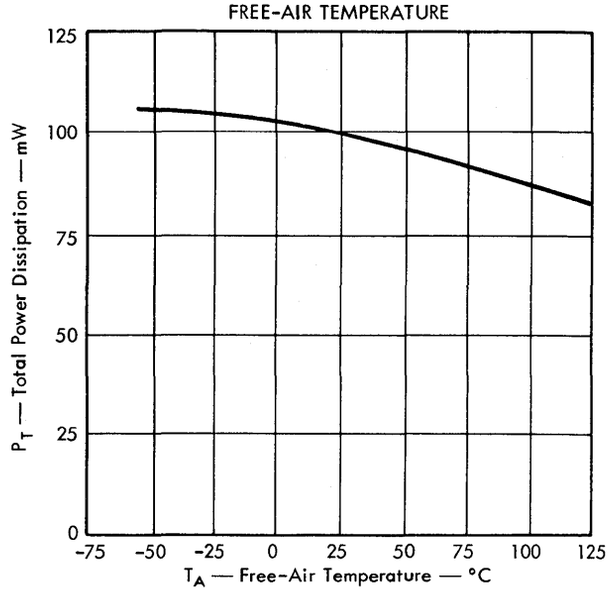


FIGURE 8

§Unless otherwise noted, test conditions are:

$V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

PRINTED IN U.S.A.

TYPE SN5231L GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN5231L
BULLETIN NO. DL-S 668833, AUGUST 1966

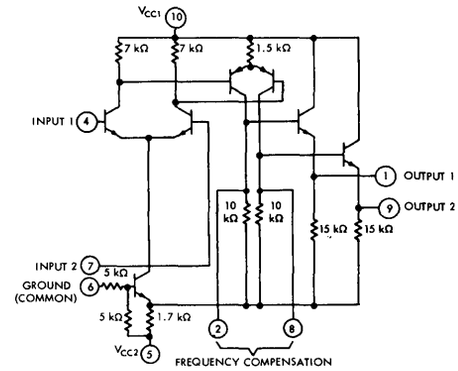
SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

description

The SN5231L offers differential inputs and differential emitter-follower outputs. Two stages of differential amplification are used to provide high gain at frequencies up to 1 MHz. A high degree of component matching, which assures stable operation over the temperature range of –55°C to 125°C, is achieved by the monolithic construction.

The SN5231L, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.

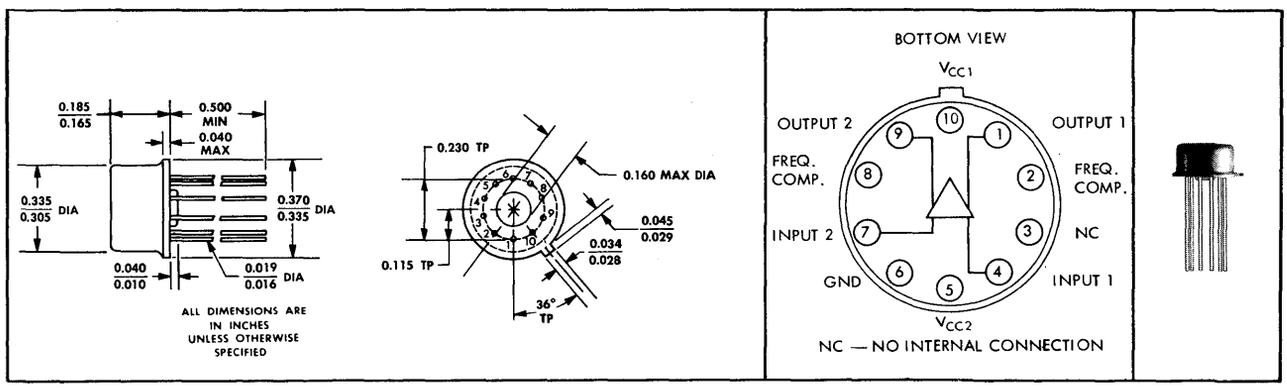


NOTE: Component values shown are nominal.

SCHEMATIC DIAGRAM

mechanical data

The SN5231L package outline is same as JEDEC TO-100 except for diameter of standoff.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1}	+15 V
V_{CC2}	–15 V
Differential Input Voltage	±6 V
Input Voltage (Either Input, See Note 1)	±10 V
Duration of Short-Circuit Output Current	5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	300 mW
Operating Free-Air Temperature Range	–55°C to 125°C
Storage Temperature Range	–65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.

2. Derate linearly to 120 mW at 125°C free-air temperature at the rate of 1.8 mW/deg.

†Patented by Texas Instruments

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			2.2	12	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	$T_{A(1)} = 125°C$, $T_{A(2)} = -55°C$		9		μV/deg
V_{CMO}	Common-mode output offset voltage			500		mV
I_{in}	Input current			5		μA
I_{DI}	Differential-input offset current			0.5	2	μA
V_{OM}	Maximum peak-to-peak output voltage	Differential output, f = 1 kHz		24		V
		Differential output, f = 1 kHz, $T_A = -55°C$ to 125°C	20			V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_{VD}	Differential voltage gain	$R_S = 50\ \Omega$, f = 1 kHz		4000		
		$R_S = 50\ \Omega$, f = 1 kHz, $T_A = -55°C$ to 125°C	2500			
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, f = 1 kHz		90		dB
BW	Bandwidth (–3 dB)		70	180		kHz
Z_{in}	Input impedance	f = 1 kHz	5	15		kΩ
Z_{out}	Output impedance	f = 1 kHz		200		Ω
P_T	Total power dissipation			100		mW

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin (6) grounded.

letter symbol and parameter definitions

V_{DI} That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

α_{VDI} Temperature coefficient averaged over the specified temperature range and defined by the equation:

$$\alpha_{VDI} = \frac{(V_{DI} @ T_{A(1)}) - (V_{DI} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}$$

V_{CMO} That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} The current into either input of the amplifier.

I_{DI} The difference in the currents into the two input terminals when the output is balanced.

V_{OM} The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR The ratio of the differential-mode voltage gain to the commmon-mode voltage gain.

BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

Z_{in} The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} The impedance between either output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS§

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

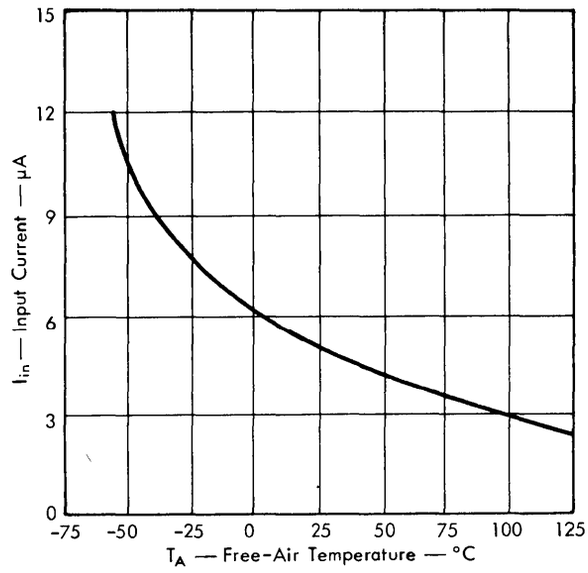


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

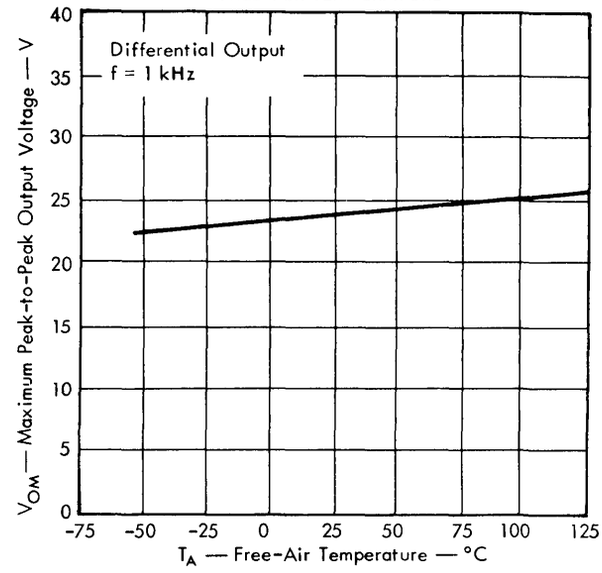


FIGURE 2

SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

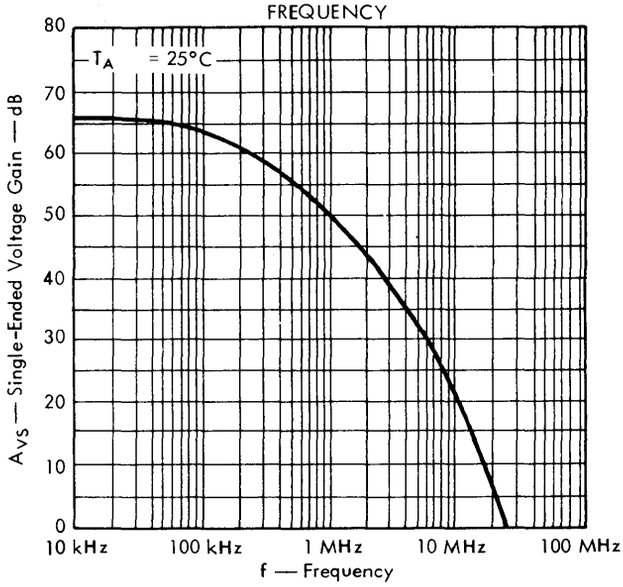


FIGURE 3

DIFFERENTIAL VOLTAGE GAIN
vs
SUPPLY VOLTAGE

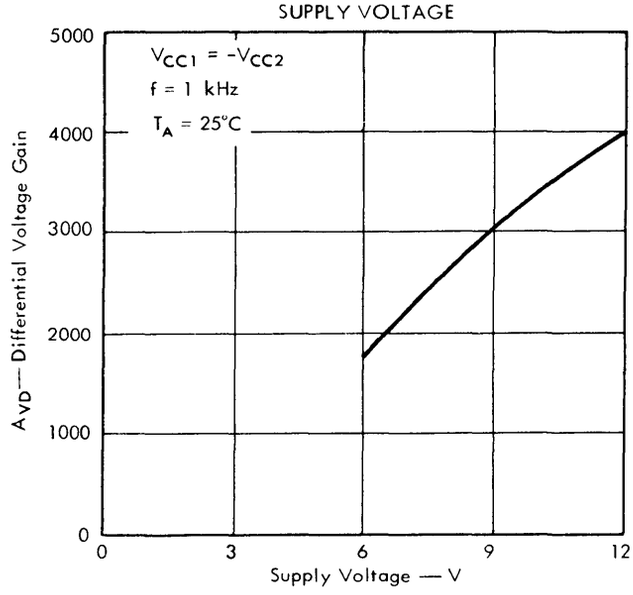


FIGURE 4

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin (6) grounded.

TYPICAL CHARACTERISTICS §

DIFFERENTIAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

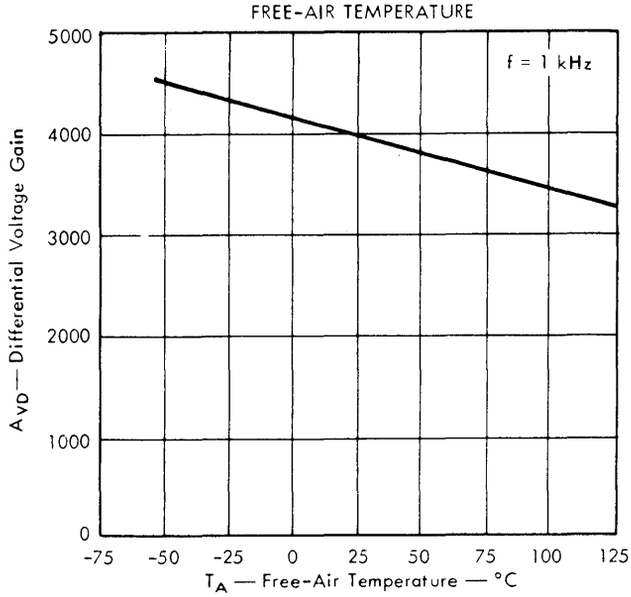


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

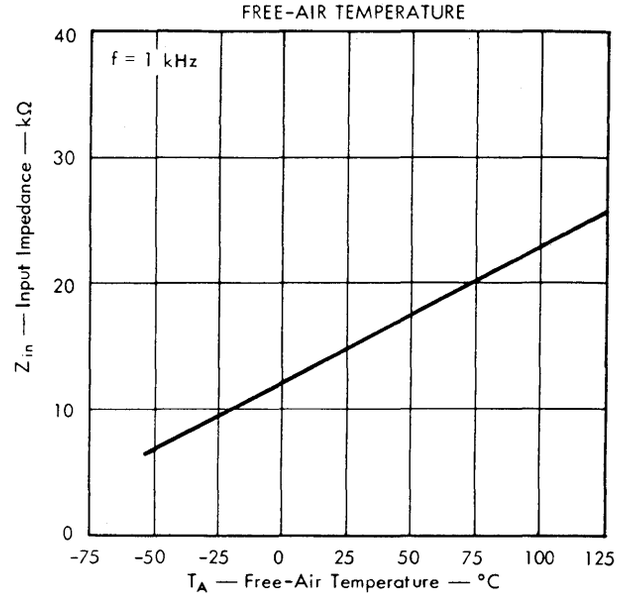


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

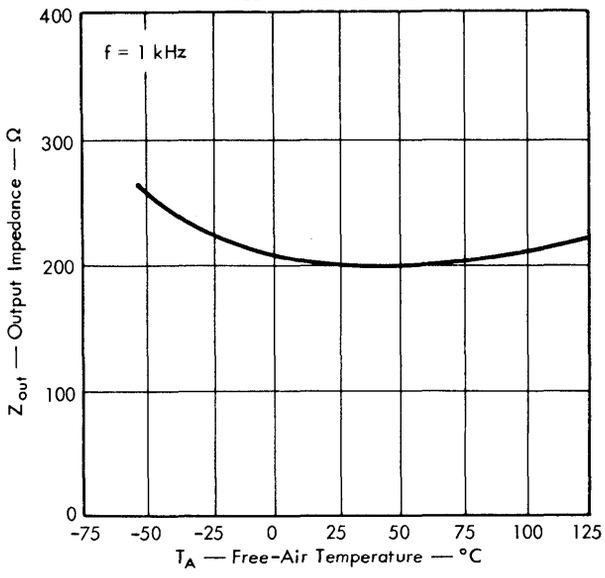


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

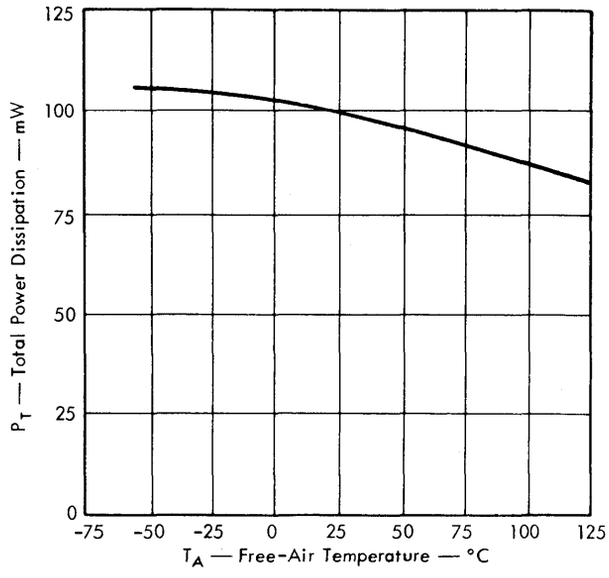


FIGURE 8

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin (6) grounded.

PRINTED IN U.S.A.

TYPES SN524A, SN524AL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TYPES SN524A, SN524AL
BULLETIN NO. DL-S 668375, MARCH 1966
REPLACES ENGINEERING SPEC. DATED AUGUST 1964

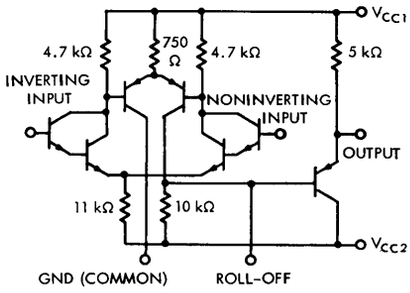
SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIERS for application as

- Buffer Amplifier
- Differentiator
- Integrator
- Multivibrator
- Level Detector
- Summing Amplifier

description

Each of these networks is a general-purpose operational amplifier consisting of two differential-gain stages and a single-ended emitter-follower output. The input stage utilizes Darlington-connected n-p-n transistors for high input impedance.

The SN524A and SN524AL, two of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

SCHEMATIC DIAGRAM

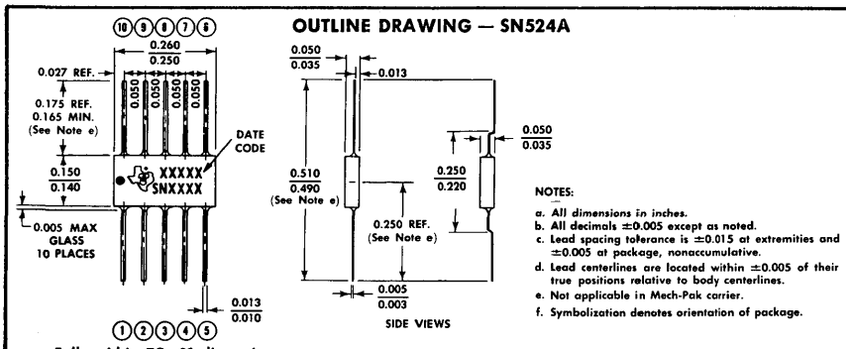
mechanical data

The SN524A operational amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN524A is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

SN524A ORDERING INSTRUCTIONS

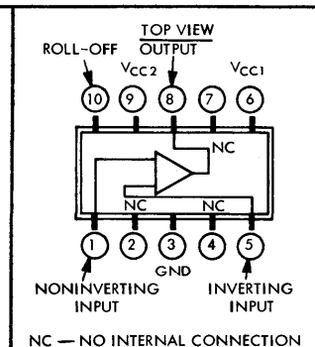
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

OUTLINE DRAWING — SN524A



Falls within TO-89 dimensions

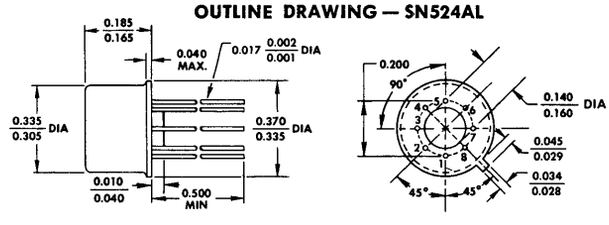
NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.



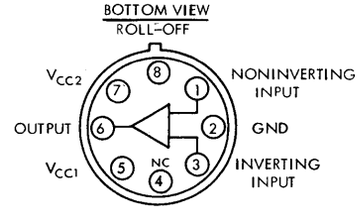
NC — NO INTERNAL CONNECTION

The SN524AL package outline is same as JEDEC TO-76 except for case height.

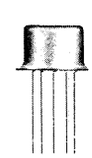
OUTLINE DRAWING — SN524AL



DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED



NC — NO INTERNAL CONNECTION



†Patented by Texas Instruments.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . 12 V
Common-Mode Input Voltage . . . . . ±10 V
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			12		mV
		T_A = −55°C to 125°C			40	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = −55°C to 125°C		25		μV/deg
I_{in}	Input Current			80	350	nA
I_{DI}	Differential-input offset current			20		nA
		T_A = −55°C		60		nA
		T_A = 125°C		6		nA
V_{OM}	Maximum peak-to-peak output voltage	f = 1 kc/s, T_A = −55°C to 125°C	11			V
		f = 1 kc/s		16		V
		10 kΩ load, f = 1 kc/s, T_A = −55°C to 125°C	9			V
		10 kΩ load, f = 1 kc/s		15		V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_V	Voltage gain	f = 1 kc/s, T_A = −55°C to 125°C	630			
		f = 1 kc/s		1400		
CMRR	Common-mode rejection ratio	f = 1 kc/s, T_A = −55°C to 125°C		55		dB
BW	Bandwidth (−3 dB)		70	140		kc/s
Z_{in}	Input impedance	f = 1 kc/s	350	1000		kΩ
Z_{out}	Output impedance	f = 1 kc/s		200		Ω
P_T	Total power dissipation	No input signal, no external load		120		mW

§*Unless otherwise noted test conditions are:* V_{CC1} = +12 V, V_{CC2} = −12 V, *ground and* V_{DI} *applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.*

letter symbol and parameter definitions

V_{DI} That d-c voltage which must be applied between the input terminals to obtain zero-output voltage referenced to ground. The application of this voltage balances the amplifier.

I_{in} The current into either input of the amplifier.

I_{DI} The difference in the currents into the two input terminals when the output is balanced.

V_{OM} The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW The range of frequencies within which the voltage gain is within 3 dB of the mid-frequency value.

Z_{in} The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} The impedance between the output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS §

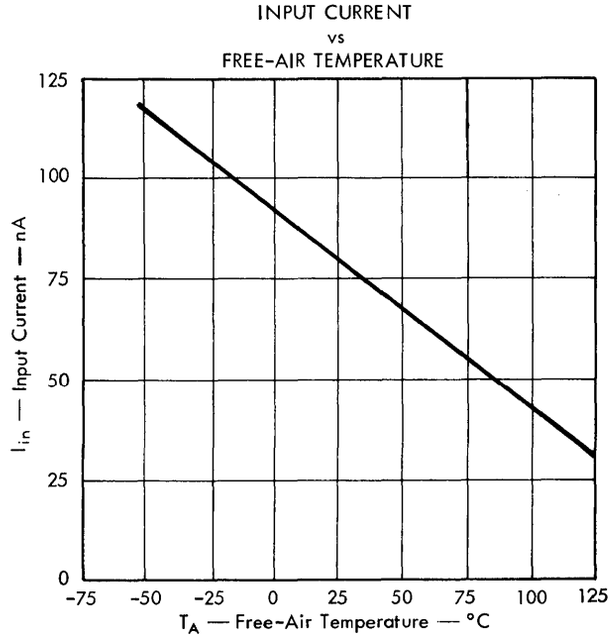


FIGURE 1

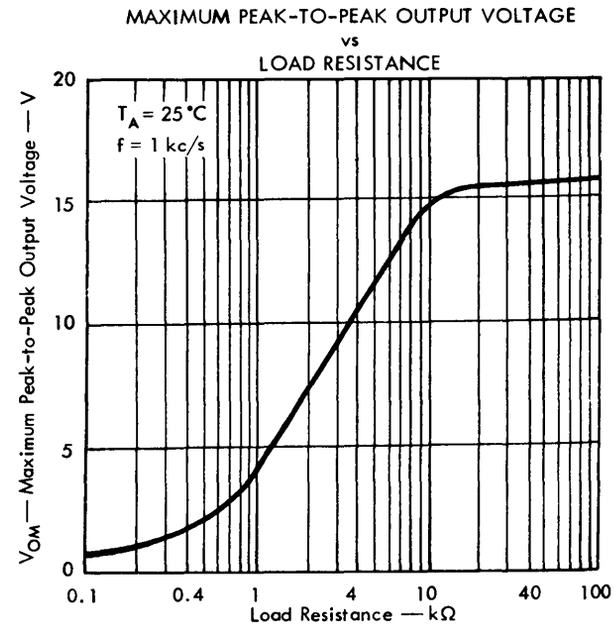


FIGURE 2

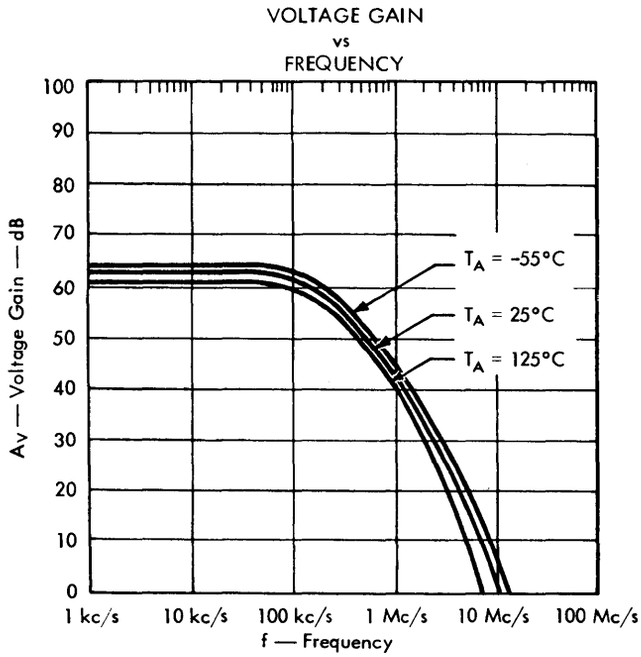


FIGURE 3

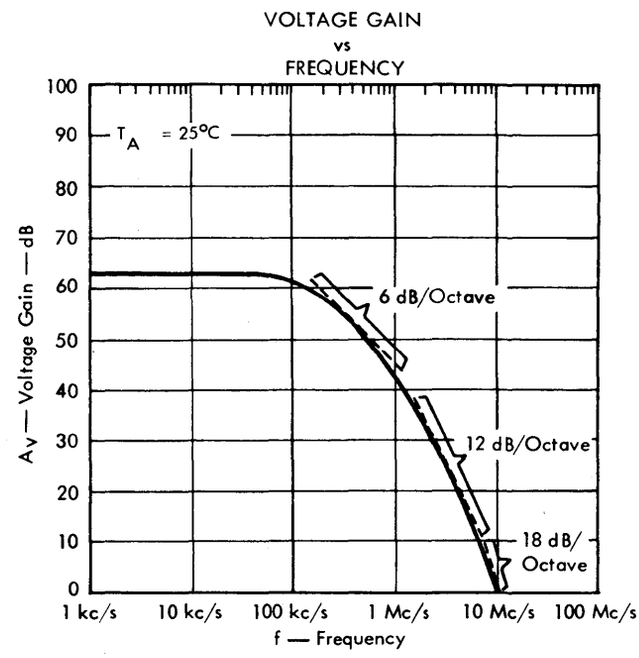


FIGURE 4

§Unless otherwise noted test conditions are: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

TYPICAL CHARACTERISTICS §

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

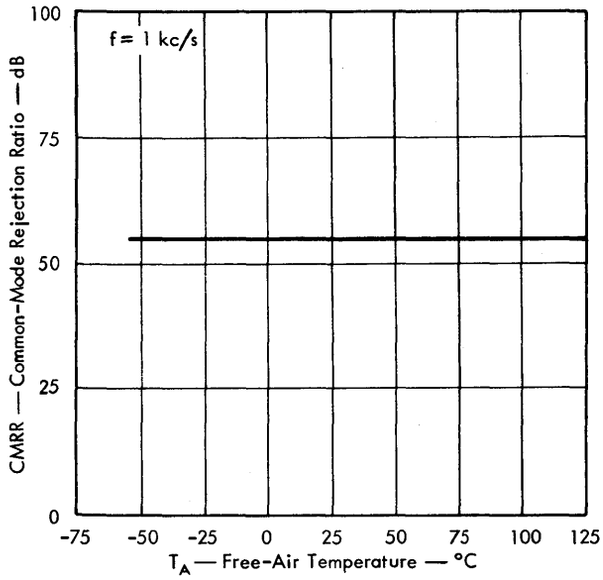


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

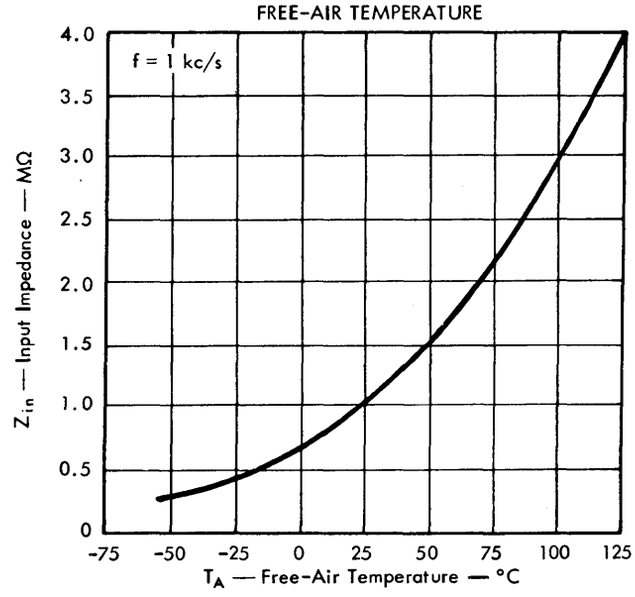


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

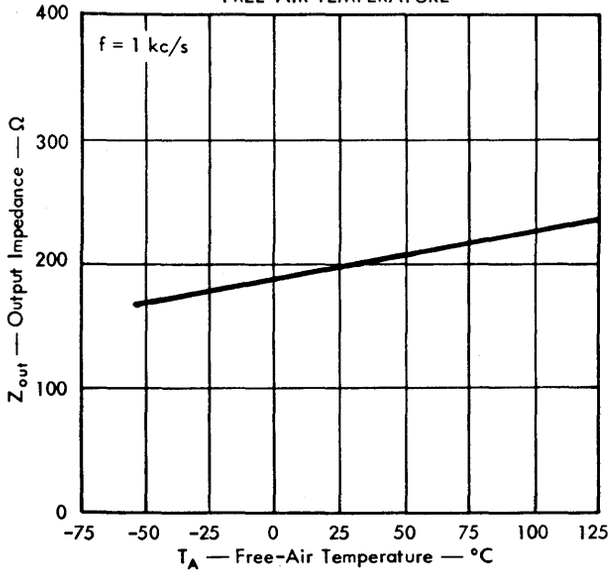


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

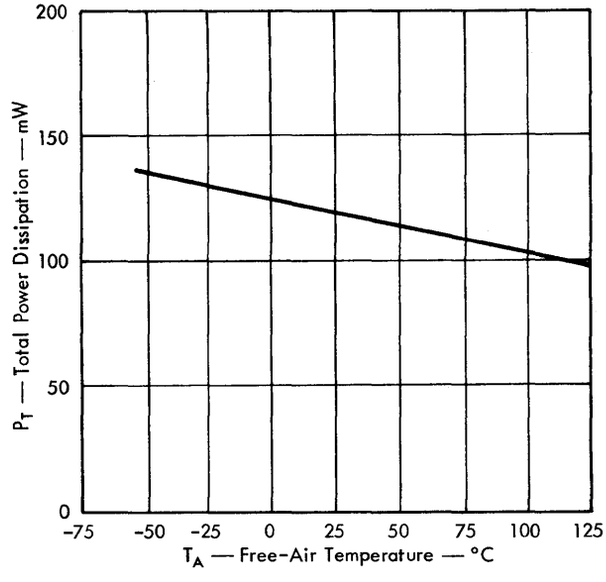


FIGURE 8

§Unless otherwise noted test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

PRINTED IN U.S.A.

TYPE SN525
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN525
BULLETIN NO. DL-S 669272, NOVEMBER 1966

A SERIES 52 AMPLIFIER

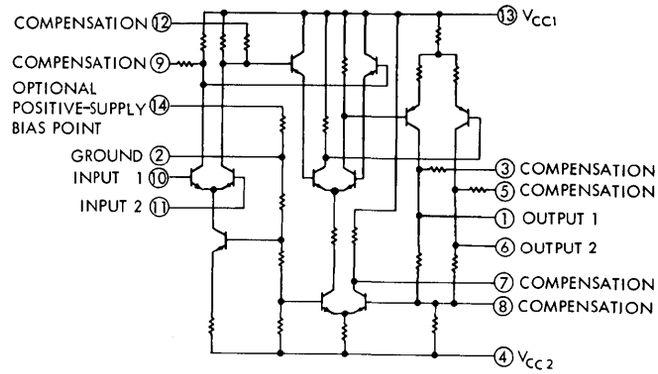
featuring

- **Open-Loop Gain ...90 dB**
- **Typical CMRR ...100 dB**

description

The SN525 is a high-performance amplifier featuring an open-loop gain of 90 dB, yet it is unconditionally stable when used with external capacitors in the frequency-response shaping circuit. A feedback loop provides high common-mode rejection. Both differential input and output terminals are available.

Texas Instruments Series 52 catalog line of linear integrated circuits offers higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



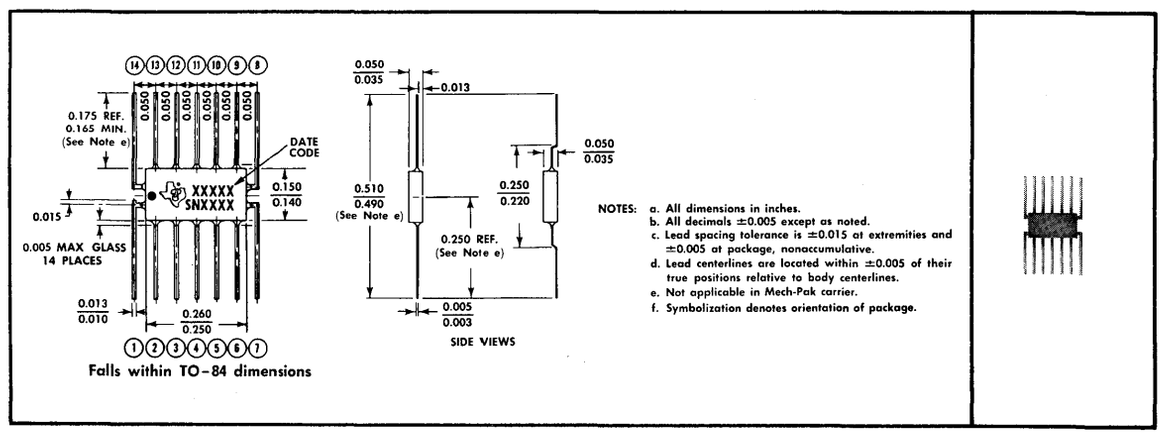
SCHEMATIC

mechanical data

The SN525 semiconductor network is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN525 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See ordering instructions.

ORDERING INSTRUCTIONS

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5



†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . 5 V
Common-Mode Input Voltage . . . . . ±12 V
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS §	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			1	3	mV
		T_A = −55°C to 125°C			4	mV
V_{CMO}	Common-mode output offset voltage			250	1000	mV
I_{in}	Input current	T_A = 125°C		270	700	nA
				450	900	nA
		T_A = −55°C		750	1500	nA
I_{DI}	Differential-input offset current	T_A = 125°C		12	200	nA
				16	200	nA
		T_A = −55°C		38	550	nA
V_{OM}	Maximum peak-to-peak output voltage	Single-ended output, f = 1 kHz		18		V
		Single-ended output, f = 1 kHz, T_A = −55°C to 125°C	14			V
V_{CMIM}	Maximum common-mode input voltage			±7		V
A_{VS}	Small-signal single-ended voltage gain	f = 1 kHz	20 000	32 000		
		f = 1 kHz, T_A = −55°C to 125°C	10 000			
A_{VCMS}	Small-signal common-mode single-ended voltage gain	f = 1 kHz			0.9	
CMRR	Small-signal common-mode rejection ratio	f = 1 kHz		100		dB
BW	Bandwidth (−3 dB)			45		kHz
z_{in}	Input impedance	f = 1 kHz	50	140		kΩ
z_{out}	Output impedance	f = 1 kHz		10		kΩ
SVRR	Supply voltage rejection ratio	$\Delta V_{CC} \leq 0.5$ V		25		μV/V
P_T	Total power dissipation			100	135	mW

§ Unless otherwise noted, test conditions include: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

letter symbol and parameter definitions

V_{DI} That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

V_{CMO} That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} The current into either input of the amplifier.

I_{DI} The difference in the currents into the two input terminals when the output is balanced.

V_{OM} The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

z_{in} The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

z_{out} The impedance between either output terminal and ground when the output is balanced.

SVRR The ratio of the change in input offset voltage to the change in power supply voltage which produces the variation.

compensation requirements

External capacitance must be connected between pins (7) and (8) to stabilize the amplifier if symmetrical compensation to ground is not used on pins (3) and (5) or pins (1) and (6).

TYPICAL CHARACTERISTICS §

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

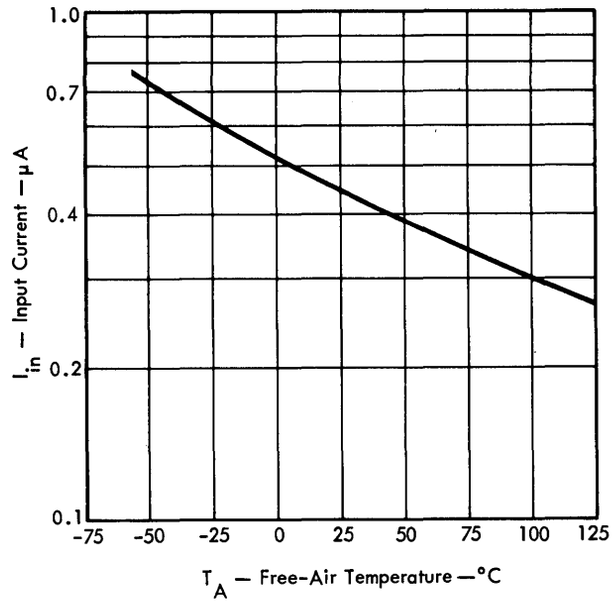


FIGURE 1

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

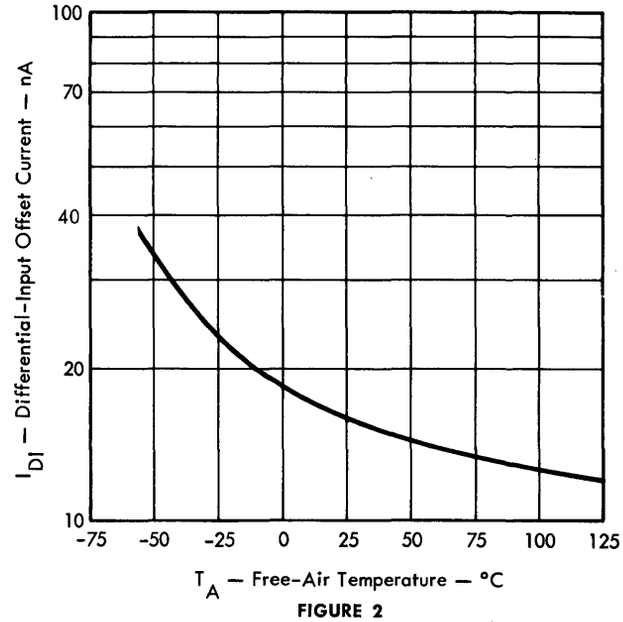


FIGURE 2

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

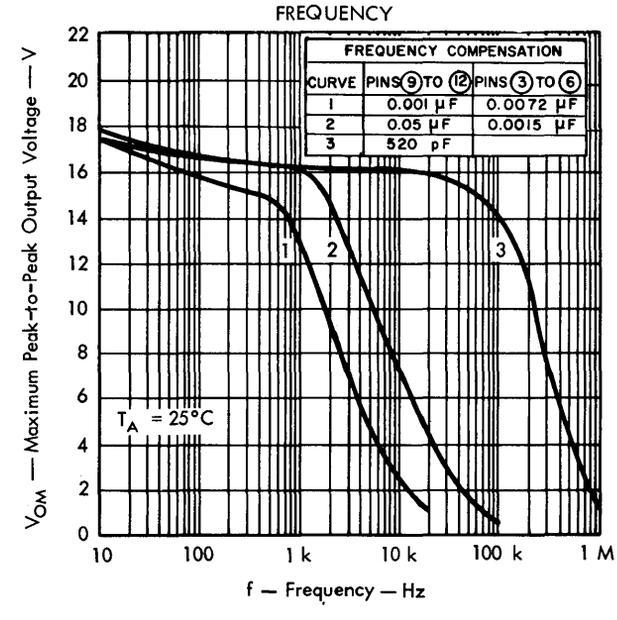


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

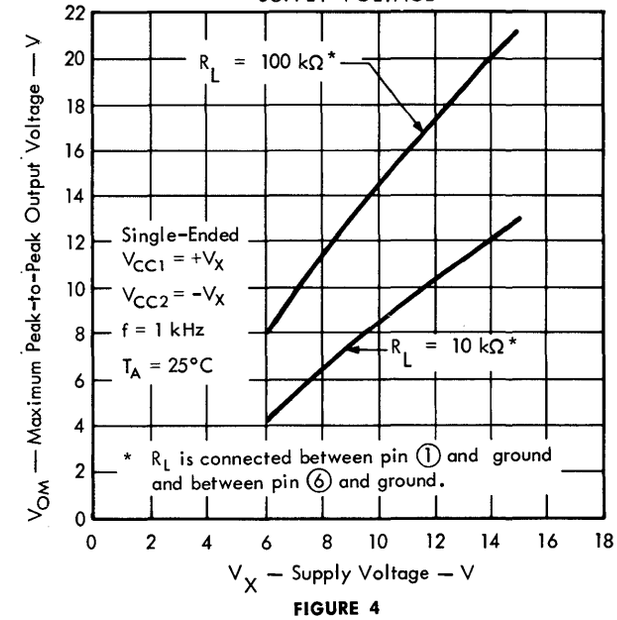


FIGURE 4

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

TYPICAL CHARACTERISTICS §

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

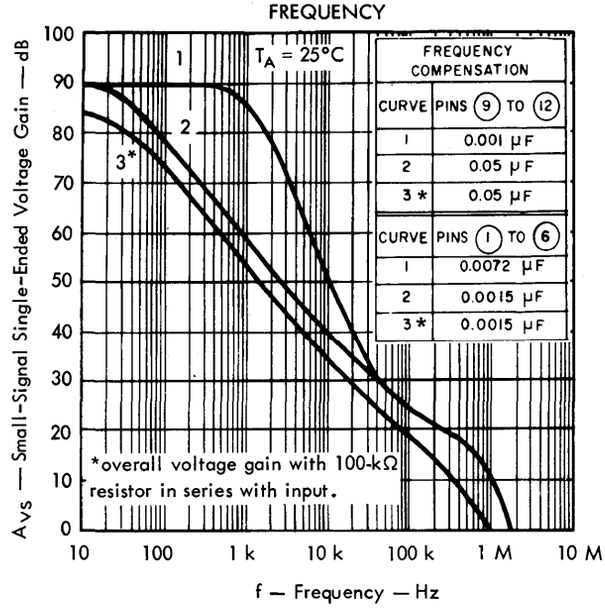


FIGURE 5

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

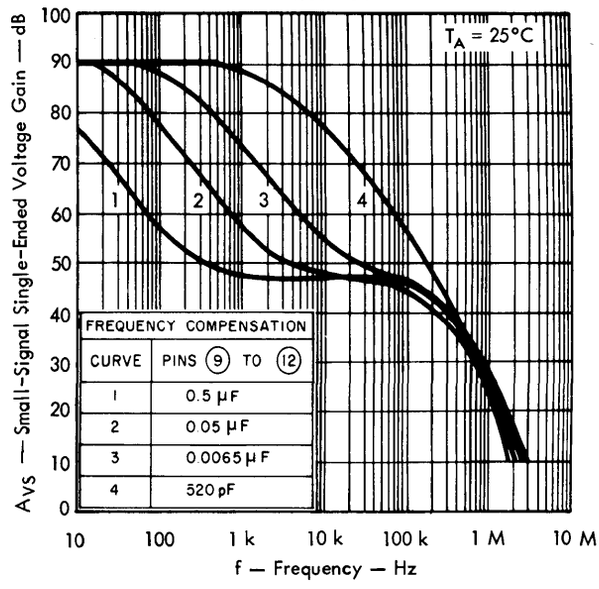


FIGURE 6

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

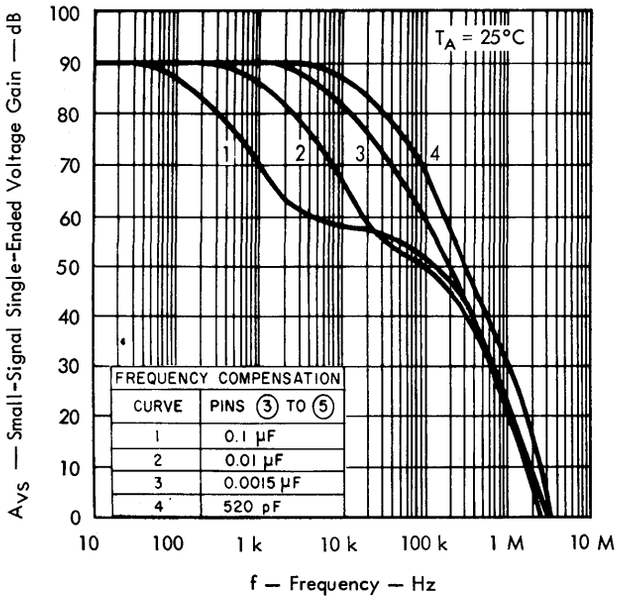


FIGURE 7

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

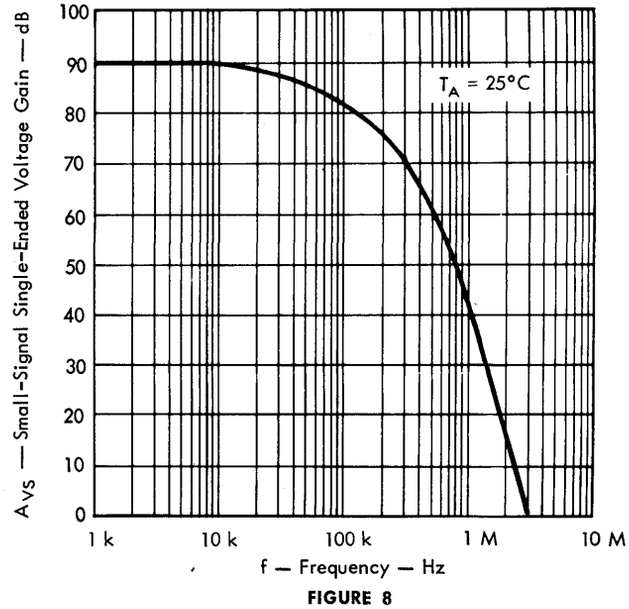


FIGURE 8

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

TYPICAL CHARACTERISTICS §

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

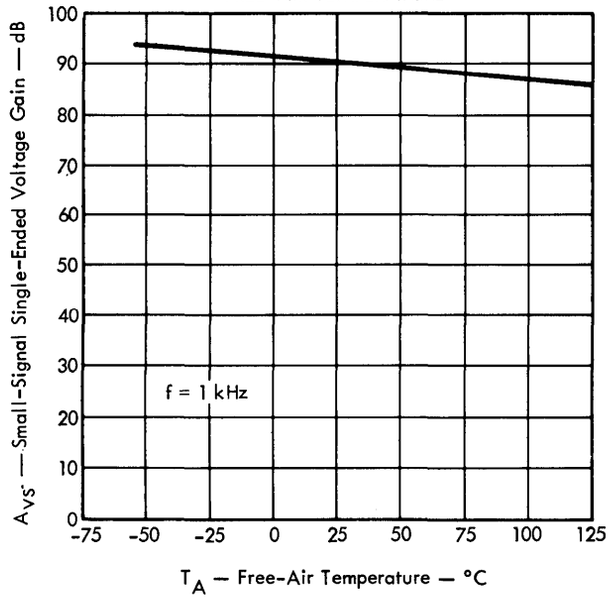


FIGURE 9

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
GAIN-CONTROL RESISTOR VALUE

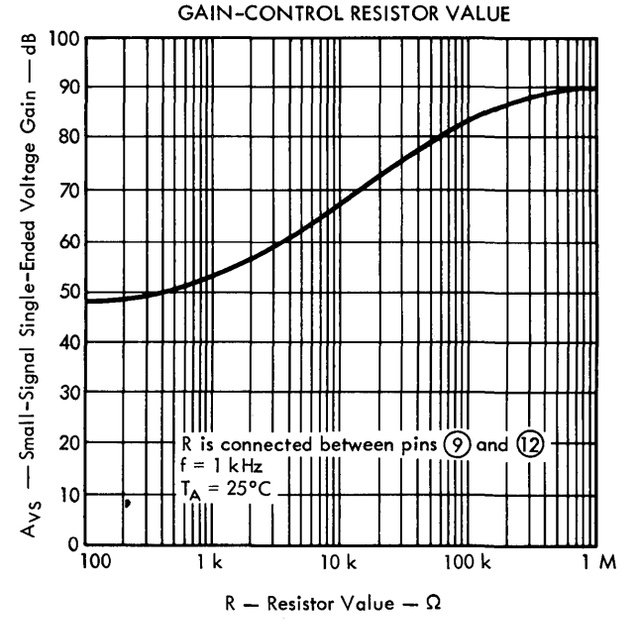


FIGURE 10

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
SUPPLY VOLTAGE

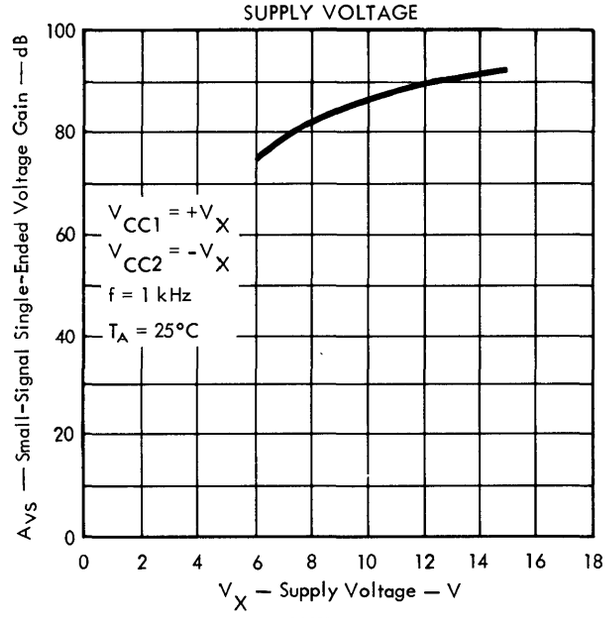


FIGURE 11

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

TYPICAL UNITY-GAIN CONFIGURATION

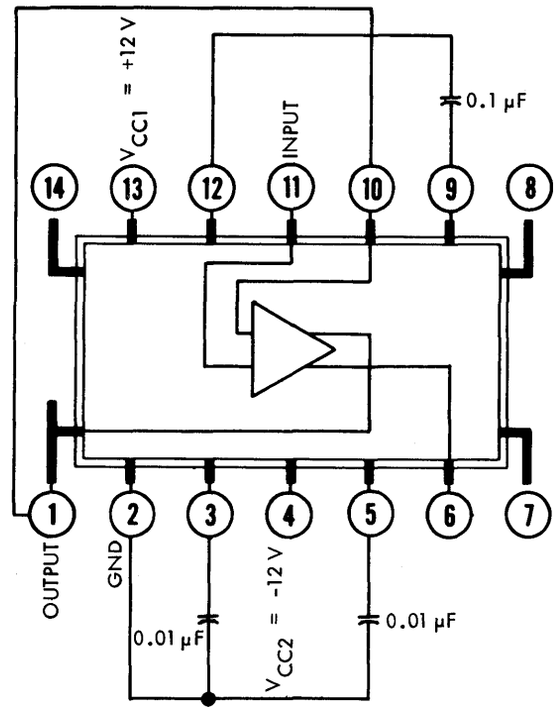


FIGURE 12

TYPE SN526 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN526
BULLETIN NO. DL-S 669273, NOVEMBER 1966

A SERIES 52 AMPLIFIER

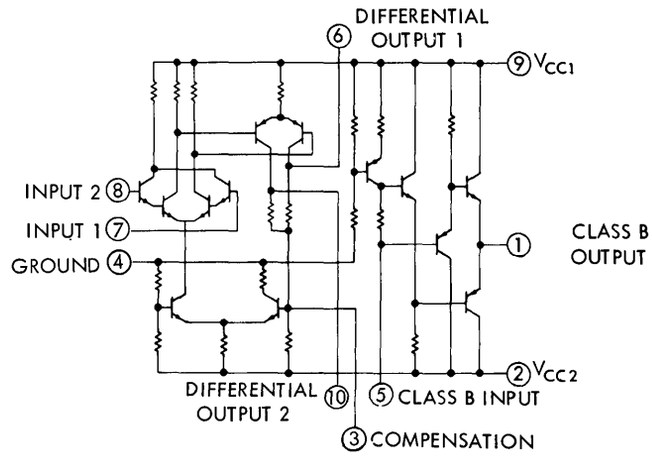
featuring

- **Minimum Z_{in} ... 350 kΩ**
- **Differential or Class B Power Output**

description

The SN526 semiconductor-network amplifier features Darlington high-impedance differential-input stages and a Class B output power amplifier with high-voltage- and current-range capabilities. Common-mode input signals are rejected by use of common-mode feedback to the input amplifier.

The SN526, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and less weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



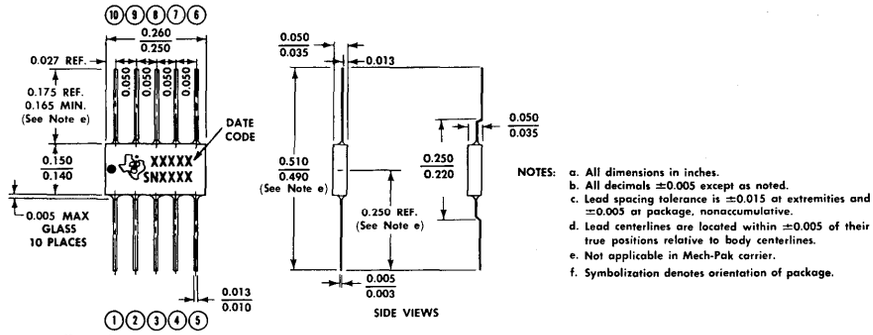
SCHEMATIC

mechanical data

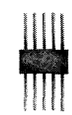
The SN526 is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15‡ glass sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN526 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

ORDERING INSTRUCTIONS

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5



NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.



†Patented by Texas Instruments.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE SN526
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . 10 V
Common-Mode Input Voltage . . . . . ±12 V
Continuous Total Power Dissipation at (or below) 100°C Case Temperature (See Note 2) . . . 250 mW
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. Derate linearly above 100°C case temperature at a rate of 5 mW/deg.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS §	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			3	17	mV
		T_A = −55°C to 125°C			20	mV
V_{CMO}	Common-mode output offset voltage			220	750	mV
I_{in}	Input current	T_A = 125°C		9	100	nA
				50	300	nA
		T_A = −55°C		230	1000	nA
I_{DI}	Differential-input offset current	T_A = 125°C		1.5	50	nA
				6	100	nA
		T_A = −55°C		60	500	nA
V_{OM}	Maximum peak-to-peak output voltage	Class B output (See Note 3) R_L = 600 Ω, f = 1 kHz		11.7		V
		Class B output (See Note 3) R_L = 600 Ω, f = 1 kHz T_A = −55°C to 125°C	10			V
V_{CMIM}	Maximum common-mode input voltage			±7		V
A_{VS}	Small-signal single-ended voltage gain	f = 1 kHz	800	1200		
		f = 1 kHz, T_A = −55°C to 125°C	630			
A_{VCMS}	Small-signal single-ended common-mode voltage gain	f = 1 kHz		0.14	0.5	
CMRR	Small-signal common-mode rejection ratio	f = 1 kHz		77		dB
BW	Bandwidth (−3 dB)			120		kHz
z_{in}	Input impedance	f = 1 kHz	0.35	1		MΩ
P_T	Total power dissipation			132	190	mW

§ Unless otherwise noted, test conditions include: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied, no external load, and a 0.05-μF capacitor between pin (3) and ground. All parameters except V_{OM} are measured with pin (5) grounded and pin (1) open.

Note 3: Pin (5) is connected to pin (6) or pin (10).

letter symbol and parameter definitions

V_{DI} That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

V_{CMO} That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} The current into either input of the amplifier.

I_{DI} The difference in the currents into the two input terminals when the output is balanced.

V_{OM} The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

z_{in} The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

z_{out} The impedance between either output terminal and ground when the output is balanced.

compensation requirements

External capacitance must be connected between pin (3) and ground to stabilize the amplifier if symmetrical compensation is not used on pins (6) and (10).

TYPICAL CHARACTERISTICS §

COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

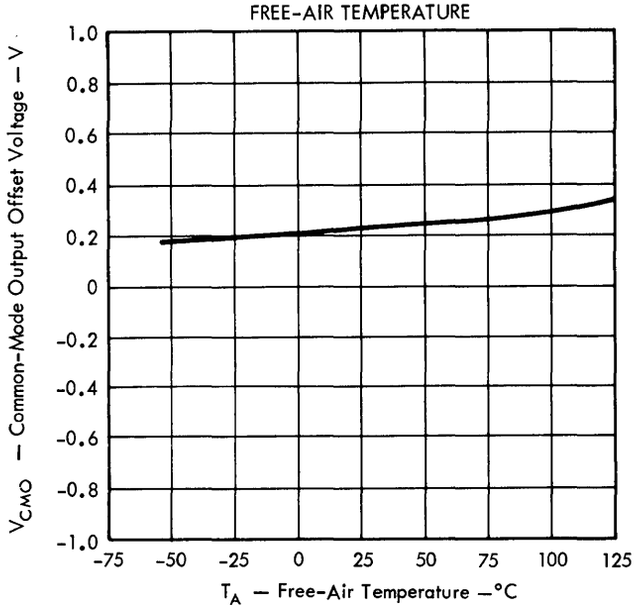


FIGURE 1

COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
SUPPLY VOLTAGE

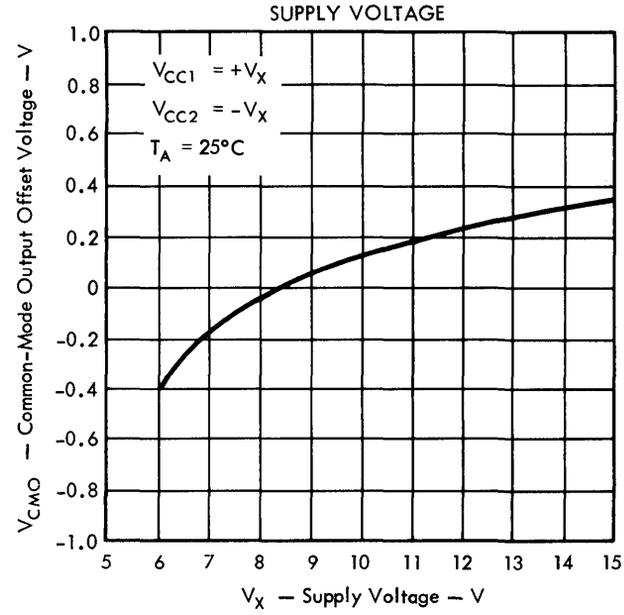


FIGURE 2

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

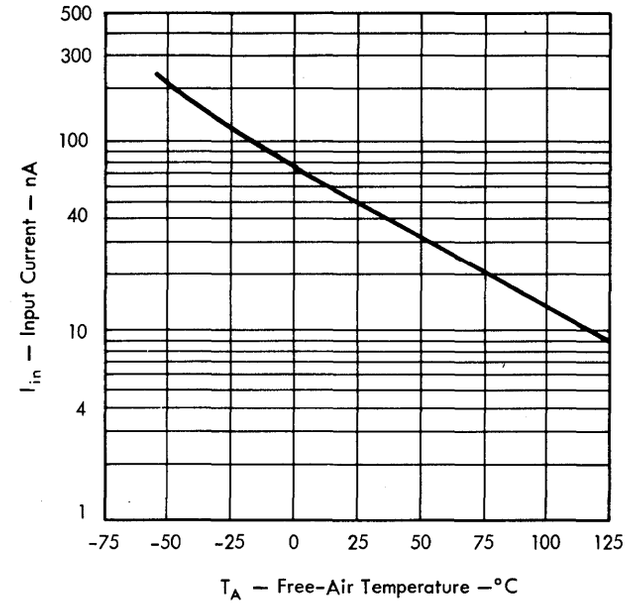


FIGURE 3

DIFFERENTIAL-INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

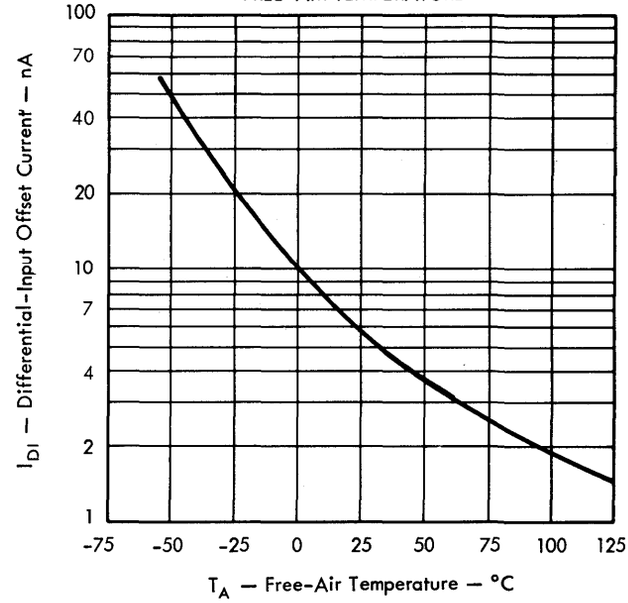


FIGURE 4

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, and a 0.05-μF capacitor between pin (3) and ground. All parameters except V_{OM} are measured with pin (5) grounded and pin (1) open.

TYPICAL CHARACTERISTICS §

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

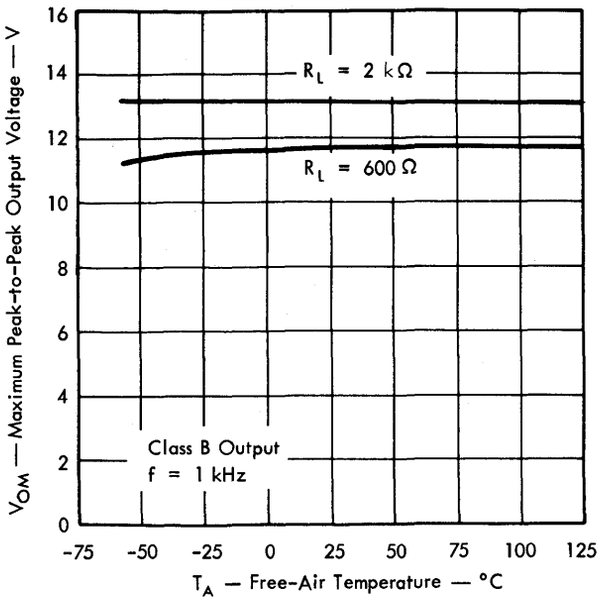


FIGURE 5

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

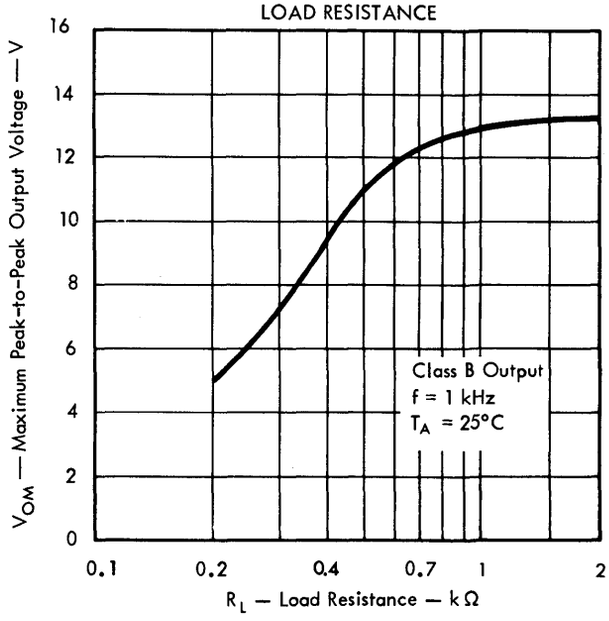


FIGURE 6

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

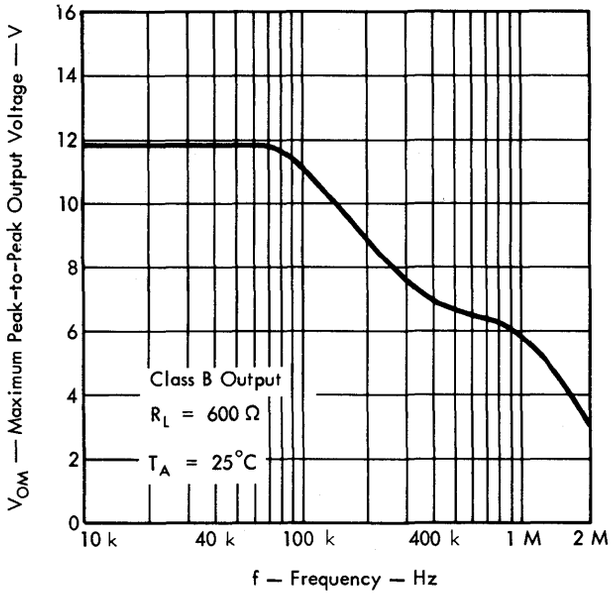
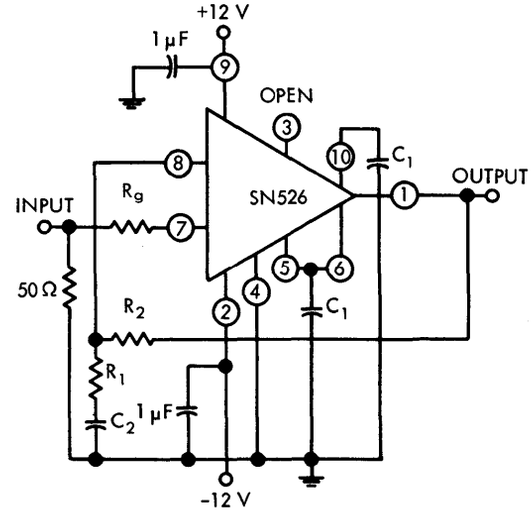


FIGURE 7



FREQUENCY RESPONSE TEST CIRCUIT

FIGURE 8

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, and a 0.05-μF capacitor between pin (3) and ground. All parameters except V_{OM} are measured with pin (5) grounded and pin (1) open.

TYPICAL CHARACTERISTICS §

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

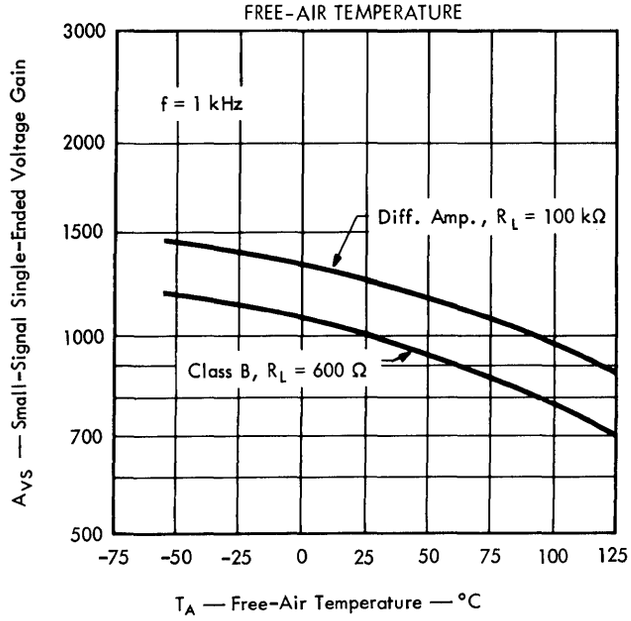


FIGURE 9

SMALL-SIGNAL SINGLE-ENDED VOLTAGE GAIN
vs
SUPPLY VOLTAGE

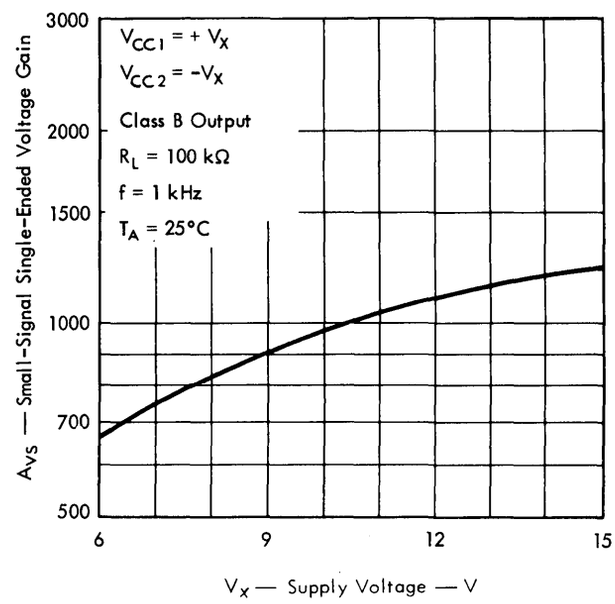


FIGURE 10

VOLTAGE GAIN
vs
FREQUENCY

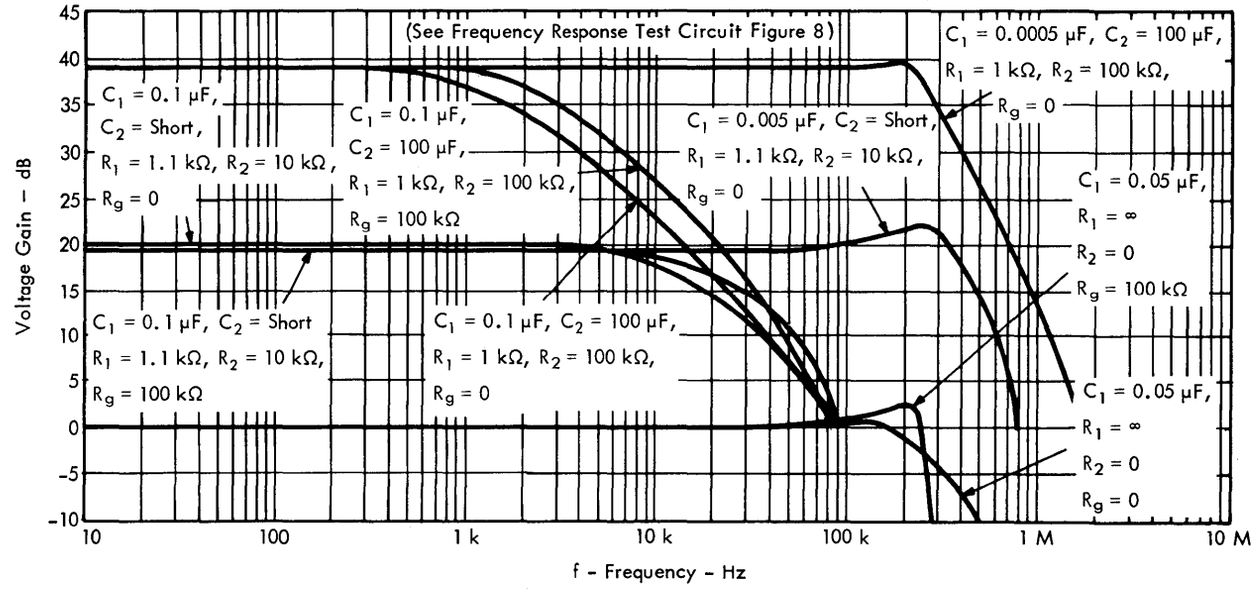


FIGURE 11

§ Unless otherwise noted, test conditions include: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied, no external load, and a 0.05-μF capacitor between pin (3) and ground. All parameters except V_{OM} are measured with pin (5) grounded and pin (1) open.

TYPICAL CHARACTERISTICS §

SMALL-SIGNAL COMMON-MODE SINGLE-ENDED VOLTAGE GAIN vs FREE-AIR TEMPERATURE

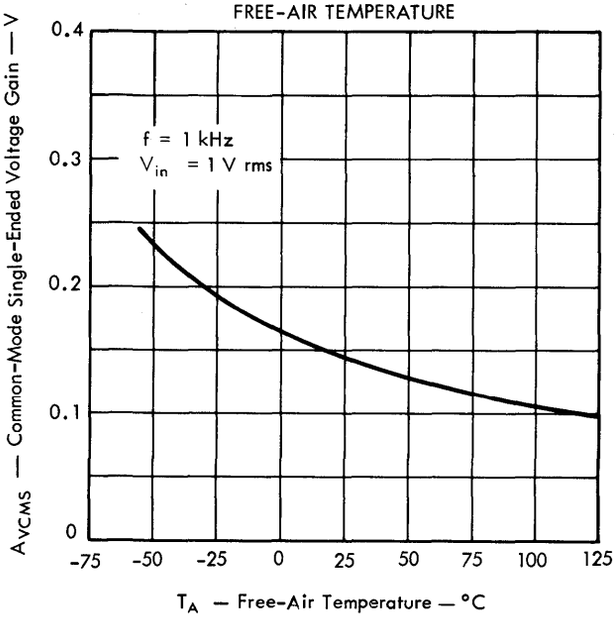


FIGURE 12

TOTAL POWER DISSIPATION vs SUPPLY VOLTAGE

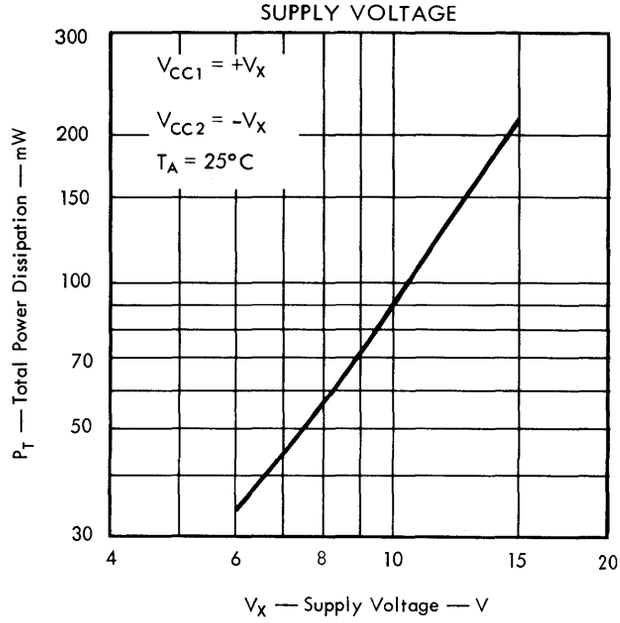


FIGURE 13

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

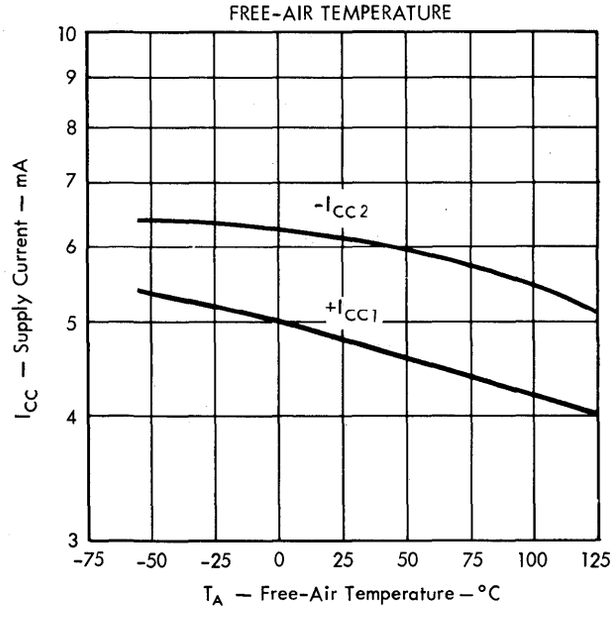


FIGURE 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

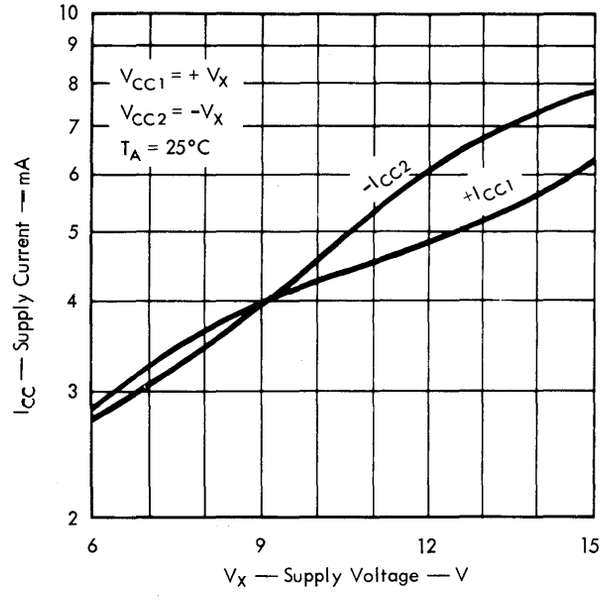


FIGURE 14

§ Unless otherwise noted, test conditions include: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied, no external load, and a 0.05-μF capacitor between pin (3) and ground. All parameters except V_{OM} are measured with pin (5) grounded and pin (1) open.

TYPE SN5500
BULLETIN NO. DL-S 657487, MARCH 1965
REVISED AUGUST 1966

A SERIES 55 HIGH-SPEED SEMICONDUCTOR NETWORK SENSE AMPLIFIER FOR APPLICATION IN MAGNETIC CORE MEMORIES FOR

• DIGITAL COMPUTER SYSTEMS • DATA HANDLING SYSTEMS • CONTROL SYSTEMS

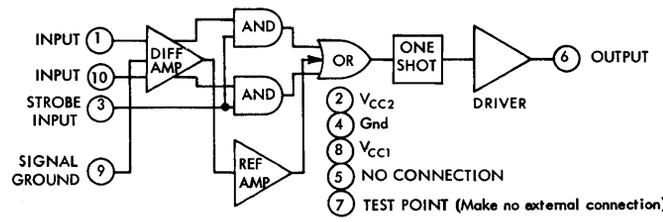
description

The SN5500 sense amplifier detects bipolar (positive or negative) differential-input signals from a magnetic core memory and provides the interface circuitry between the memory unit and the logic circuitry. In performing this function the sense amplifier accepts low-level pulses originating in the memory, discriminates between those representing logical 1 and those representing logical 0, and converts them to logic levels compatible with standard integrated logic circuitry.

The SN5500 is an amplitude-discriminating sense amplifier incorporating a threshold circuit with a narrow region of uncertainty. Signals of either polarity are accepted. A strobe input is provided so the threshold detector can be enabled when the signal-to-noise ratio is a maximum during the system read cycle and inhibited during the write cycle. It is recommended for core memory application with cycle times as low as two microseconds.

An internal one-shot pulse amplifier provides a standard-width negative-going output pulse when triggered by the threshold detector.

FUNCTIONAL BLOCK DIAGRAM



PULSE TRUTH TABLE

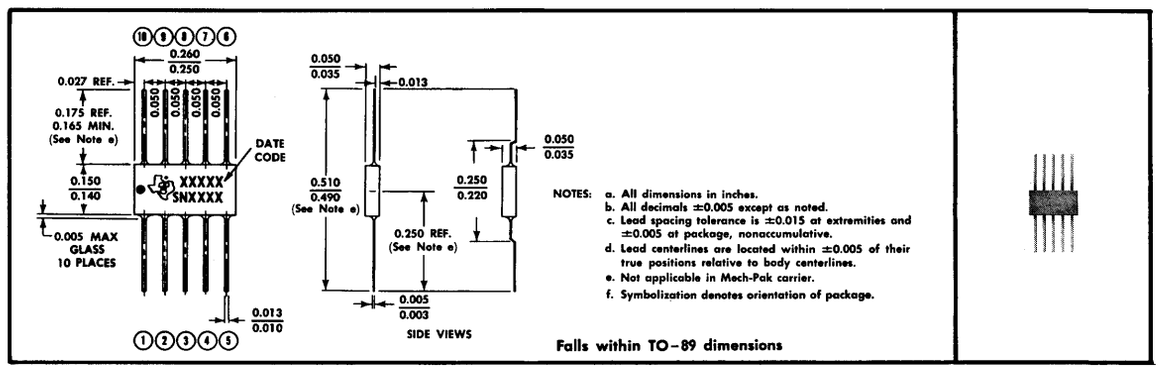
INPUT CONDITION		
INPUT VOLTAGE MAGNITUDE	STROBE INPUT	OUTPUT
$\|V_{in}\| < V_T$	Lo	V_{off}
$\|V_{in}\| < V_T$	Hi	V_{off}
$\|V_{in}\| > V_T$	Lo	V_{off}
$\|V_{in}\| > V_T$	Hi	V_{on}
$\pm V_{CMR}$	Lo	V_{off}
$\pm V_{CMR}$	Hi	V_{off}

mechanical data

The SN5500 Semiconductor Network is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN5500 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See ordering instructions.

ORDERING INSTRUCTIONS

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5



†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

absolute maximum ratings over operating free-air temperature range

Supply Voltages: V_{CC1} . . . . . +6 v
V_{CC2} . . . . . −6 v
Strobe Input Voltage: V_{strobe} . . . . . +6 v
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

electrical characteristics, T_A = −55°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_T	Input threshold voltage level		V_{CC1} = +4.5 v, V_{CC2} = −4.5 v, V_{strobe} = +2.5 v, $t_{p(strobe)}$ = 100 nsec,	10	30	mv
		T_A = 25°C		15	19	mv
V_{TO}	Input threshold offset voltage				4	mv
R_{in}	Differential-input resistance			150	300	Ω
I_S	Strobe input current				2.5	ma
V_{off}	Off output level	I_{load} = −3 ma		2.5		v
V_{on}	On output level	I_{sink} = 3 ma			0.5	v
V_{CMR}	Common-mode rejection voltage	$t_r = t_f$ = 20 nsec, t_p = 100 nsec		1		v
P_T	Total power dissipation				200	mw

switching characteristics, T_A = −55°C to +125°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{p(out)}$	Output pulse width	V_{diff} = 50 mv	V_{CC1} = +4.5 v, V_{CC2} = −4.5 v, V_{strobe} = +2.5 v, $t_{p(strobe)}$ = 100 nsec, See Figure 4	200	800	nsec
t_{pd}	Propagation delay time	V_{diff} = 50 mv			125	nsec
t_{od}	Differential input overload recovery time	V_{diff} = 250 mv			100	nsec

letter symbol and parameter definitions

V_T — Differential input signal level just sufficient to cause an output when coincident with a strobe signal. See Figure 2.

V_{TO} — Input threshold offset to opposite polarity input signals, $|V_{T①} - V_{T⑩}|$.

R_{in} — D-c resistance between input terminals.

I_S — Strobe input current.

V_{off} — High output-voltage level while supplying specified current.

V_{on} — Low output-voltage level while sinking specified current.

V_{CMR} — Common-mode signal that will not cause an output when a strobe signal is present.

$t_{p(out)}$ — Output pulse width measured at 50-percent levels (see Figure 4).

V_{diff} — Differential voltage between input terminals.

t_{pd} — Propagation delay time from input leading edge to output leading edge measured at 50-percent levels with 50-mv input.

t_{od} — Strobe delay time after a specified differential overload noise signal required to inhibit an output.

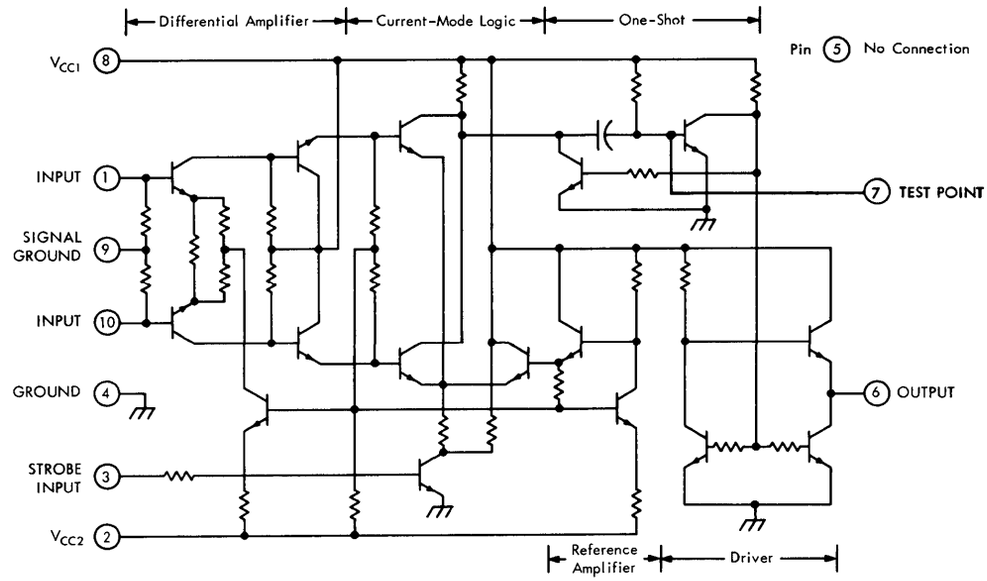


FIGURE 1 — CIRCUIT DIAGRAM

NOTES: 1. dV_1 is the core output voltage developed when a read current pulse is applied to a core in the disturbed logical 1 state.
2. $dV_{\bar{z}}$ is the core output voltage developed when a read current pulse is applied to a core in the disturbed logical 0 state.

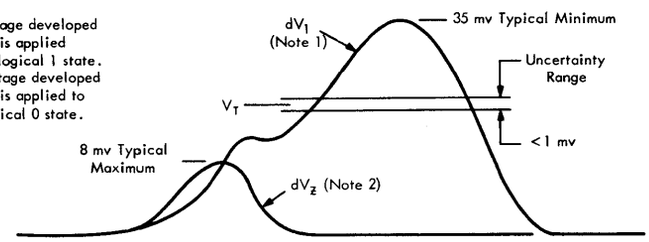


FIGURE 2 — THRESHOLD CHARACTERISTICS

(Referred to Typical Coincident-Current Memory Core dV_1 and $dV_{\bar{z}}$ Output Voltage Waveforms)

PARAMETER MEASUREMENT INFORMATION

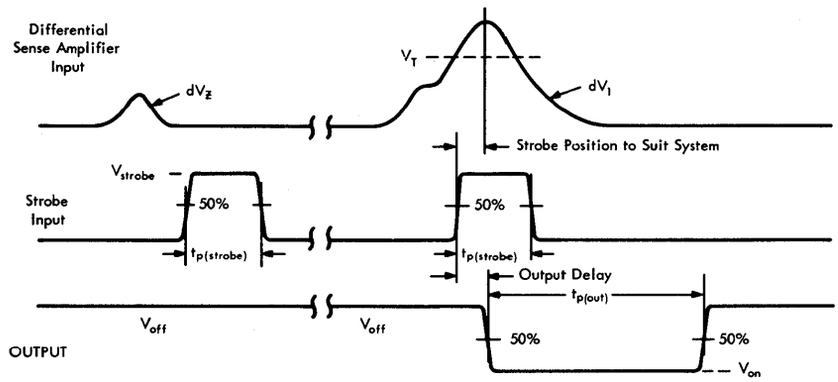


FIGURE 3 — TYPICAL SYSTEM TIMING DIAGRAM

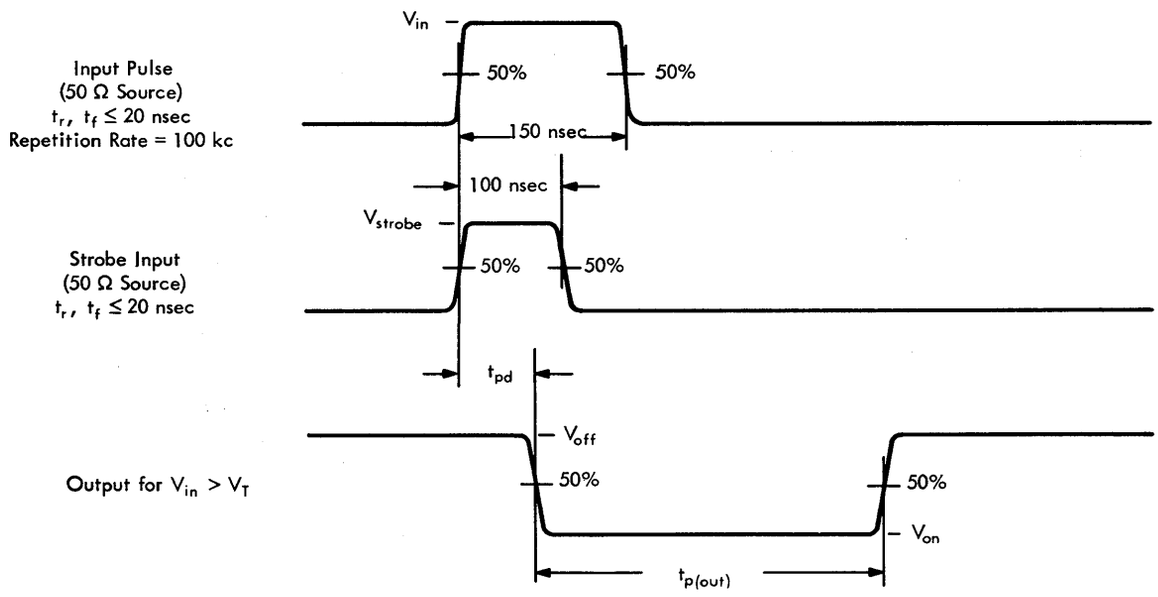


FIGURE 4 — TEST TIMING DIAGRAM FOR THRESHOLD AND SWITCHING CHARACTERISTICS

TYPES SN5510, SN5510L
WIDE-BAND VIDEO AMPLIFIERS

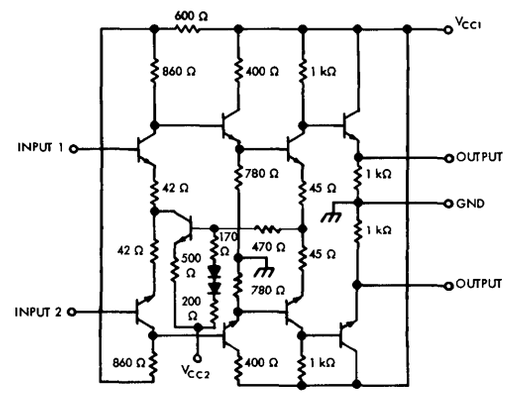
TYPES SN5510, SN5510L
BULLETIN NO. DL-S 668842, NOVEMBER 1966

SERIES 55 WIDE-BAND VIDEO AMPLIFIERS
FEATURING
Flat Frequency Response with Low Phase-Shift from DC to 40 MHz

description

Each of these wide-band video amplifiers features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit them to be used as high-frequency differential amplifiers.

Elements of the Series 55 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low-V_{CE} conditions. Circuit frequency response from dc to greater than 100 MHz is possible.



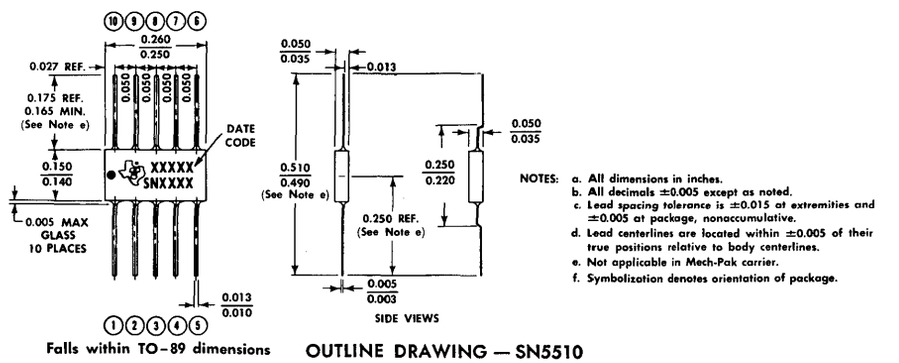
See logic symbols below for pin numbers

mechanical data

The SN5510 wide-band video amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN5510 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

SN5510 ORDERING INSTRUCTIONS

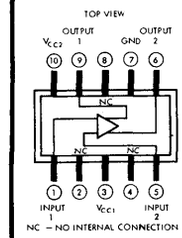
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

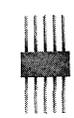


NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

Falls within TO-89 dimensions

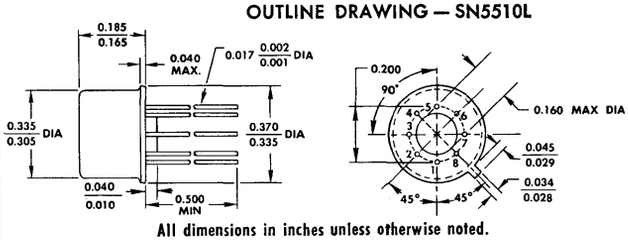
OUTLINE DRAWING — SN5510



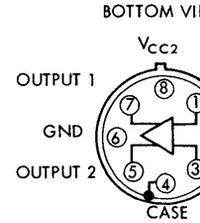


The SN5510L package outline is same as JEDEC TO-99 except for diameter of standoff.

OUTLINE DRAWING — SN5510L



All dimensions in inches unless otherwise noted.



†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1): V_{CC1} . . . . . +8 V
V_{CC2} . . . . . −8 V
Differential input voltage . . . . . 5 V
Positive input voltage (See Note 1) . . . . . V_{CC1}
Negative input voltage (See Note 1) . . . . . V_{CC2}
Operating free-air temperature ranges: SN5510 . . . . . −55°C to 70°C
SN5510L . . . . . −55°C to 100°C
Operating case temperature ranges: SN5510 . . . . . −55°C to 100°C
SN5510L . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground.

electrical characteristics, $T_A = 25°C$, $V_{CC1} = +6$ V, $V_{CC2} = -6$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Differential-output offset voltage	1			0.5	1.3	V
$V_{CMO(av)}$	Average common-mode output offset voltage	1		2.6	3.1	3.5	V
I_{in}	Input current	1			40	80	μA
I_{DI}	Differential-input offset current	1			3	20	μA
D_S	Single-ended output distortion	2	Load resistance = 5 kΩ, input distortion < 0.2%, V_{out} = 1 V rms, f = 10 kHz		1.5	5	%
$V_{\overline{N(in)}}$	Equivalent average input noise voltage	3	Single-ended, R_S = 0, f = 10 Hz to 500 kHz		5		μV
V_{CMIM}	Maximum common-mode input voltage				±1		V
A_{vs}	Small-signal voltage gain	2	Single-ended, load resistance = 5 kΩ, f = 100 kHz	75	93	110	
A_{vcm}	Common-mode-input voltage gain	4	Single-ended, load resistance = 5 kΩ, V_{in} = 0.3 V rms, f = 100 kHz		−45	--30	dB
CMRR	Common-mode rejection ratio	4	Load resistance = 5 kΩ, f = 100 kHz		85		dB
BW	Bandwidth (−3 dB)	2			40		MHz
r_{in}	Input resistance	5	f = 100 kHz		6		kΩ
C_{in}	Input capacitance	5	f = 100 kHz		7		pF
z_{out}	Output impedance	5	f = 100 kHz		35		Ω
P_T	Total power dissipation	1	No input signal, no external load		165	220	mW
t_r	Rise time	6	Single-ended, V_{in} = 5 mV		9	12	ns
t_f	Fall time	6	Single-ended, V_{in} = 5 mV		9	12	ns

TYPICAL CHARACTERISTICS §

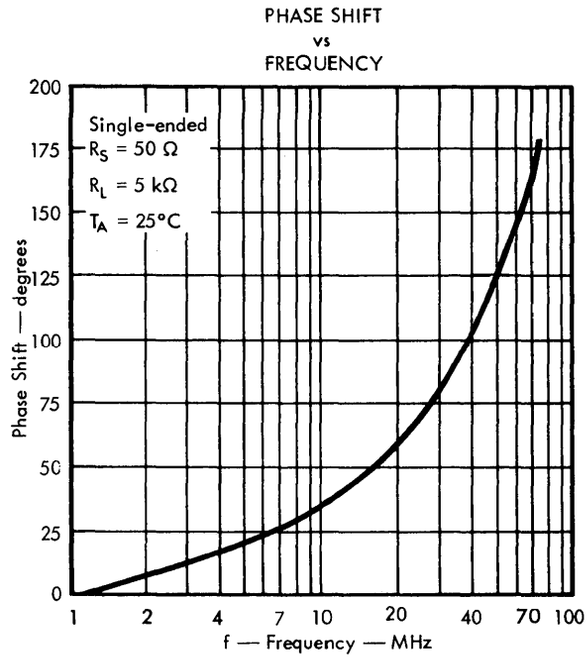


FIGURE 15

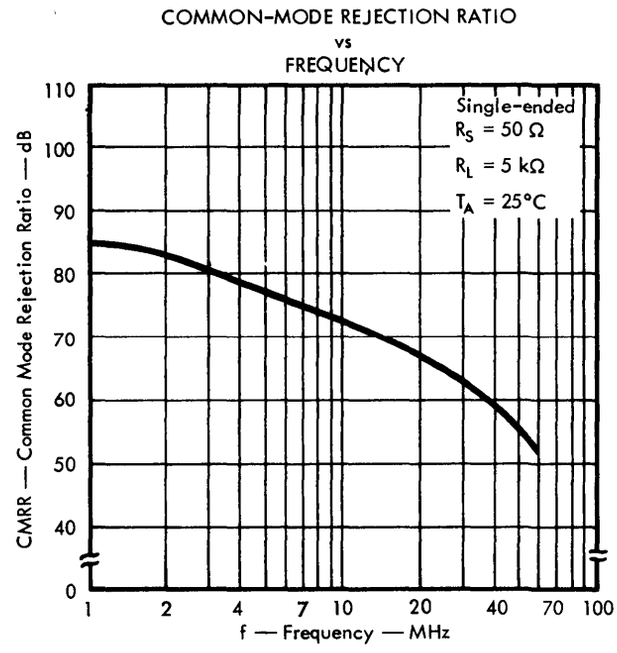


FIGURE 16

§V_{CC1} = +6 V and V_{CC2} = −6 V.

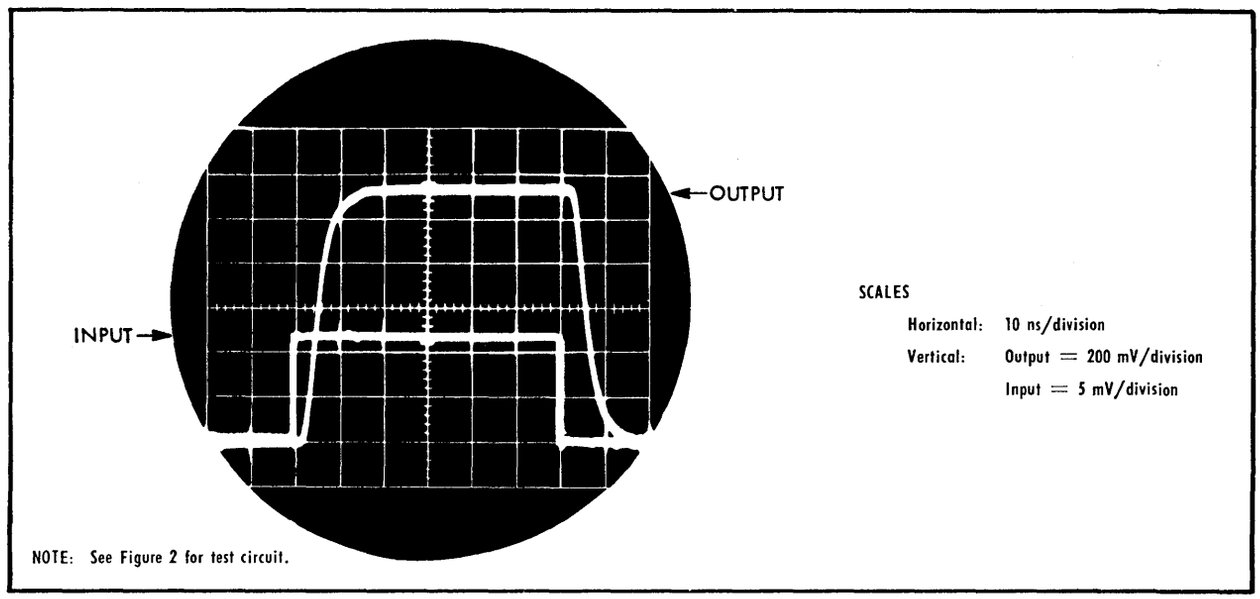


FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

TYPICAL CHARACTERISTICS §

SMALL-SIGNAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

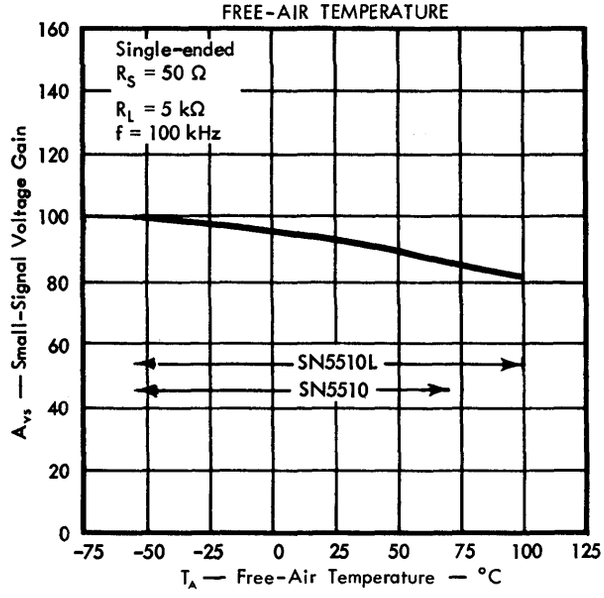


FIGURE 11

SMALL-SIGNAL VOLTAGE GAIN VARIATION
vs
SUPPLY VOLTAGE

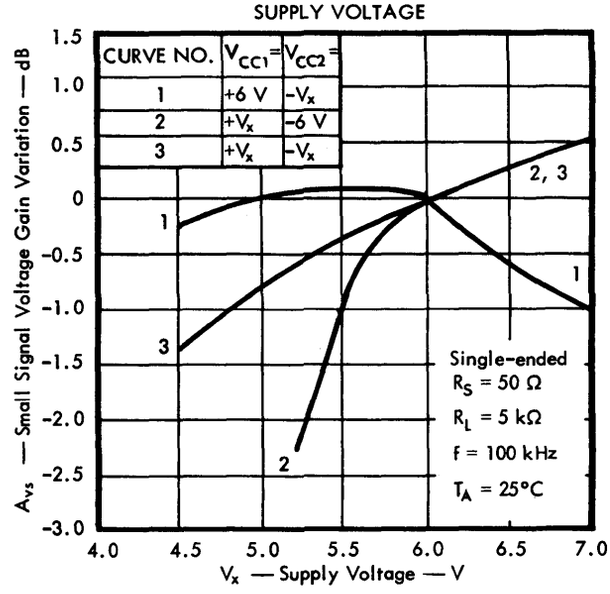


FIGURE 12

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

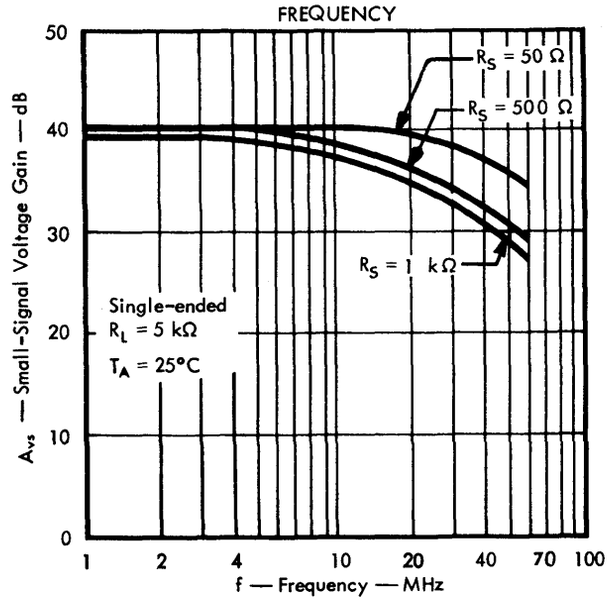


FIGURE 13

SMALL-SIGNAL VOLTAGE GAIN
vs
FREQUENCY

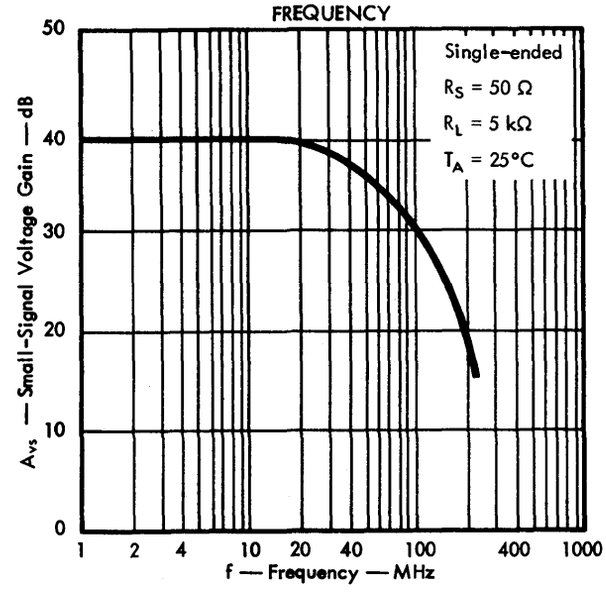


FIGURE 14

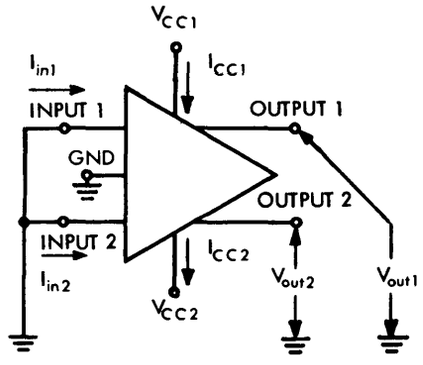
§Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

letter symbol and parameter definitions

V_{DO}	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
I_{DI}	The difference in the currents into the two input terminals.
V_{CMIM}	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

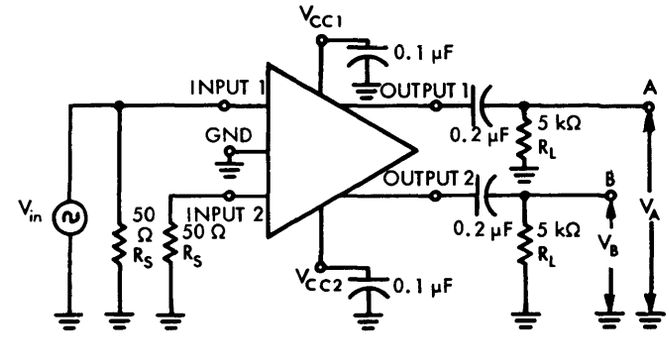
PARAMETER MEASUREMENT INFORMATION

test circuits



1. $V_{DO} = |V_{out1} - V_{out2}|$
2. $V_{CMO(av)} = \dfrac{V_{out1} + V_{out2}}{2}$
3. $I_{DI} = |I_{in1} - I_{in2}|$
4. $P_T = |V_{CC1} \bullet I_{CC1}| + |V_{CC2} \bullet I_{CC2}|$

FIGURE 1



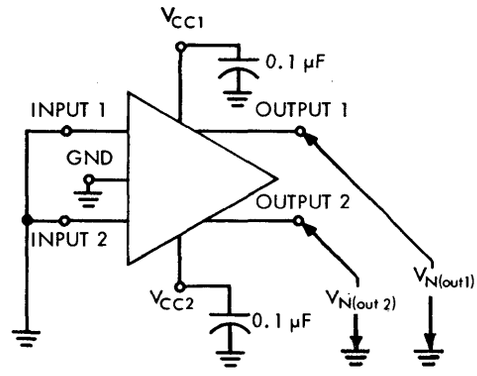
1. Single-ended output distortion is measured at A or B with V_A or V_B = 1 V rms, input distortion < 0.2%, and f = 10 kHz.
2. $A_{VS} = \left|\dfrac{V_A \text{ or } V_B}{V_{in}}\right|$

where: V_{in} = 1 mV rms and f = 100 kHz.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION

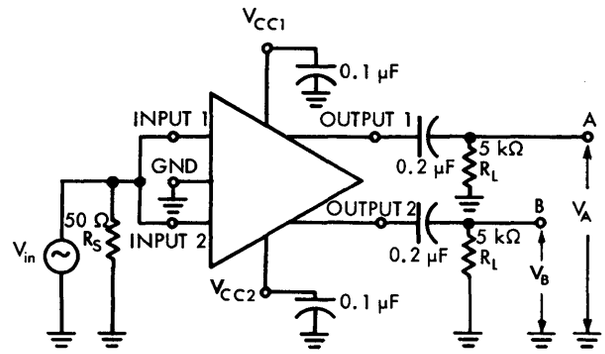
test circuits (continued)



1. $V_{\overline{N(in)}} = \dfrac{V_{\overline{N(out1)}} \text{ or } V_{\overline{N(out2)}}}{A_{VS}}$

where: $V_{\overline{N(out)}}$ = true rms broad-band noise voltage from 10 Hz to 500 kHz.

FIGURE 3



1. $A_{vcm} = 20 \text{ Log} \left| \dfrac{V_A \text{ or } V_B}{V_{in}} \right|$

where: V_{in} = 0.3 V rms and f = 100 kHz.

2. CMRR = 20 Log $A_{VS} - A_{vcm}$

FIGURE 4

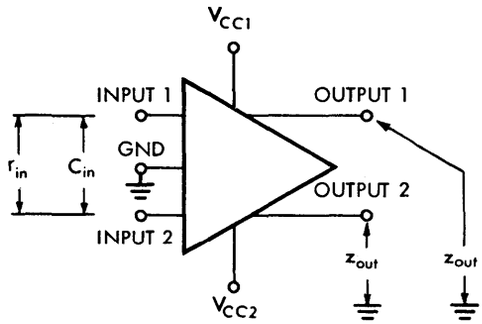
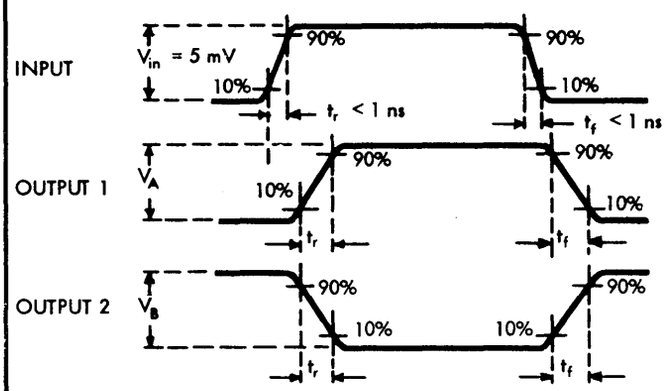


FIGURE 5



1. Test circuit is identical to that shown in Figure 2.

FIGURE 6 — t_r and t_f VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS §

AVERAGE COMMON-MODE OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

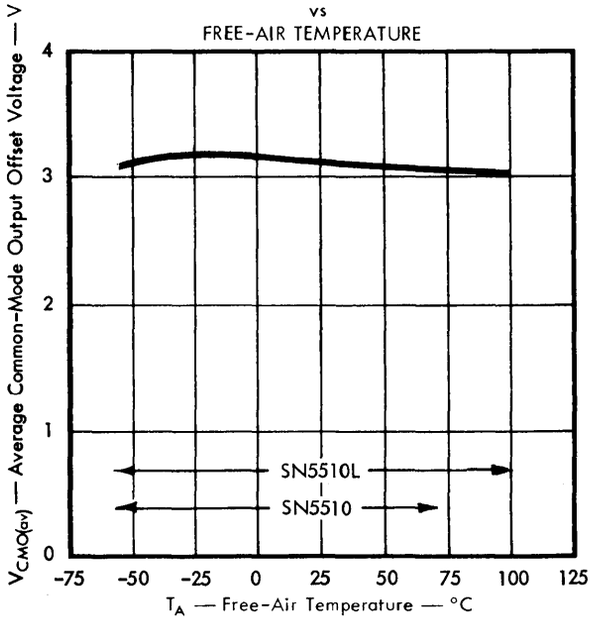


FIGURE 7

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

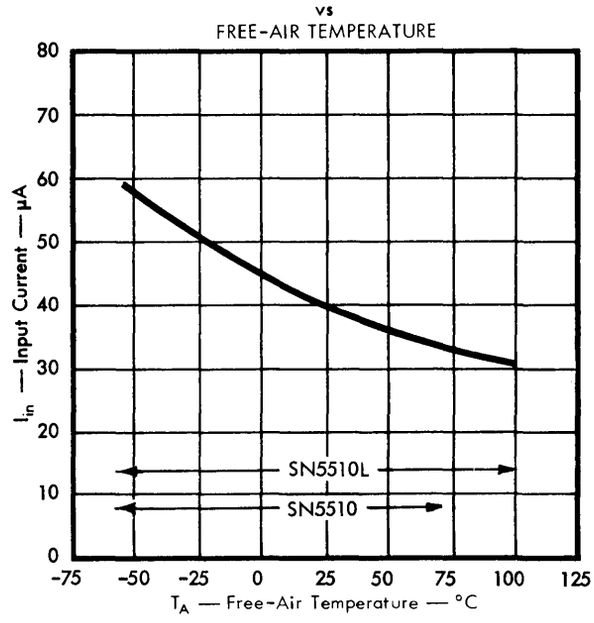


FIGURE 8

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

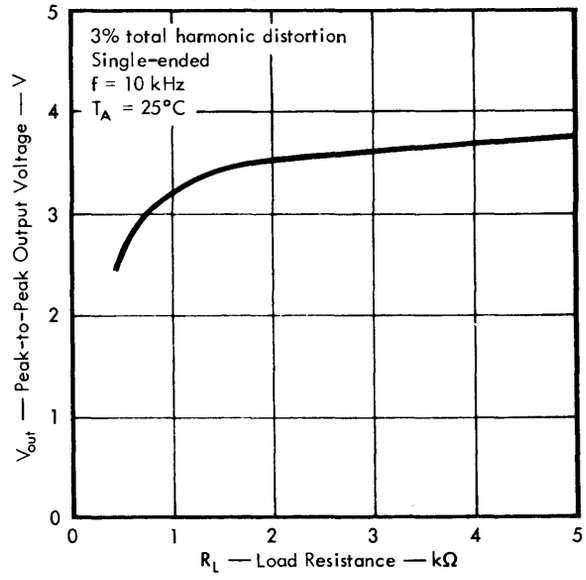


FIGURE 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

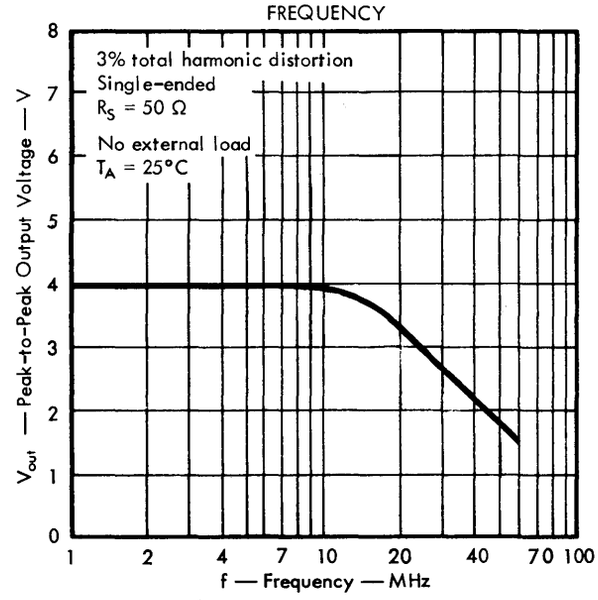


FIGURE 10

§Unless otherwise noted $V_{CC1} = +6$ V, $V_{CC2} = -6$ V.

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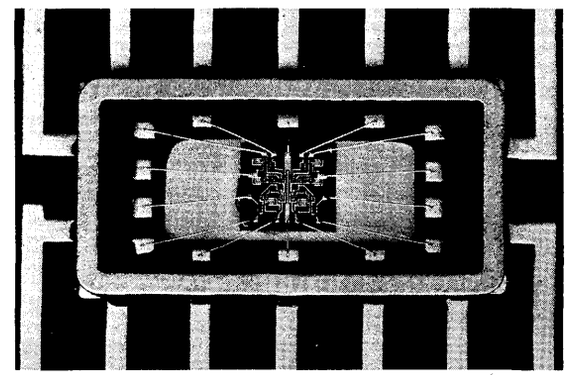
SERIES 74
BULLETIN NO. DL-S 669195, DECEMBER 1966
REPLACES BULLETIN NO. DL-S 657934, AUGUST 1965

HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS

description

Series 74 integrated circuits have been designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 70°C. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions required of general purpose industrial digital systems.



TYPE SN7400 PRIOR TO CAPPING

features

LOW SYSTEM COST

- **maximum number of circuits per package through use of 14-lead package**

OPTIMUM CIRCUIT PERFORMANCE

- **high speed — typical gate propagation delay time of 13 ns**
- **high d-c noise margin — typically one volt**
- **low output impedance provides low a-c noise susceptibility**
- **waveform integrity over full range of loading and temperature conditions**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **full fan-out of 10**

CONTENTS

†Patented by Texas Instruments.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

design characteristics

Series 74 digital integrated circuits effect an optimization between saturated logic circuitry and monolithic semiconductor technology yielding high performance at lowest cost. In discrete-component circuitry maximum use is made of lower cost components (diodes and resistors) instead of the higher priced transistors. However, in monolithic circuitry it costs no more to build transistors than diodes or resistors. Therefore, in Series 74, transistors are used to buffer the fluctuations in currents that occur as resistor values change. Also, the Series 74 multiple-emitter transistor can easily be built in a monolithic bar to eliminate the need for conventional input diodes.

circuit operation

The transistor-transistor logic (TTL) used in Series 74 is analogous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode D_3. If inputs A and B are raised to a high voltage, drive current will then pass through diode D_3.

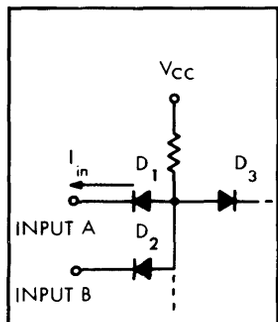


Figure A
Diode AND Logic

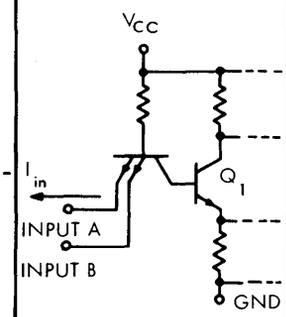


Figure B
Series 74 AND Logic

In Series 74 TTL circuitry, the multiple-emitter transistor performs the same function as the diodes in DTL (see figure B). However, the transistor action of the multiple-emitter transistor causes transistor Q_1 to turn-off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

Although one-volt d-c noise margins are typical for Series 74 circuits, an absolute guarantee of 400 millivolts is assured for every unit. This is accomplished by testing each output and input as shown in figures C and D.

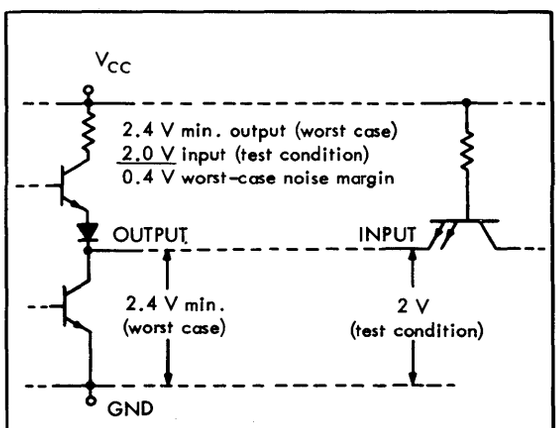


Figure C — Logical 1 Noise Margin

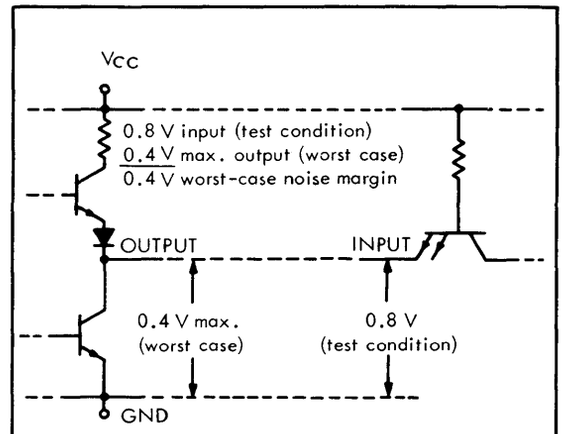


Figure D — Logical 0 Noise Margin

Each output is tested to ensure that the logical 1 output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest V_{CC}, and 0.8 volt on the input — 400 mV more than the logical 0 maximum.

Each output is tested to ensure that the logical 0 output voltage will not exceed 0.4 volt. This is done with full fan-out, lowest V_{CC}, and 2 volts on the input — 400 mV less than the logical 1 minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition, the threshold voltage of the Series 74 circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in figure E.

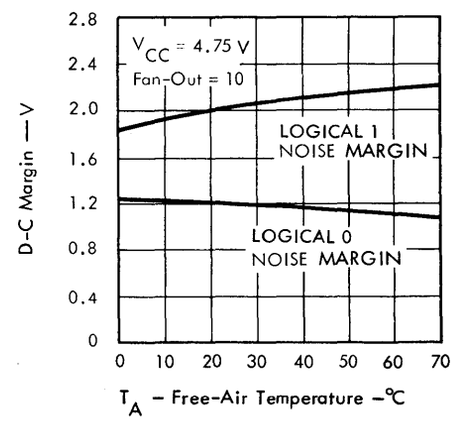
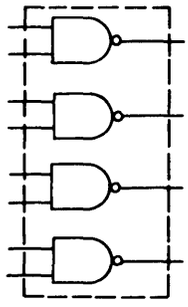


Figure E — Typical D-C Margin vs Temperature

Another important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12 Ω and logical 1 output impedance is 70 Ω. This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve waveshape integrity.

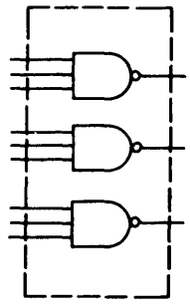
standard line summary

SN7400 See Page 5005



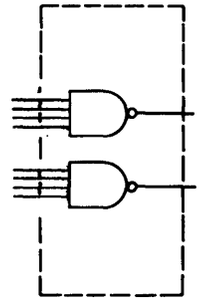
QUADRUPLE 2-INPUT
POSITIVE NAND GATE

SN7410 See Page 5006



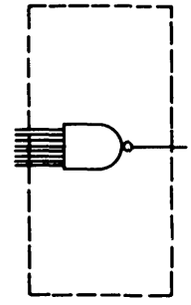
TRIPLE 3-INPUT
POSITIVE NAND GATE

SN7420 See Page 5007



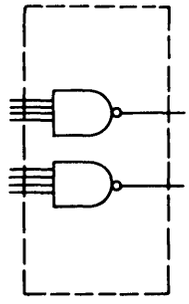
DUAL 4-INPUT
POSITIVE NAND GATE

SN7430 See Page 5008



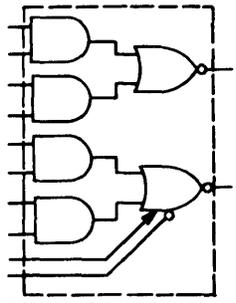
8-INPUT
POSITIVE NAND GATE

SN7440 See Page 5009



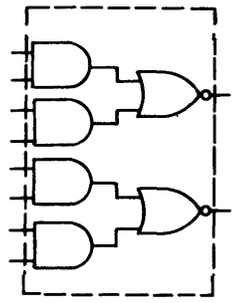
DUAL 4-INPUT
POSITIVE NAND BUFFER

SN7450 See Page 5010



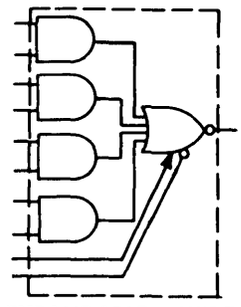
EXPANDABLE DUAL
2-WIDE 2-INPUT
AND-OR-INVERT GATE

SN7451 See Page 5010



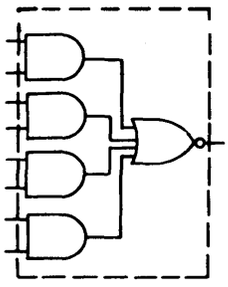
DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATE

SN7453 See Page 5012



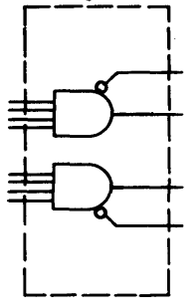
EXPANDABLE 4-WIDE
2-INPUT
AND-OR-INVERT GATE

SN7454 See Page 5012



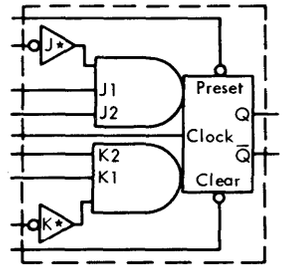
4-WIDE 2-INPUT
AND-OR-INVERT GATE

SN7460 See Page 5014



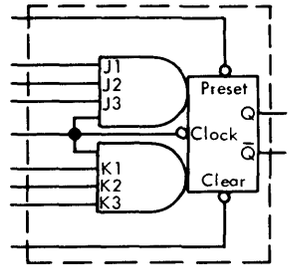
DUAL 4-INPUT EXPANDER

SN7470 See Page 5015



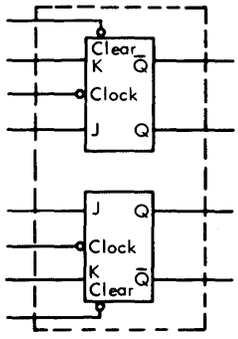
J-K FLIP-FLOP

SN7472 See Page 5018



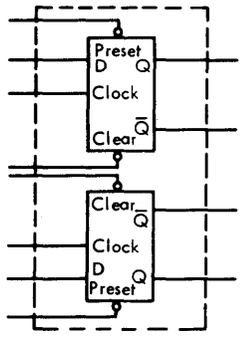
J-K MASTER-SLAVE
FLIP-FLOP

SN7473 See Page 5021



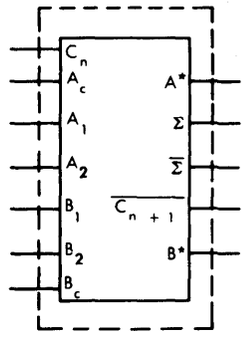
DUAL J-K
MASTER-SLAVE FLIP-FLOP

SN7474 See Page 5024



DUAL D-TYPE
EDGE-TRIGGERED FLIP-FLOP

SN7480 See Page 5027



GATED FULL ADDER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input-current requirements

Input-current requirements reflect worst-case conditions for T_A = 0°C to 70°C and V_{CC} = 4.75 V to 5.25 V. Each input of the multiple-emitter input transistor requires that no more than −1.6 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is −1.6 mA maximum. Each input requires current into the input at a logical 1 voltage level. This current is 40 μA maximum for each emitter input. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads (N = 10). The buffer gate is capable of sinking current or supplying current to 30 loads (N = 30). The carry output (C_{n+1}) of the full adder is capable of driving 5 loads (N = 5) and the A★ and B★ nodes may be used to drive 3 loads (N = 3). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

unused inputs

For optimum switching times, unused gate inputs should be tied to a positive voltage source of 2.4 V to 5.5 V. This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Supply voltage V_{CC}, if regulated to 5.5 V maximum, may be used.

If the supply voltage V_{CC} cannot be limited to 5.5 V the following alternatives are recommended:

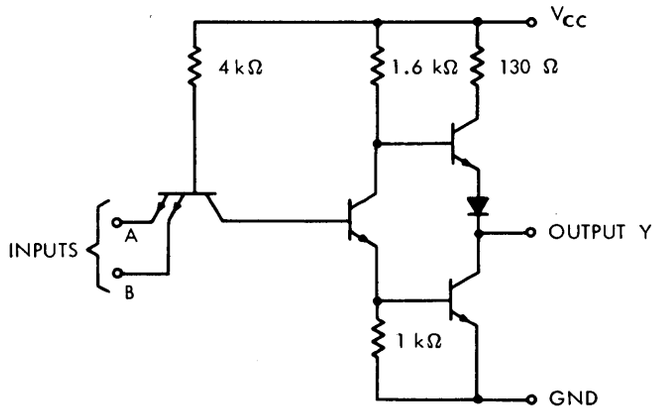
a. Connect unused gate inputs to an independent supply voltage source of 2.4 V to 5.5 V.

b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded.

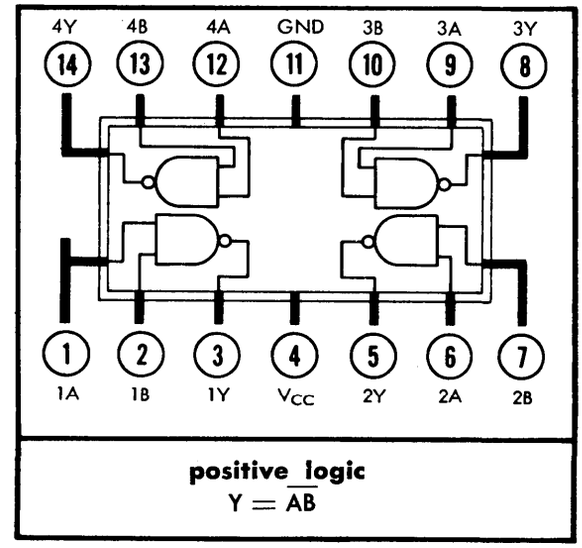
In all cases, unused J★ and K★ inputs of the SN7470 must be connected to ground.

Instructions for terminating unused inputs of the SN7480 are provided in the applications shown for that device.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V,		−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1‡		mA

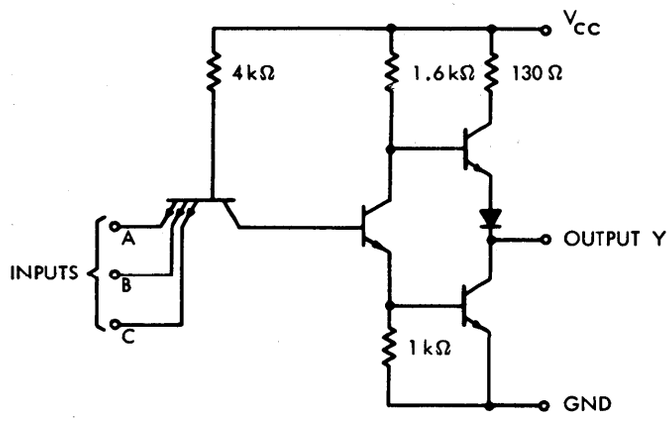
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_L = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_L = 15 pF		18	29	ns

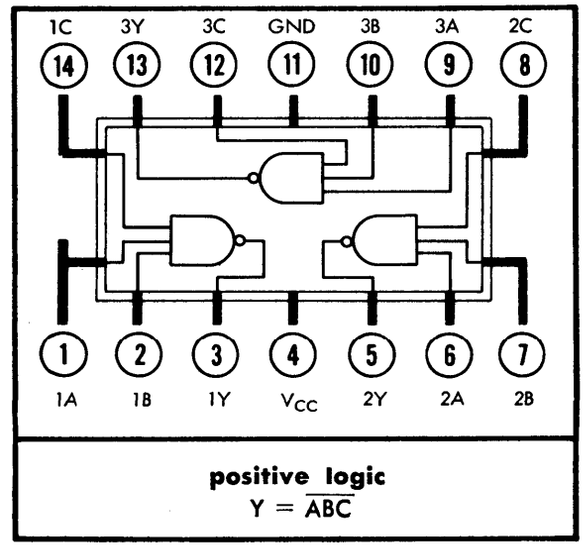
†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPE SN7410
TRIPLE 3-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to $70°C$

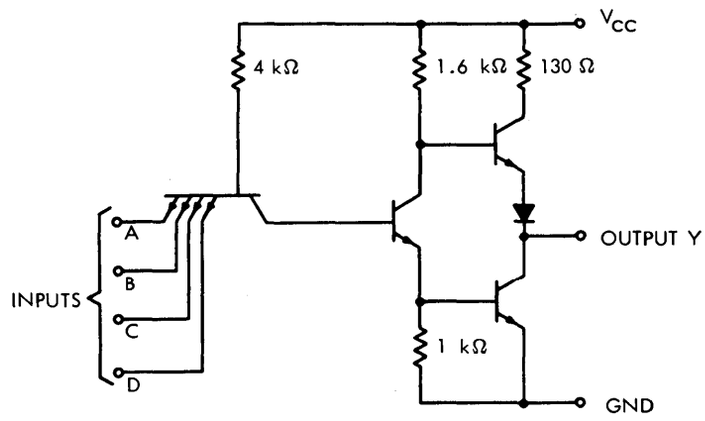
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V		−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

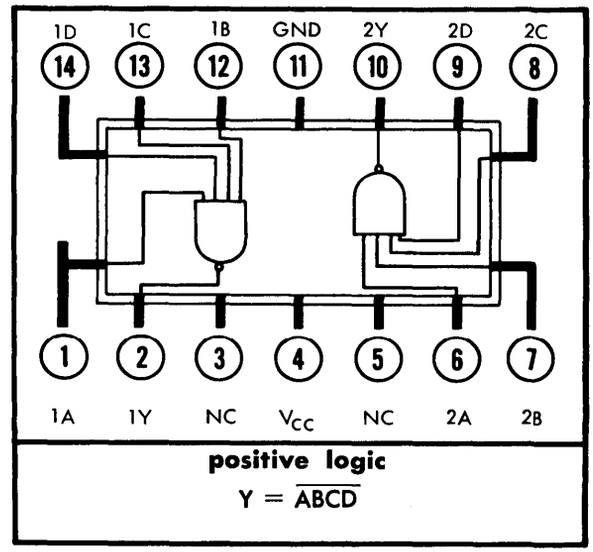
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V		−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1‡		mA

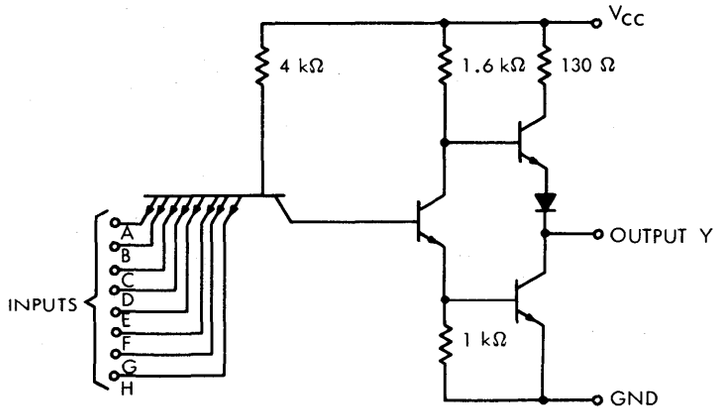
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_l = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_l = 15 pF		18	29	ns

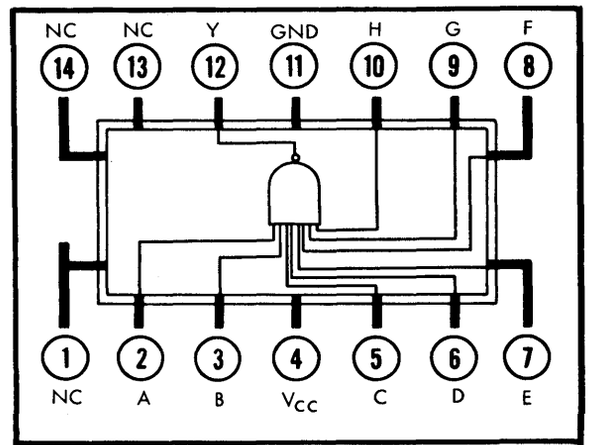
†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPE SN7430
8-INPUT POSITIVE NAND GATE

schematic



Component values shown are nominal.



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

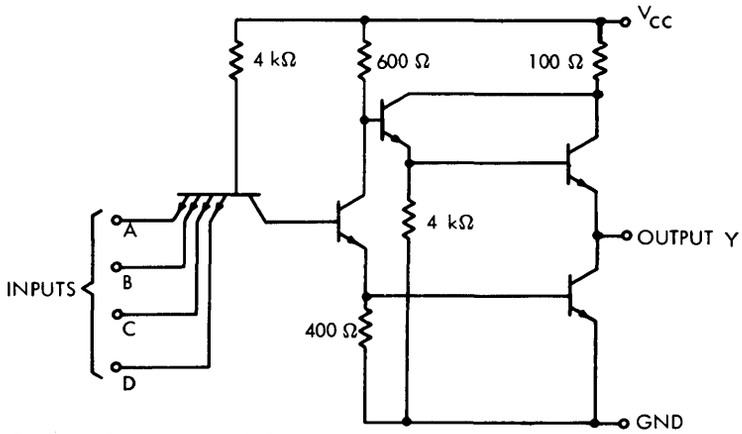
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V, $V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V, $V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, V_{in} = 0.8 V, I_{load} = −400 μA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, V_{in} = 2 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current	5	V_{CC} = 5.25 V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = 5 V, V_{in} = 5 V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = 5 V, V_{in} = 0		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

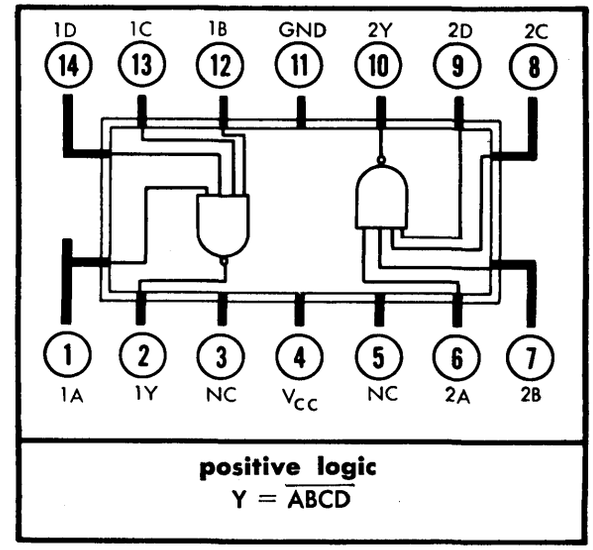
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_L = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_L = 15 pF		18	29	ns

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each gate)



Component values shown are nominal.



positive logic
$Y = \overline{ABCD}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 30

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V, $V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V, $V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, V_{in} = 0.8 V, I_{load} = −1.2 mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, V_{in} = 2 V, I_{sink} = 48 mA		0.28‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V	−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V, V_{in} = 5 V		8.6‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V, V_{in} = 0		2 ‡		mA

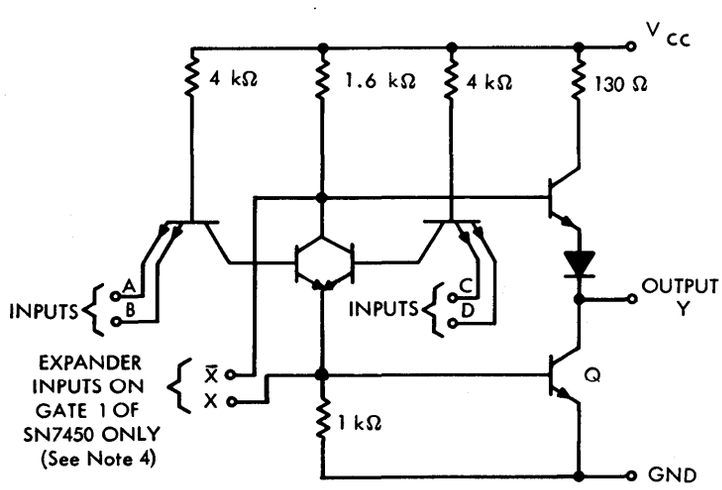
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 30

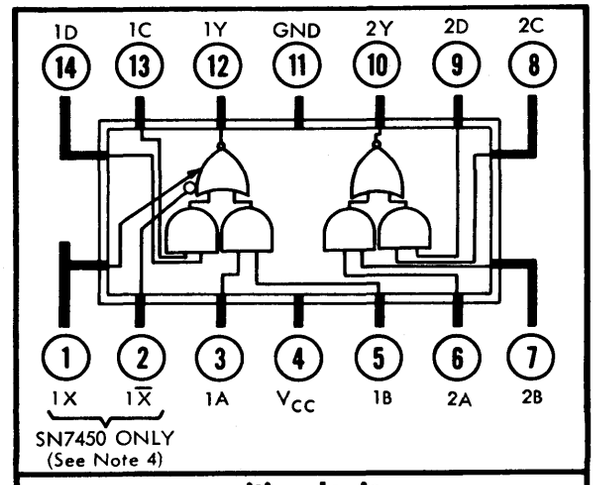
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_L = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_L = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

TYPES SN7450, SN7451
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

schematic (each gate)





positive logic

$Y = (AB) + (CD) + (X \text{ of SN7450})$

$(SN7450\ X) = ABCD \text{ from SN7460}$

NOTES: 1. Component values shown are nominal.
2. Both SN7450 expander inputs are used simultaneously for expanding with the SN7460.
3. If expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN7451.
5. A total of four expander gates may be connected to the SN7450 expander.

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, $T_A = 0°C$ to $70°C$, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	$V_{CC} = 5.25$ V, $V_{in} = 0$			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	11	$V_{CC} = 5.25$ V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	12	$V_{CC} = 5$ V, $V_{in} = 5$ V		3.7‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	13	$V_{CC} = 5$ V, $V_{in} = 0$		2‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

electrical characteristics (SN7450 only) using expander inputs, $T_A = 0°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.75$ V, $V_I = 0.4$ V, $I_{sink} = 16$ mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.62$ mA, $R_1 = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu$A, $I_1 = 0.15$ mA, $I_2 = -0.15$ mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.43$ mA, $R_1 = 130\ \Omega$		0.22‡	0.4	V

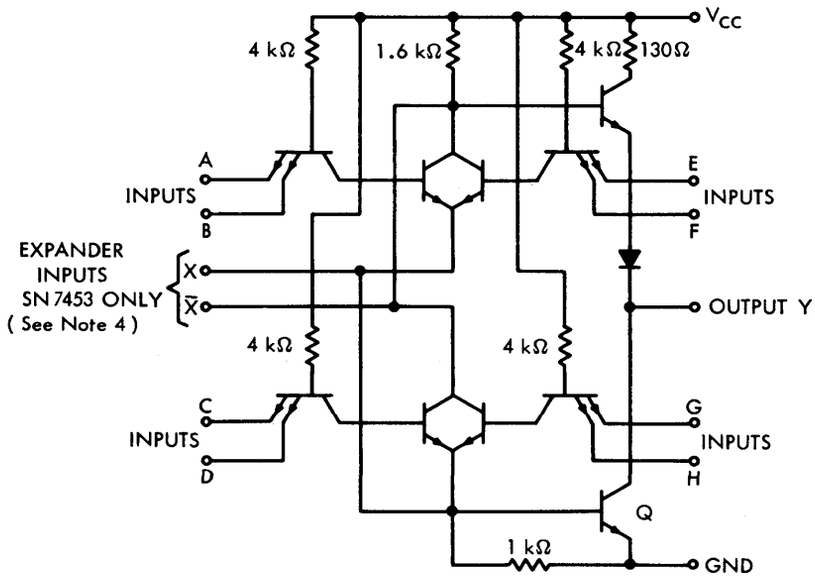
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

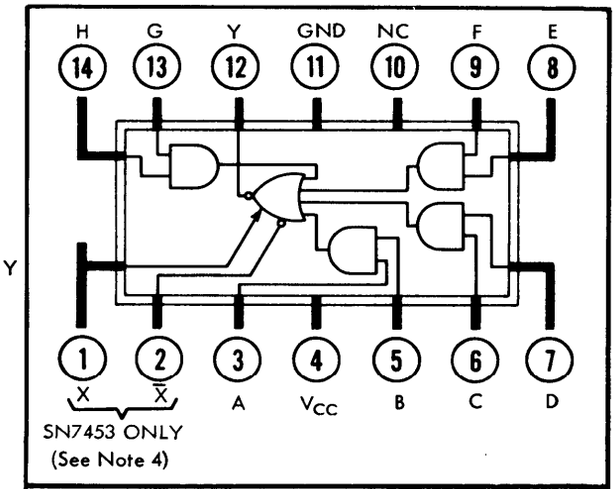
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_1 = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_1 = 15$ pF		18	29	ns

TYPES SN7453, SN7454
4-WIDE 2-INPUT AND-OR-INVERT GATES

schematic





positive logic

$$Y = \overline{(AB) + (CD) + (EF) + (GH) + (X \text{ of SN7453})}$$

(SN7453 X) = ABCD from SN7460

NOTES:
1. Component values shown are nominal.
2. Both SN7453 expander inputs are used simultaneously for expanding with the SN7460.
3. If SN7453 expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN7454.
5. A total of four expander gates may be connected to the SN7453 expander inputs.

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	V_{CC} = 4.75 V, $V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	V_{CC} = 4.75 V, $V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = 4.75 V, V_{in} = 0.8 V, I_{load} = −400 μA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = 4.75 V, V_{in} = 2 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	V_{CC} = 5.25 V, V_{in} = 0			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	11	V_{CC} = 5.25 V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current	12	V_{CC} = 5 V, V_{in} = 5 V		3.7 ‡		mA
$I_{CC(1)}$	Logical 1 level supply current	13	V_{CC} = 5 V, V_{in} = 0		2 ‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics (SN7453 only) using expander inputs, $T_A = 0°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.75$ V, $V_I = 0.4$ V, $I_{sink} = 16$ mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_I = 0.62$ mA, $R_I = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$, $I_I = 0.15$ mA, $I_2 = -0.15$ mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_I = 0.43$ mA, $R_I = 130\ \Omega$		0.22‡	0.4	V

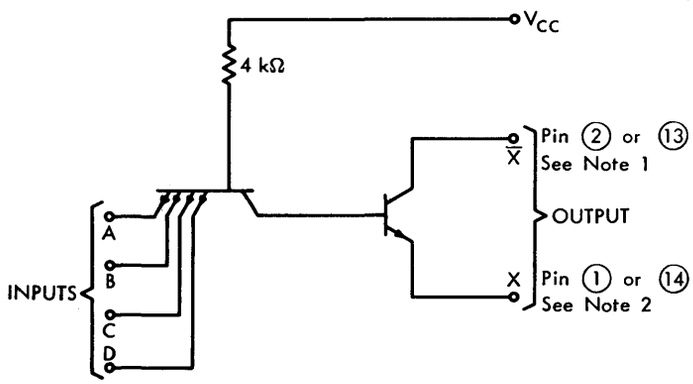
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics (SN7453 and SN7454), $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, $N = 10$

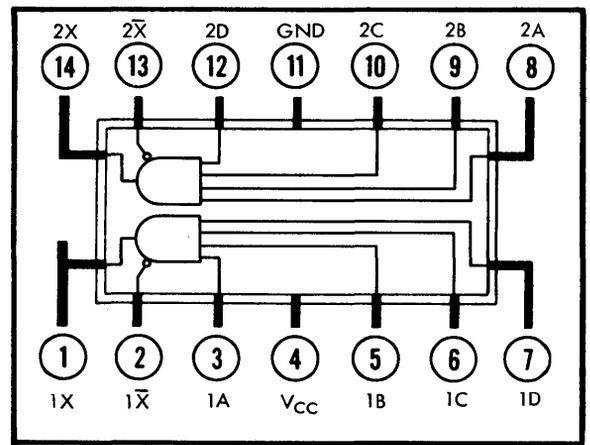
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_I = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_I = 15$ pF		18	29	ns

TYPE SN7460
DUAL 4-INPUT EXPANDER

schematic



NOTES: 1. Connect pin (2) or (13) to pin (2) of SN7450 or SN7453.
2. Connect pin (1) or (14) to pin (1) of SN7450 or SN7453.
3. Component values shown are nominal.



positive logic
X = ABCD
when connected to pins (1) and (2) of SN7450 or SN7453

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 4

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output on level	17	V_{CC} = 4.75 V, V_1 = 1 V, R = 1.1 kΩ, T_A = 0°C	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output off level current	18	V_{CC} = 4.75 V, V_1 = 4.5 V, R = 1.2 kΩ, I_{off} = 0.15 mA, T_A = 0°C			0.8	V
V_{on}	Output voltage on level	17	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V, R = 1.1 kΩ, T_A = 0°C			0.4	V
I_{off}	Output off level current	18	V_{CC} = 4.75 V, V_{in} = 0.8 V, V_1 = 4.5 V, R = 1.2 kΩ, T_A = 0°C			270	μA
I_{on}	Output on level current	19	V_{CC} = 4.75 V, V_{in} = 2 V, V_1 = 1 V	−0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	18	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	20	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{CC(on)}$	On level supply current (each gate)	21	V_{CC} = 5 V, V_{in} = 5 V, V_1 = 0.85 V		0.6 ‡		mA
$I_{CC(off)}$	Off level supply current (each gate)	21	V_{CC} = 5 V, V_{in} = 0, V_1 = 0.85 V		1 ‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

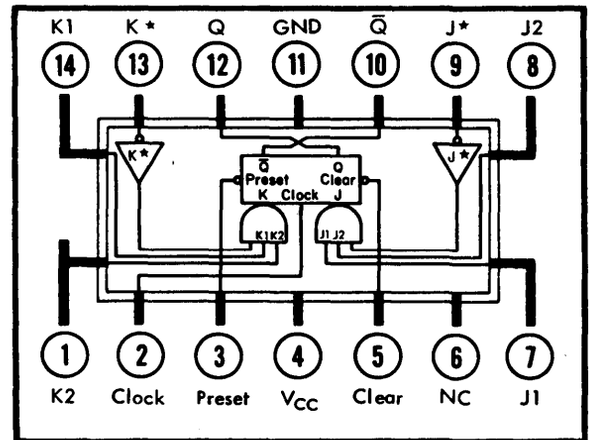
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN7450 or SN7453)	51	C_1 = 15 pF		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	51	C_1 = 15 pF		20	34	ns

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J\bigstar}$.
2. $K = K1 \cdot K2 \cdot \overline{K\bigstar}$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J★ or K★ are not used they must be grounded.



positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

The SN7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The SN7470 flip-flop is ideally suited for medium-and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10
Clock Pulse Transition Time to Logical 1 Level, $t_{t(clock)}$ (See Figure 53) . . . . . 5 to 150 ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 53) . . . . . $\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 52) . . . . . $\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 52) . . . . . $\geq$ 25 ns

electrical characteristics, T_A = 0°C to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	22	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	23	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = 4.75 V, I_{load} = −400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	23	V_{CC} = 4.75 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J★, K1, K2, K★, or clock	24	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	24	V_{CC} = 5.25 V, V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J★, K1, K2, K★, or clock	25	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	25	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	26	V_{CC} = 5.25 V, V_{in} = 0	−18		−57	mA
I_{CC}	Supply current	25	V_{CC} = 5 V, V_{in} = 5 V		13‡		mA

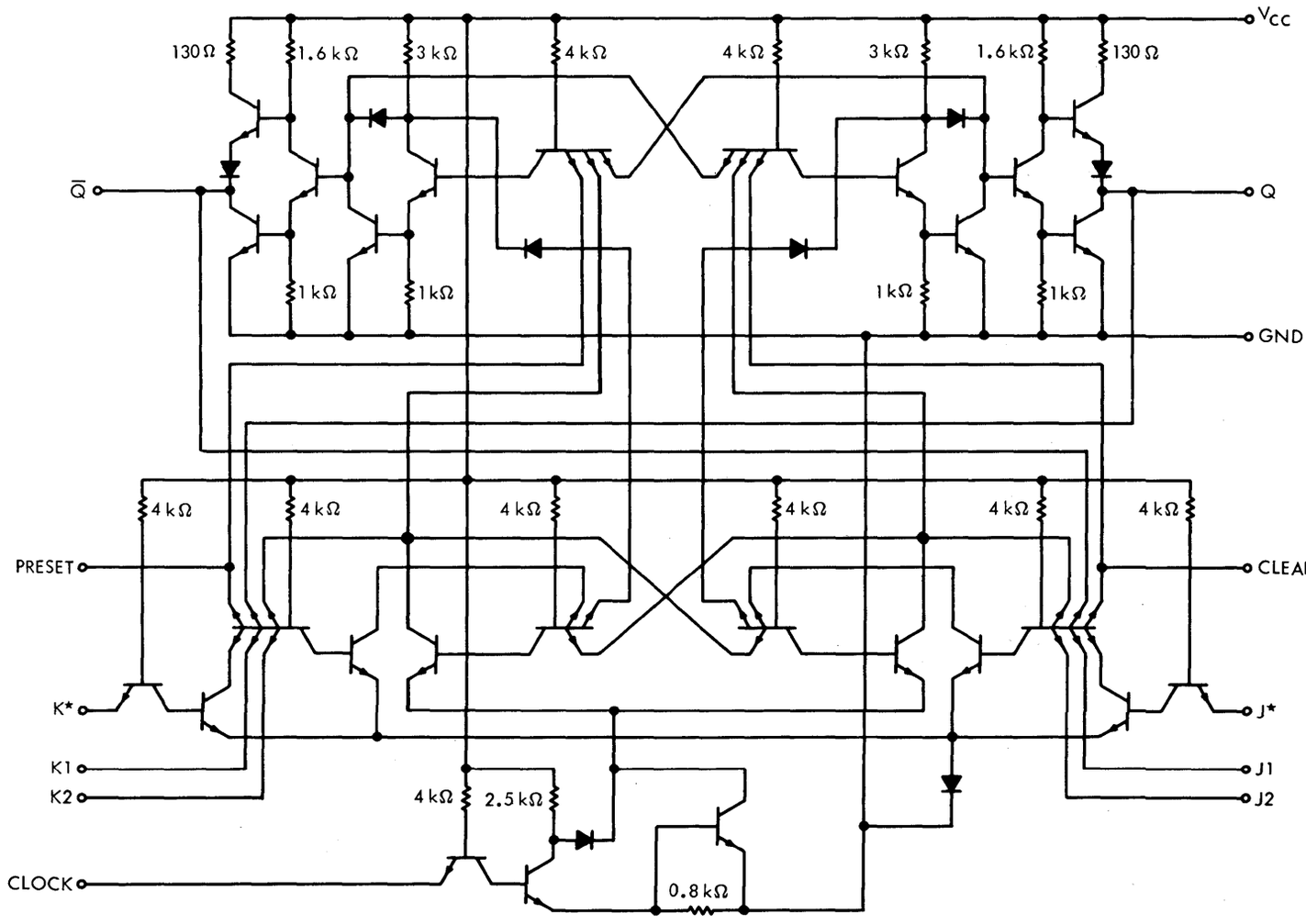
†Not more than one output should be shorted at a time.

‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	53	C_l = 15 pF	20	35		MHz
t_{setup}	Minimum input setup time	53	C_l = 15 pF		10	20	ns
t_{hold}	Minimum input hold time	53	C_l = 15 pF		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	C_l = 15 pF			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	52	C_l = 15 pF			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	53	C_l = 15 pF	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	53	C_l = 15 pF	10	18	50	ns

schematic



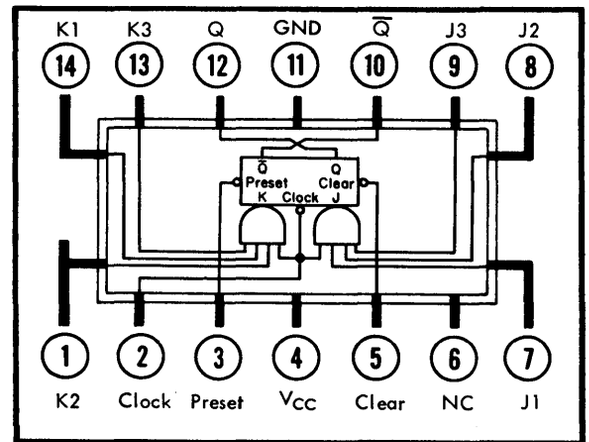
Component values shown are nominal.

TYPE SN7472
J-K MASTER-SLAVE FLIP-FLOP

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. J = J1 • J2 • J3
2. K = K1 • K2 • K3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

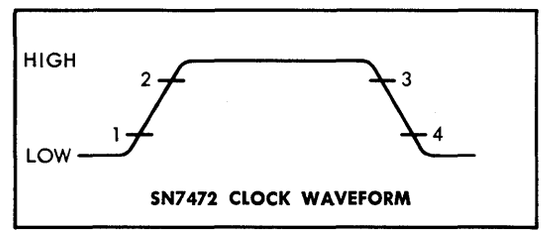


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

The SN7472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



SN7472 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54)	$\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 55)	$\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55)	$\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54)	$\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold}	$\geq$ 0

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	27	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	27	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	27	V_{CC} = 4.75 V, I_{load} = −400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	28	V_{CC} = 4.75 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	29	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	29	V_{CC} = 5.25 V, V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	30	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	30	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	31	V_{CC} = 5.25 V, V_{in} = 0	−18		−57	mA
I_{CC}	Supply current	30	V_{CC} = 5 V, V_{in} = 5 V		8‡		mA

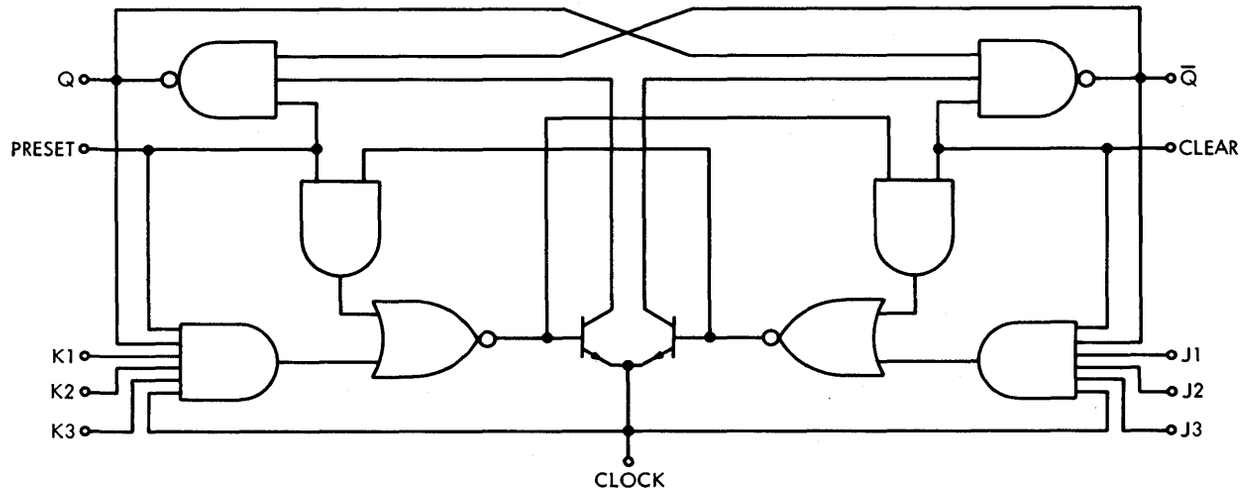
†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

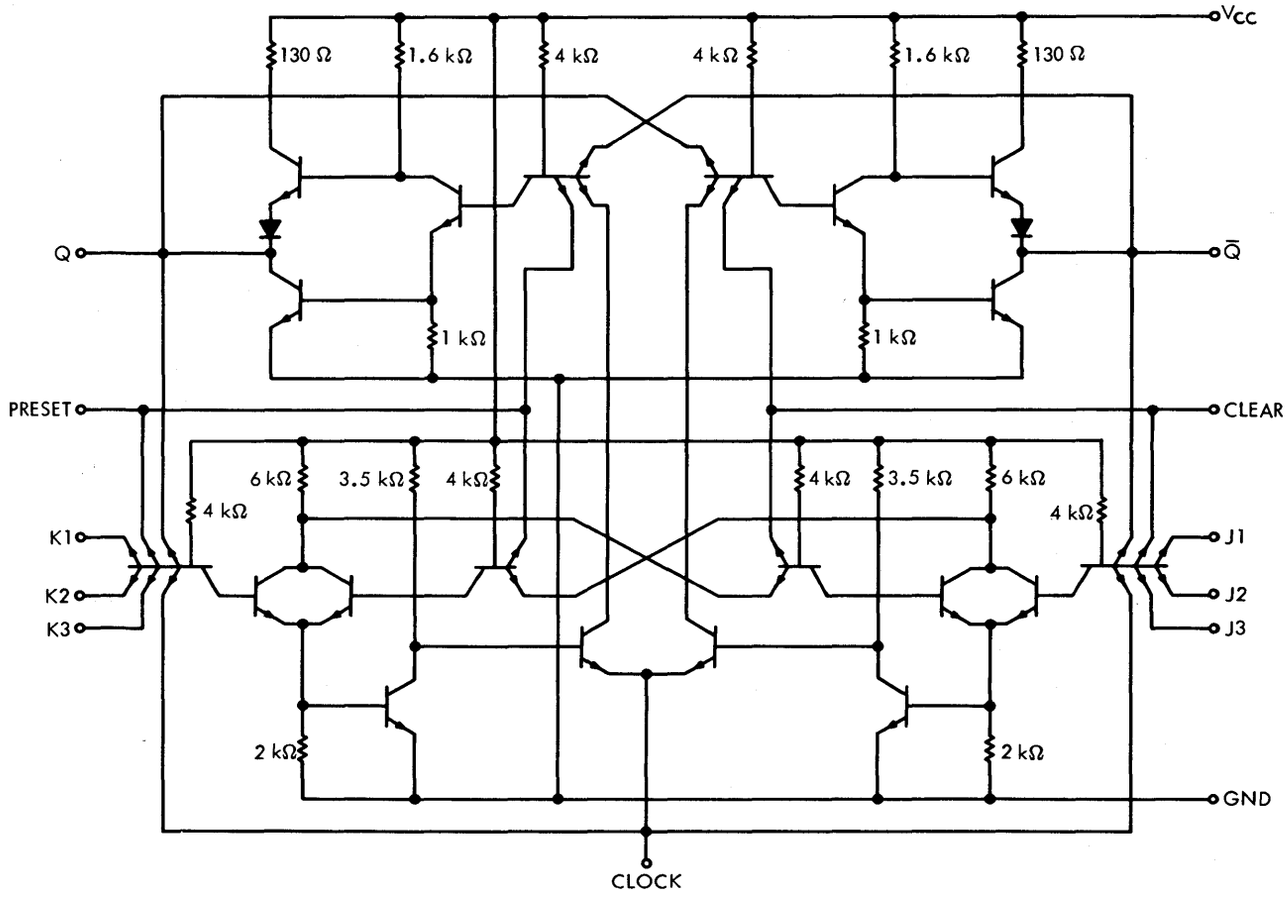
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	C_l = 15 pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	55	C_l = 15 pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	55	C_l = 15 pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	C_l = 15 pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	C_l = 15 pF	10	34	50	ns

TYPE SN7472
J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



schematic

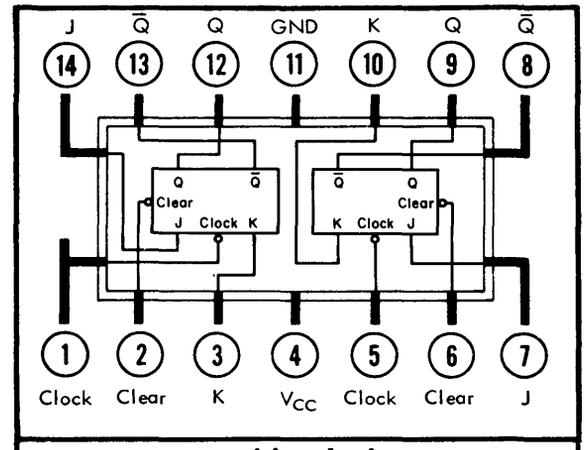


Component values shown are nominal.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



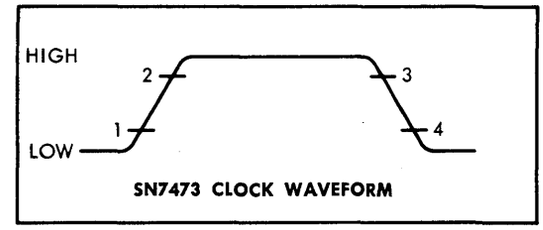
positive logic

Low input to clear sets Q to logical 0
Clear is independent of clock

description

The SN7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



SN7473 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54) . . . . . $\geq$ 20 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55) . . . . . $\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54) . . . . . $\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . $\geq$ 0

electrical characteristics, $T_A = 0°C$ to $70°C$

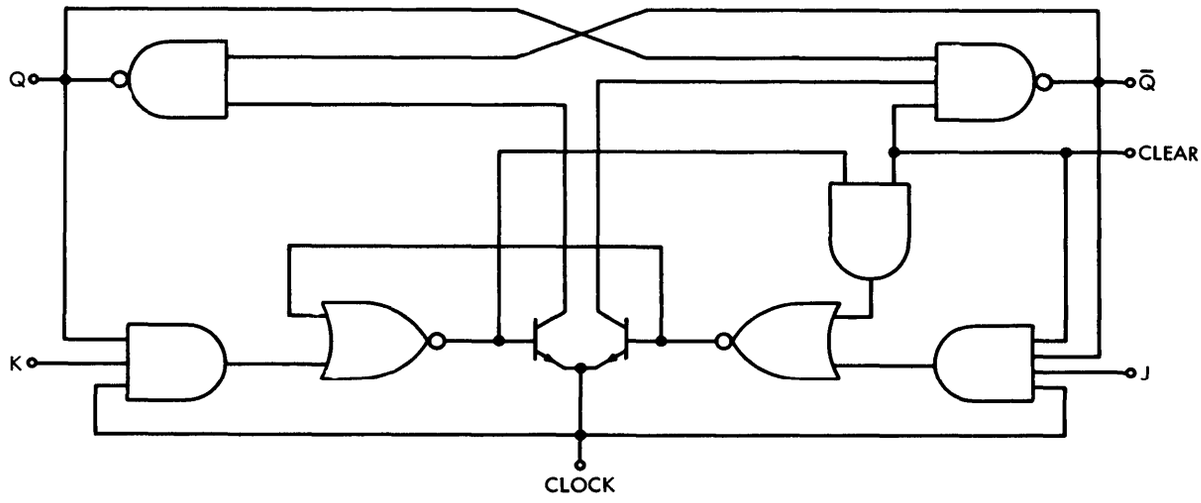
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	32	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	32	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	32	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	33	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	34	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	34	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	35	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	35	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	36	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	35	$V_{CC} = 5$ V, $V_{in} = 5$ V		8‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

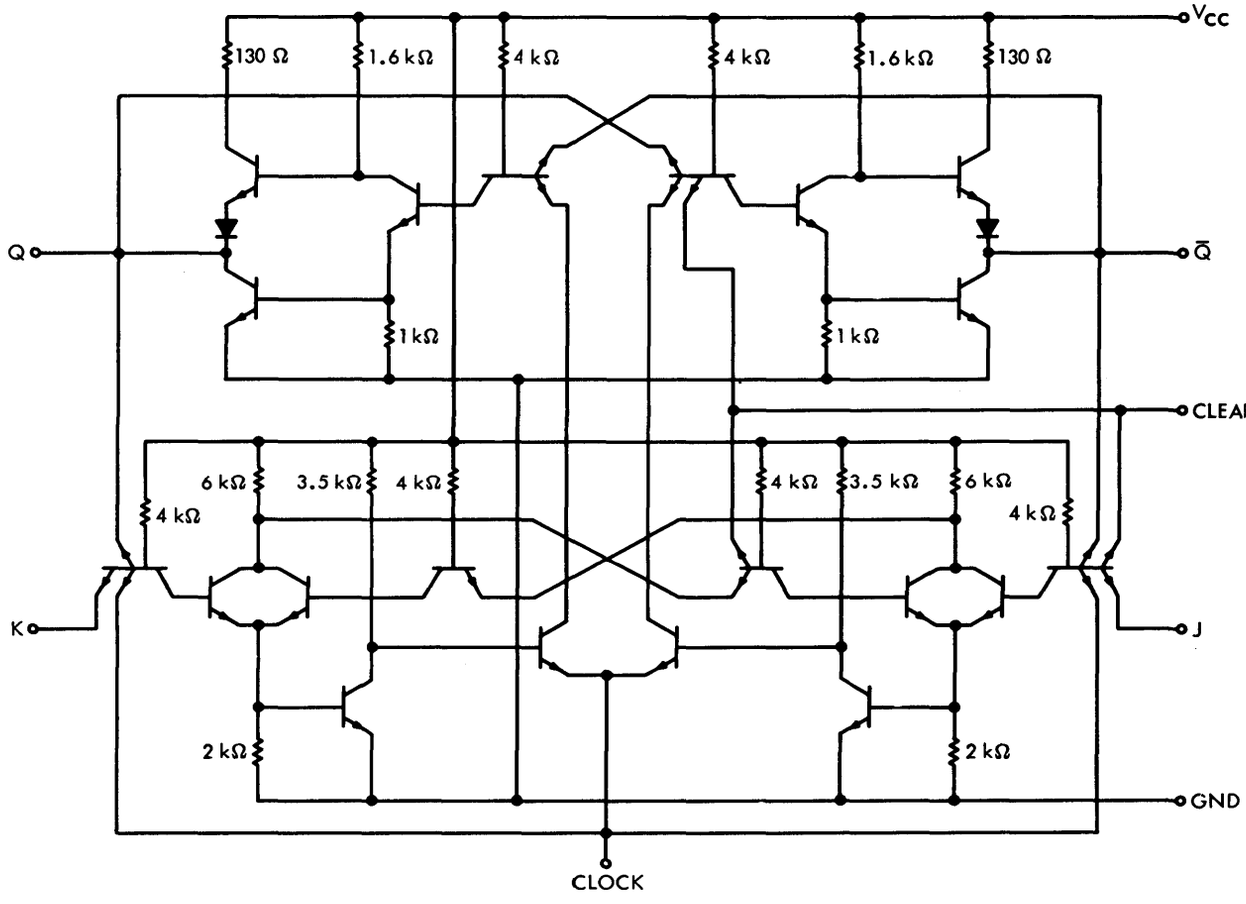
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	$C_l = 15$ pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	55	$C_l = 15$ pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	55	$C_l = 15$ pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	$C_l = 15$ pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	$C_l = 15$ pF	10	34	50	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

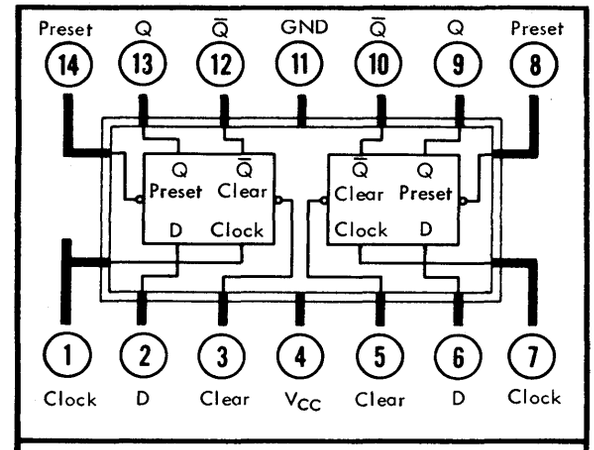
TYPE SN7474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

logic

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.



positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

The SN7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN7474 dual flip-flop has the same clocking characteristics as the SN7470 gated (edge-triggered) flip-flop and both are ideally suited for medium- and high-speed applications. The SN7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 56) . . . . . $\geq$ 30 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 53) . . . . . $\geq$ 30 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 53) . . . . . $\geq$ 30 ns

electrical characteristics, $T_A = 0°C$ to $70°C$

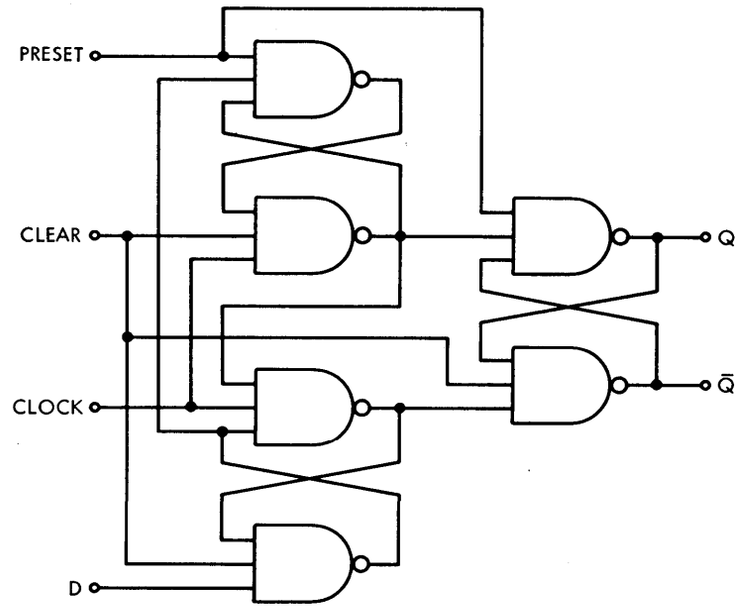
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	37	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	37	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	38	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	40	$V_{CC} = 5.25$ V, $V_{in} = 4.5$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			120	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	41	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	40	$V_{CC} = 5$ V, $V_{in} = 5$ V		8.5‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

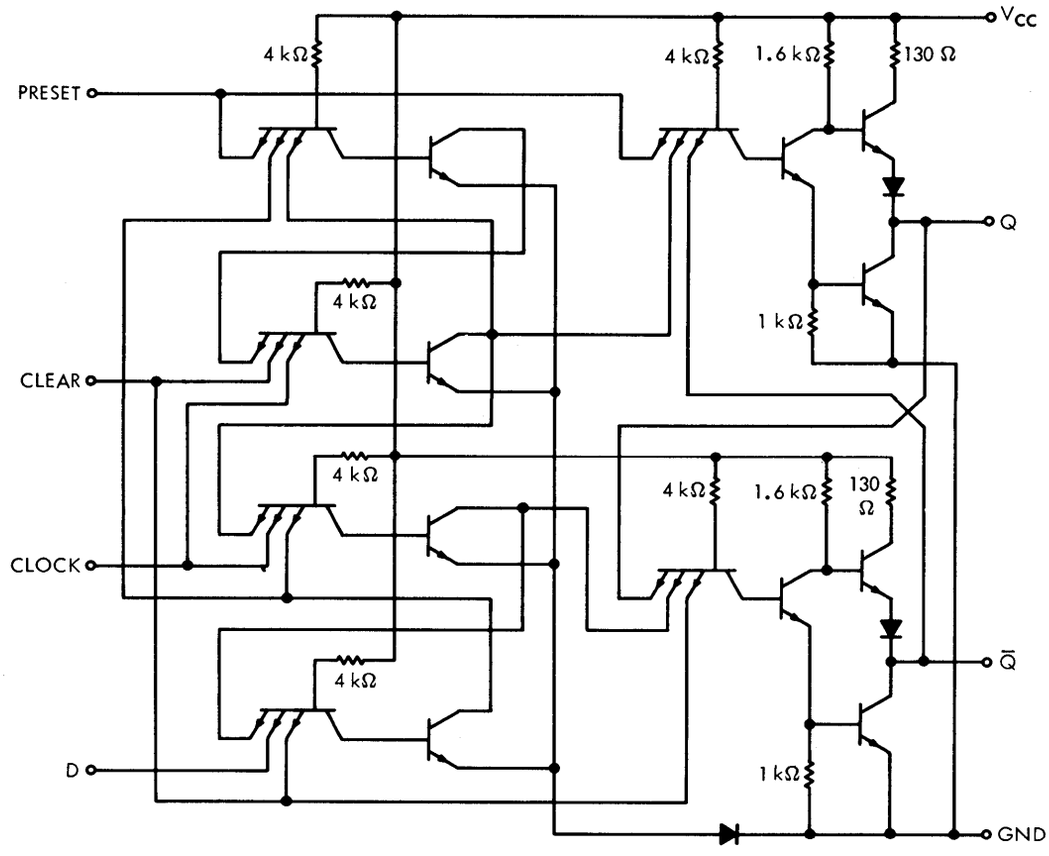
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	56	$C_1 = 15$ pF	15	25		MHz
t_{setup}	Minimum input setup time	56	$C_1 = 15$ pF		15	20	ns
t_{hold}	Minimum input hold time	56	$C_1 = 15$ pF		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	53	$C_1 = 15$ pF			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	53	$C_1 = 15$ pF			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	56	$C_1 = 15$ pF	10	28	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	56	$C_1 = 15$ pF	10	20	50	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



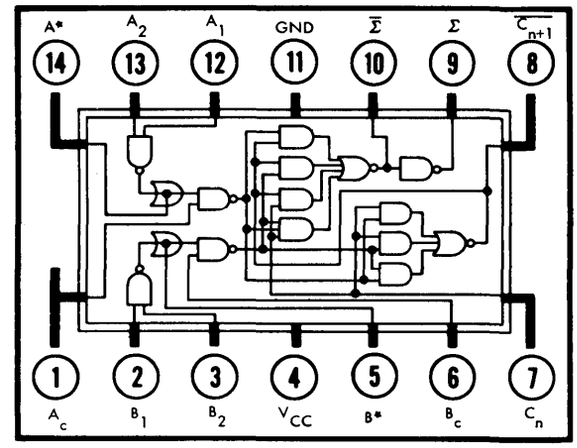
Component values shown are nominal.

logic

TRUTH TABLE (See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES: 1. $A = \overline{A\bigstar \cdot A_c}$, $B = \overline{B\bigstar \cdot B_c}$
where $A\bigstar = \overline{A_1 \cdot A_2}$, $B\bigstar = \overline{B_1 \cdot B_2}$
2. When $A\bigstar$ or $B\bigstar$ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, $A\bigstar$ or $B\bigstar$ respectively must be open or used to perform Dot-OR logic.



description

The SN7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Maximum Allowable Fan-Out From Outputs:

$\overline{C_{n+1}}$, N . . . . . 1 to 5

Σ or $\overline{\Sigma}$, N . . . . . 1 to 10

$A\bigstar$ or $B\bigstar$, N . . . . . 1 to 3

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	42 and 43	$V_{CC} = 4.75$ V, $V_{in(0)} = 0.8$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage	42 and 43	$V_{CC} = 4.75$ V, $V_{in(1)} = 2$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	43	$V_{CC} = 4.75$ V	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	42	$V_{CC} = 4.75$ V		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	44	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A★ or B★	45	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	45	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	46	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			15	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	47	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			200	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$†	48	$V_{CC} = 5.25$ V	−18		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$†	48	$V_{CC} = 5.25$ V	−18		−70	mA
I_{CC}	Supply current	49	$V_{CC} = 5$ V		21‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	N = 5		13	17	ns
t_{pd0}			2	N = 5		3	7	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	N = 5		18	25	ns
t_{pd0}			4	N = 5		38	55	ns
t_{pd1}	A_C	Σ	5	N = 10		52	70	ns
t_{pd0}			6	N = 10		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	N = 10		38	55	ns
t_{pd0}			8	N = 10		56	75	ns
t_{pd1}	A_1	A★	9	$C_L = 15$ pF		48	65	ns
t_{pd0}			10	$C_L = 15$ pF		17	25	ns
t_{pd1}	B_1	B★	11	$C_L = 15$ pF		48	65	ns
t_{pd0}			12	$C_L = 15$ pF		17	25	ns

¶t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

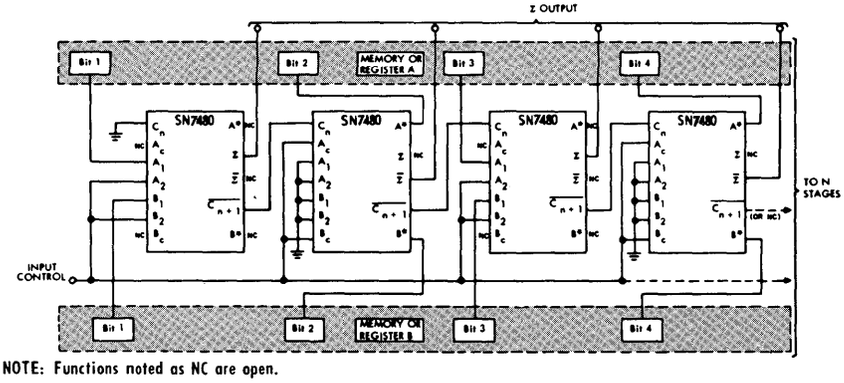
n-bit binary adder or subtractor (see figures F and G)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (figure F). The inverted carry output is a *true* carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

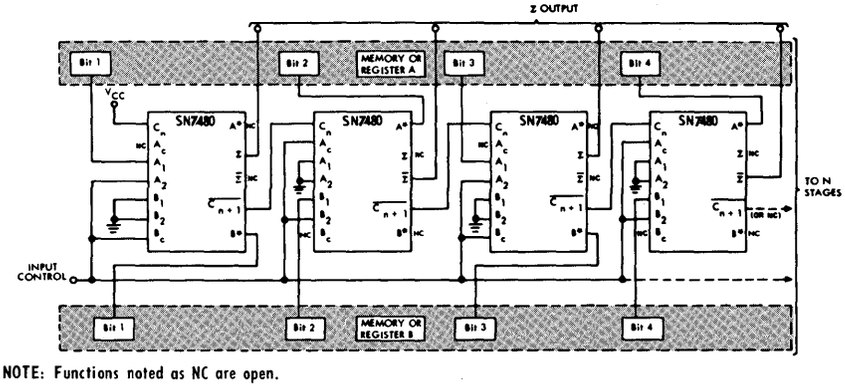
When performing subtraction (figure G) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to A_2 and B_2 of odd-numbered bits and to A_c and B_c of even-numbered bits. For the subtractor (figure G), input control is applied to A_2 and B_c of the odd-numbered bits and to A_c and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE F — N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE G — N-BIT BINARY SUBTRACTOR

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure H)

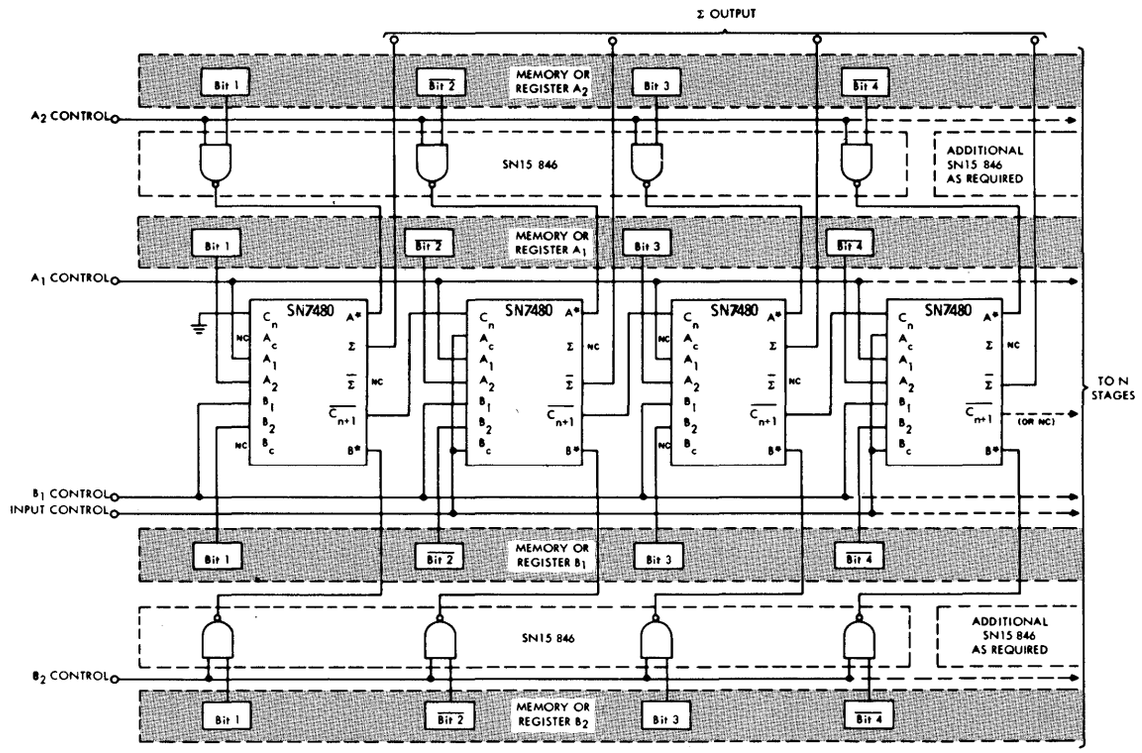
This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1 and externally by a type SN15 846 DTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fan-out rules should be observed.) In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines *and* the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15 846) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

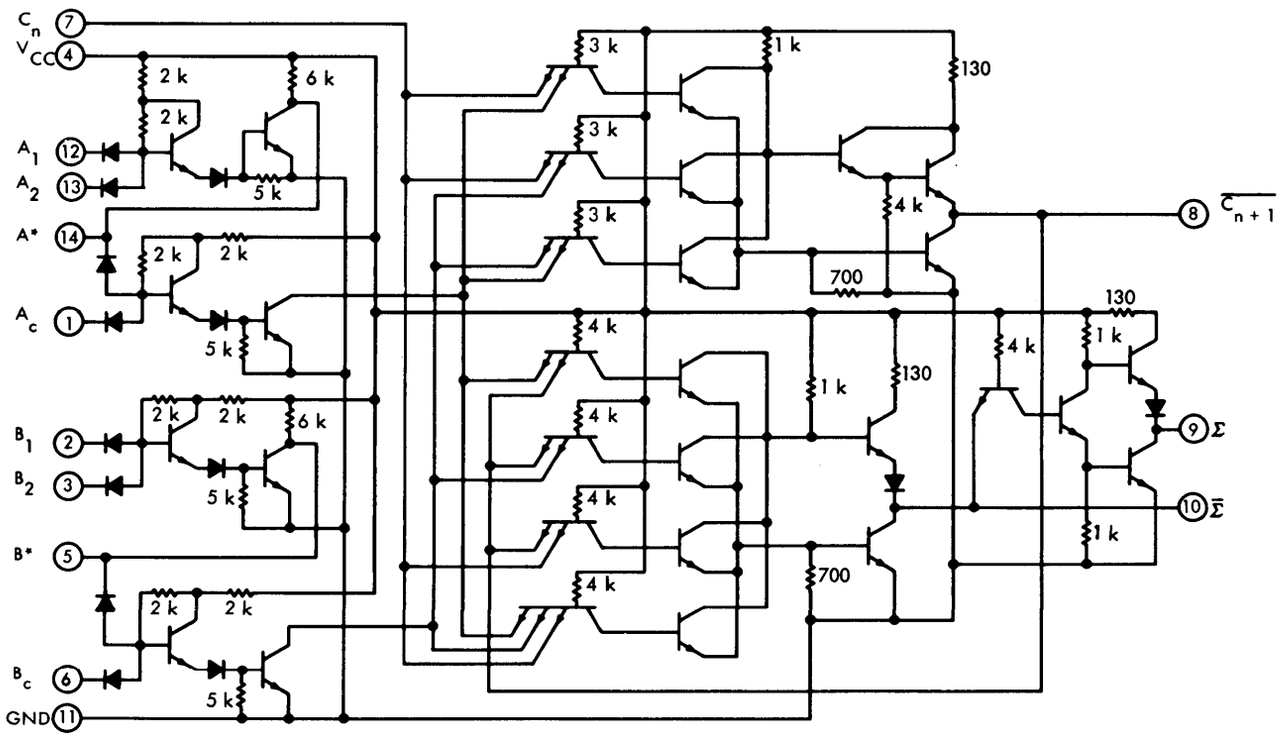
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



NOTE: Functions noted as NC are open.

FIGURE H. N-BIT BINARY ADDER WITH REGISTER SELECTION

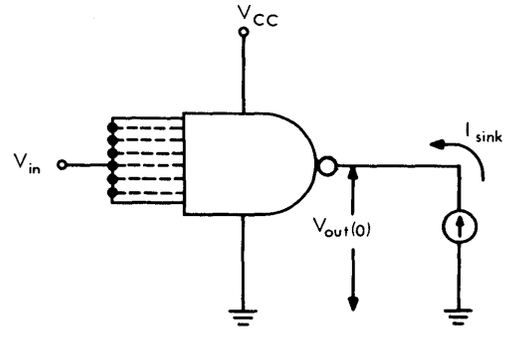
schematic diagram



Component values shown are nominal.
Resistor values are in ohms.

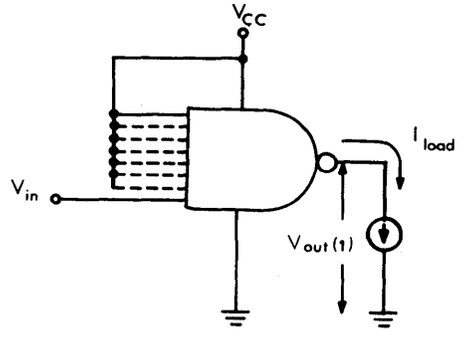
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



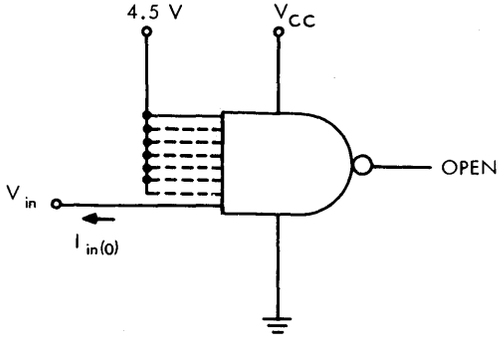
1. All inputs tested simultaneously.

FIGURE 1



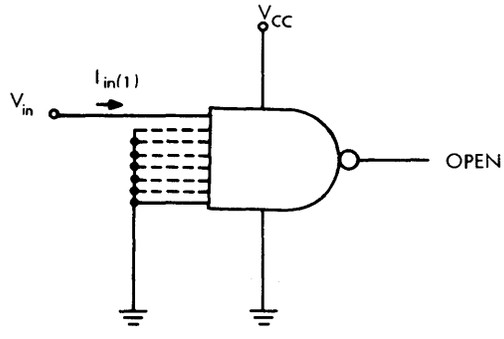
1. Each input tested separately.

FIGURE 2



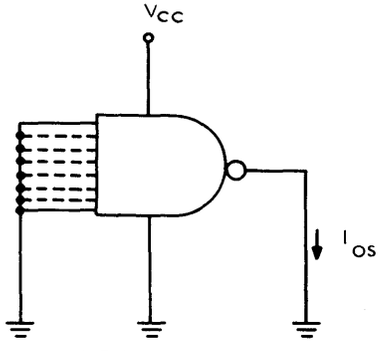
1. Each input tested separately.

FIGURE 3



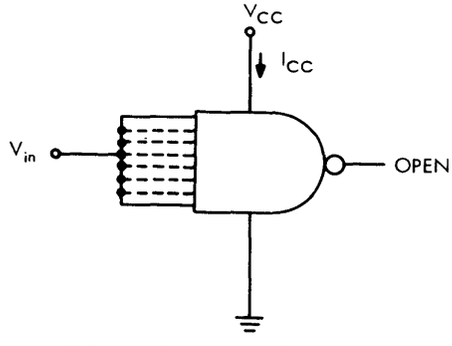
1. Each input tested separately.

FIGURE 4



1. Each gate tested separately.

FIGURE 5



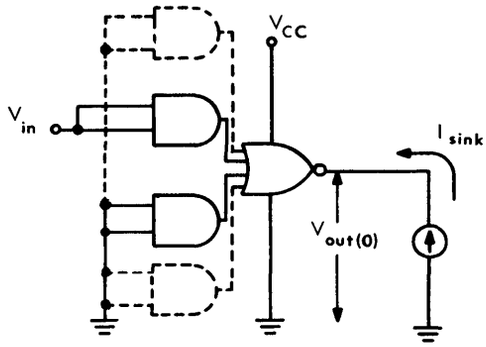
1. Test logical 0 and logical 1 conditions.

FIGURE 6

§Arrows indicate actual direction of current flow.

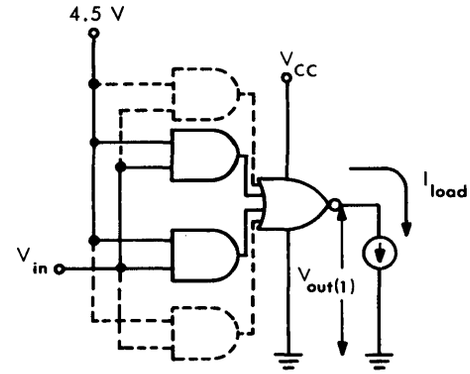
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



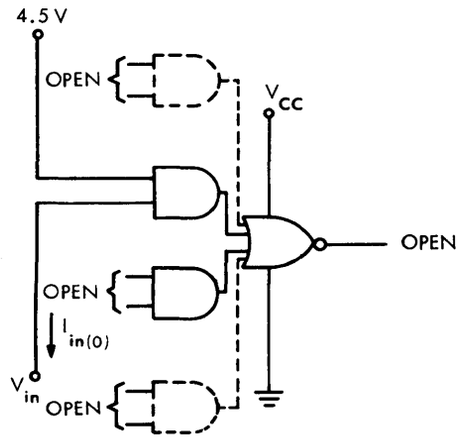
1. Each AND section tested separately.

FIGURE 7



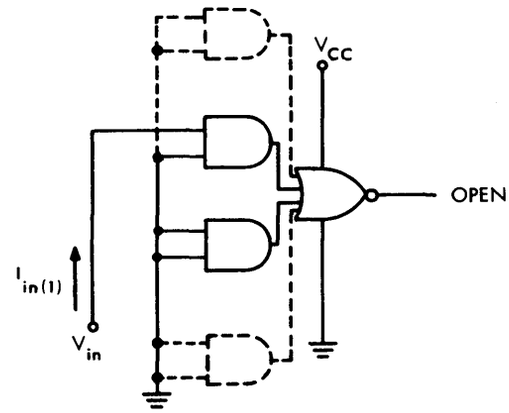
1. Each pair of inputs tested separately.

FIGURE 8



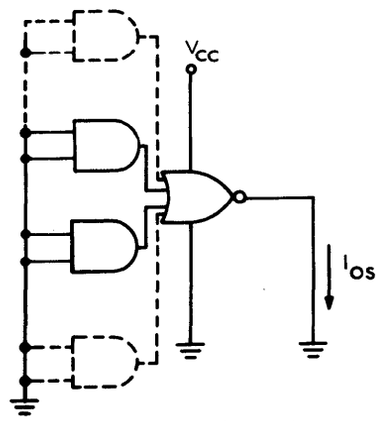
1. Each input tested separately.

FIGURE 9



1. Each input tested separately.

FIGURE 10



1. Each gate tested separately.

FIGURE 11

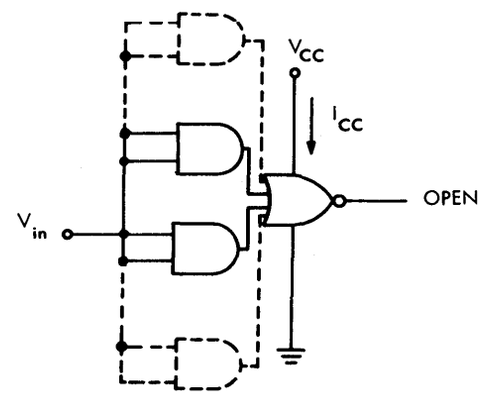


FIGURE 12

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

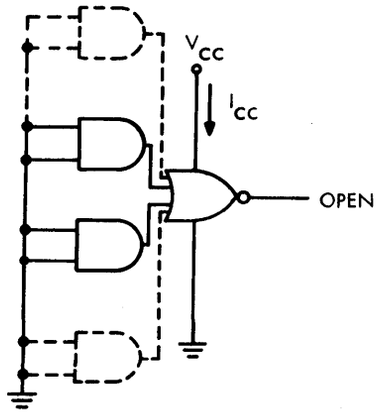


FIGURE 13

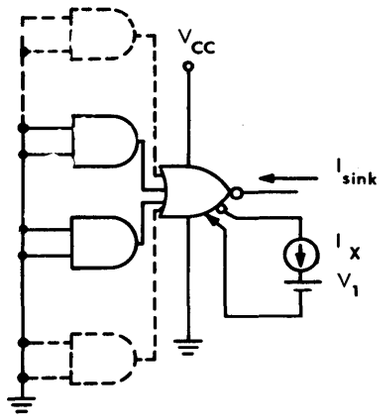


FIGURE 14

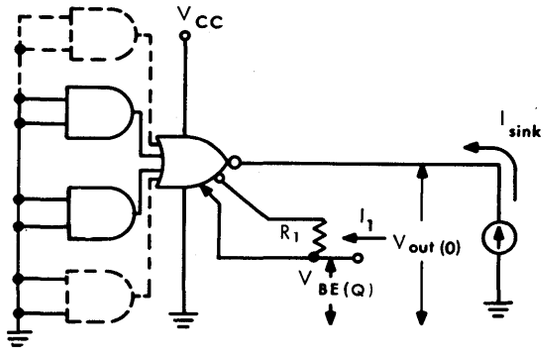


FIGURE 15

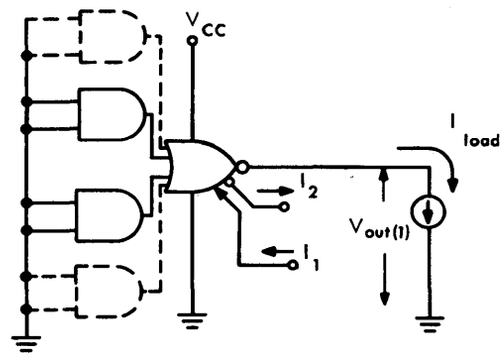
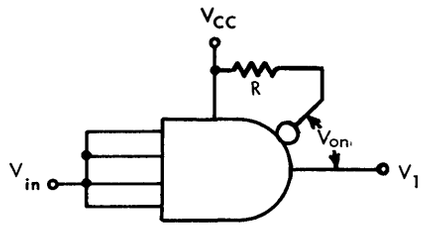
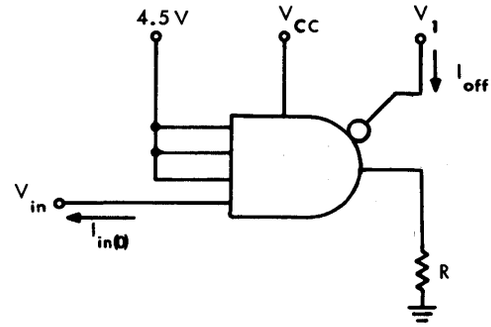


FIGURE 16



1. All inputs tested simultaneously.

FIGURE 17



1. Each input tested separately.

FIGURE 18

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

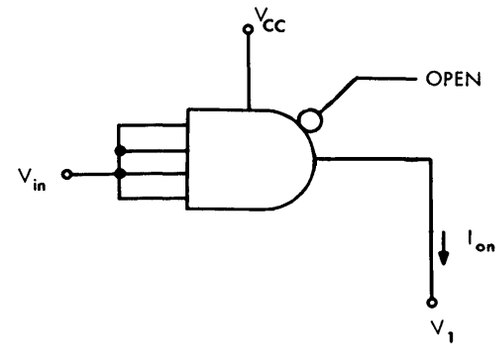
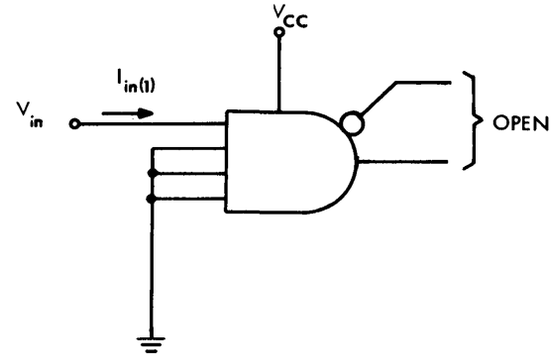
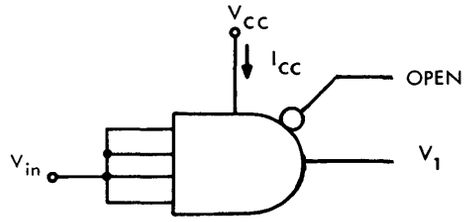


FIGURE 19



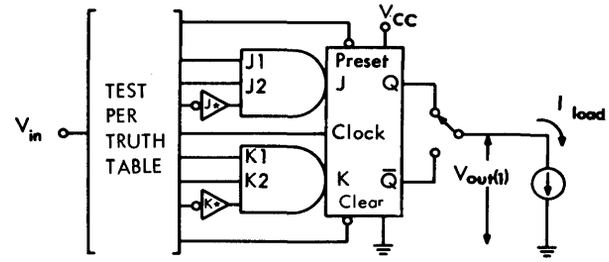
1. Each input tested separately.

FIGURE 20



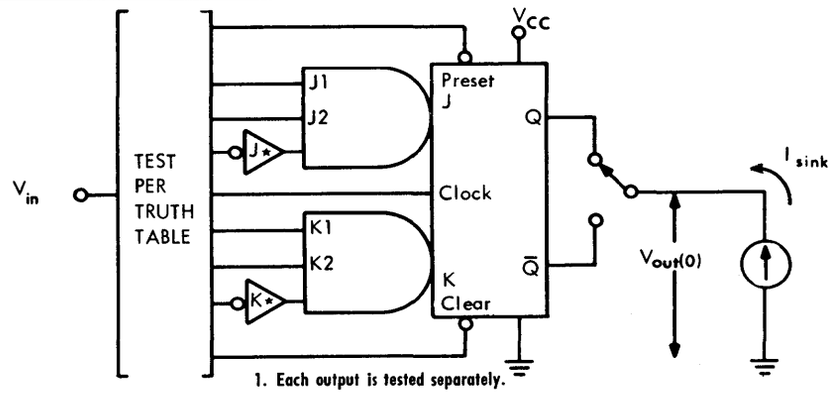
1. Test "on" and "off" conditions.

FIGURE 21



1. Each output is tested separately.
2. Preset and clear are tested with $V_{in(clock)} = 0$.

FIGURE 22



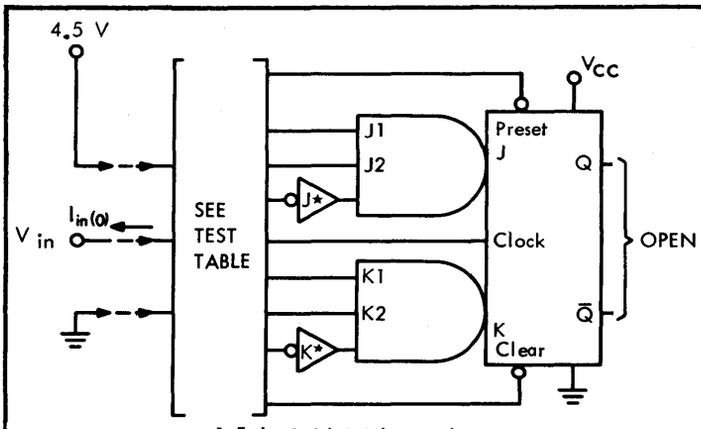
1. Each output is tested separately.

FIGURE 23

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

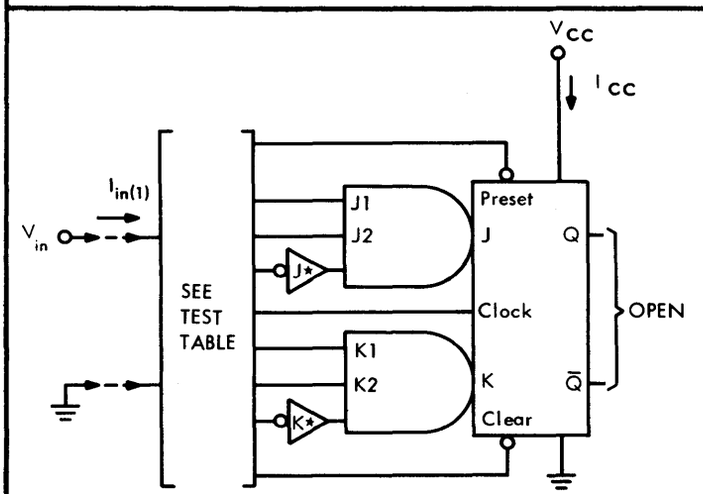
d-c test circuits§ (continued)



1. Each output is tested separately.

TEST TABLE			
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Ground	Apply Momentary GND, then 4.5 V
J2	J1	J★	Clear
J1	J2	J★	Clear
J★	None	None	None
K2	K1	K★	Preset
K1	K2	K★	Preset
K★	None	None	None
Clock	None	None	None
Preset	K1 and K2	K★	None
Clear	J1 and J2	J★	None

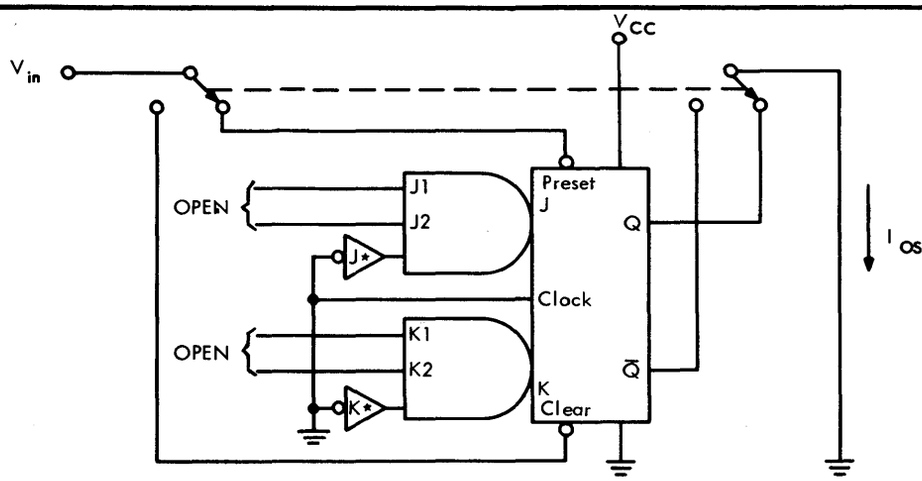
FIGURE 24



TEST TABLE (See Note 2)		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply 4.5 V
J2	J1 and Clear	J★
J1	J2 and Clear	J★
J★	None	None
K2	K1 and Preset	K★
K1	K2 and Preset	K★
K★	None	None
Clock	None	None
Preset	K1 and K2	K★
Clear	J1 and J2	J★

1. Each input is tested separately.
2. Test voltage and grounds are applied to inputs in accordance with test table, and $I_{in(1)}$ is measured for input being tested.

FIGURE 25



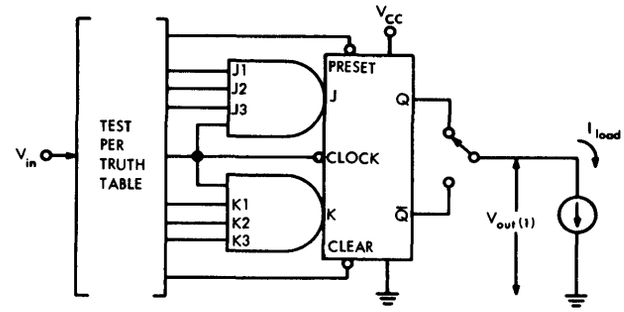
1. Each output is tested separately.

FIGURE 26

§ Arrows indicate actual direction of current flow.

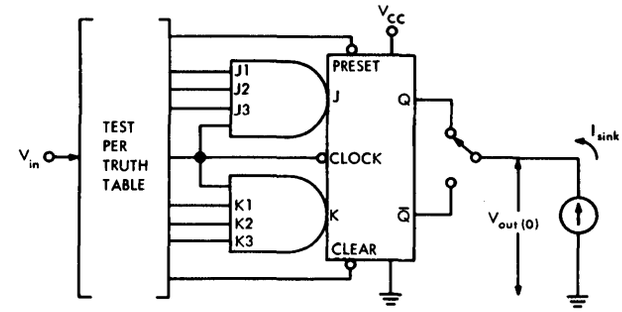
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



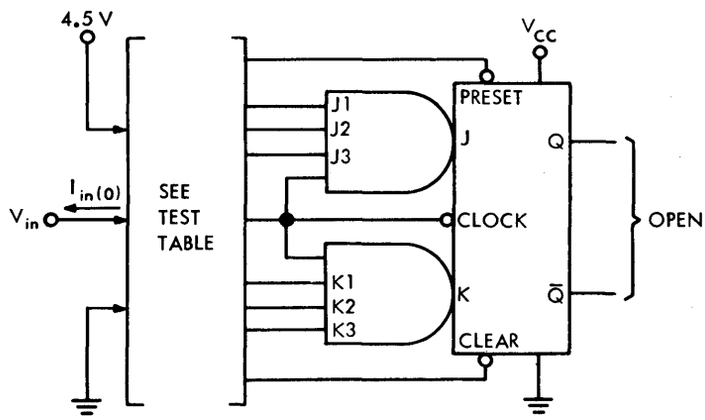
1. Each output is tested separately.

FIGURE 27



1. Each output is tested separately.

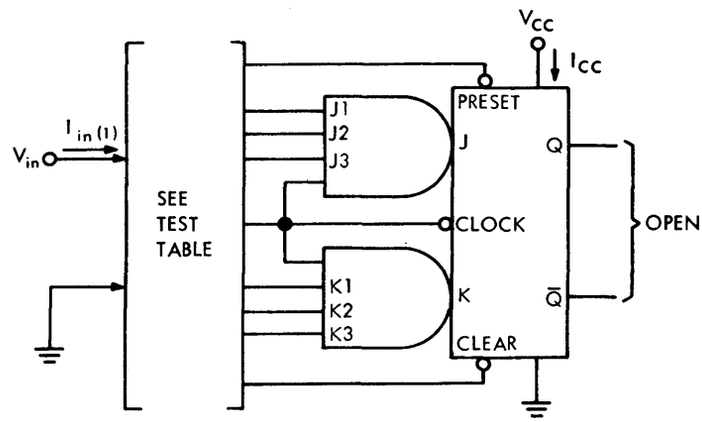
FIGURE 28



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

FIGURE 29



1. Each input is tested separately.

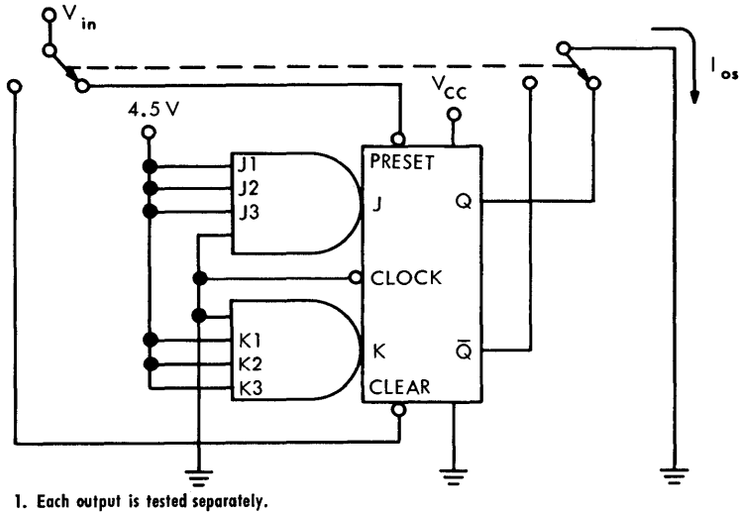
TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

FIGURE 30

§Arrows indicate actual direction of current flow.

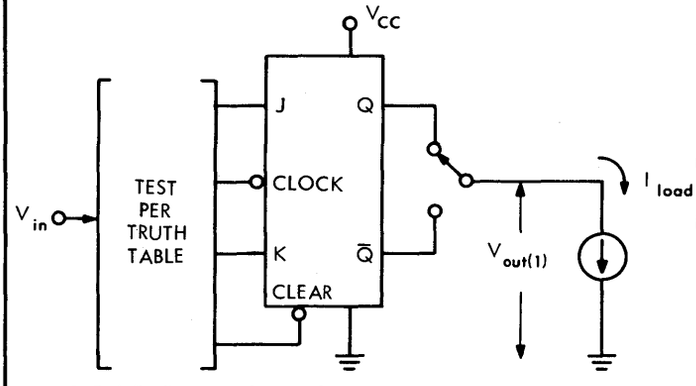
PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)



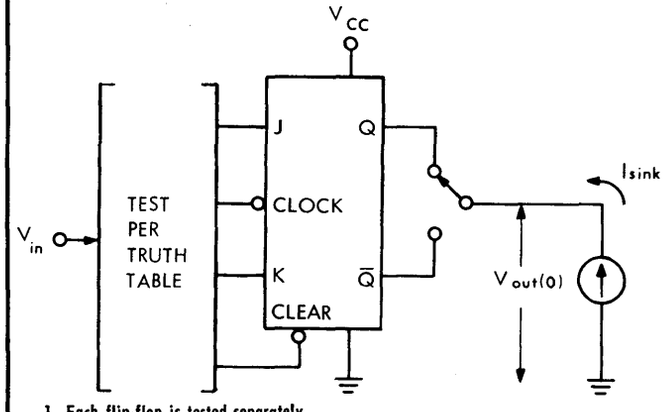
1. Each output is tested separately.

FIGURE 31



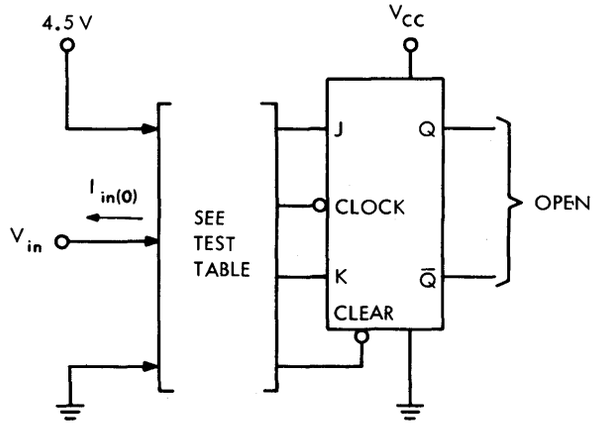
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 32



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 33



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

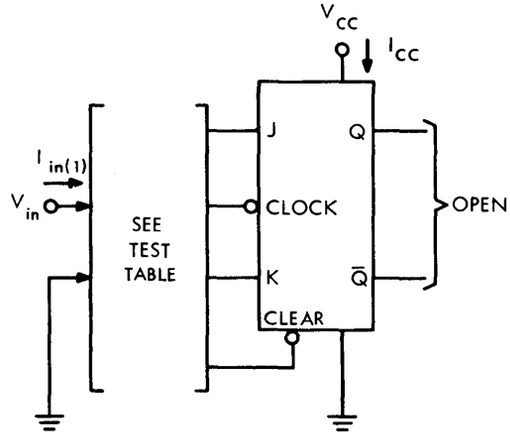
1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\bar{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.

FIGURE 34

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

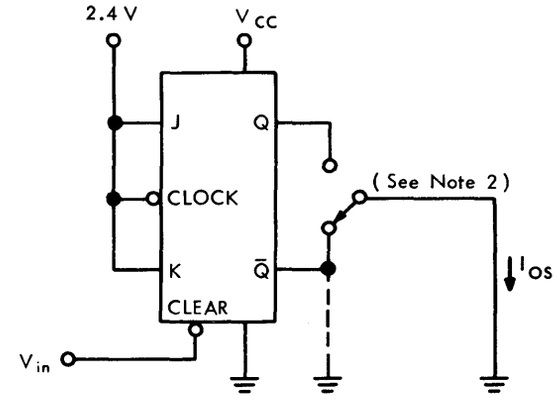
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
J	Clock and Clear	None
K	Clock	Clear

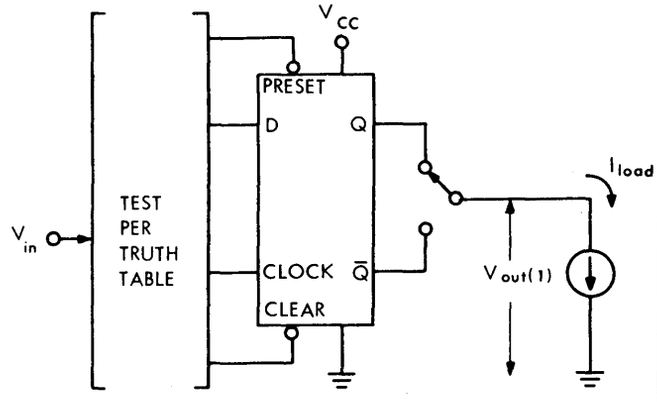
1. Each flip-flop is tested separately.

FIGURE 35



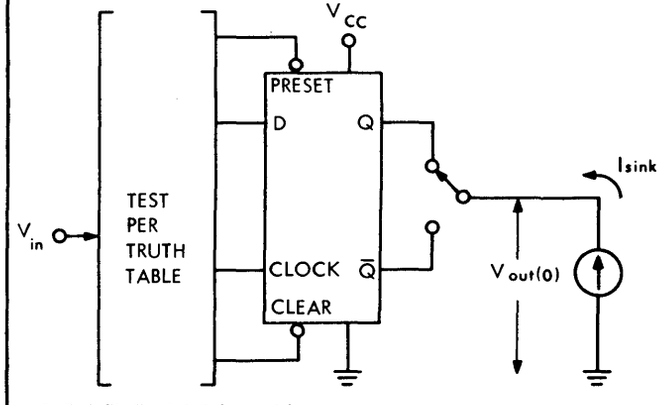
1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\bar{Q}$. When testing Q, open all inputs, ground $\bar{Q}$, and limit duration of test to 100 ms.

FIGURE 36



1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 37



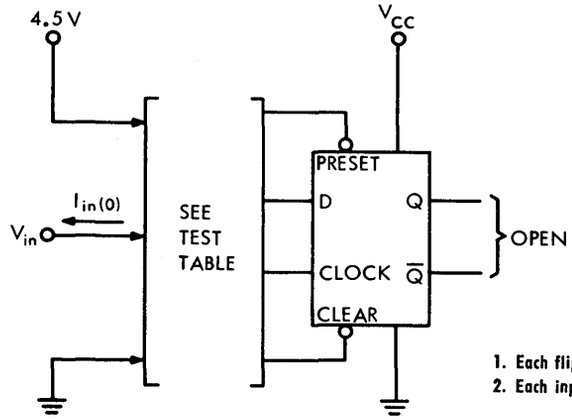
1. Each flip-flop is tested separately.
2. Each output is tested separately.

FIGURE 38

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

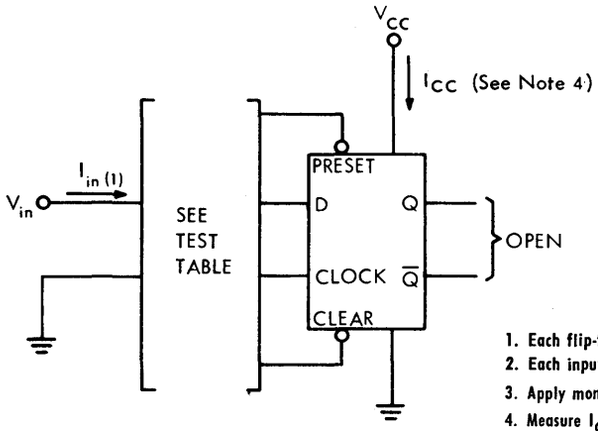
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	Apply GND
Clock	Clear and Preset	D
Preset	Clear and Clock	D
Clear	Clock and D	None
D	Clear and Clock	Preset

1. Each flip-flop is tested separately.
2. Each input is tested separately.

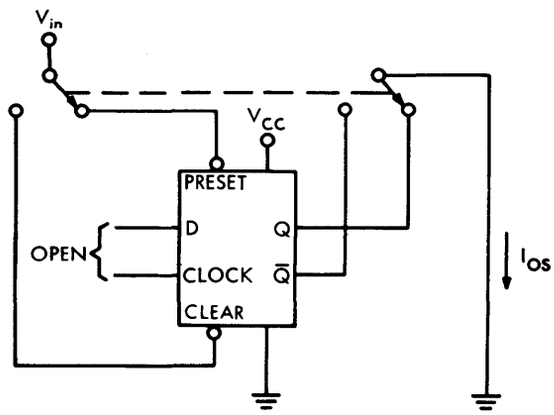
FIGURE 39



TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Apply 4.5 V	Apply GND
Clock	None	Clear
Preset	Clear and D	Clock (See Note 3)
Clear	None	D, Clock, and Q
D	Clock	Clear

1. Each flip-flop is tested separately.
2. Each input is tested separately.
3. Apply momentary GND to Clock, then 4.5 V.
4. Measure I_{CC} with D and clock input at GND.

FIGURE 40



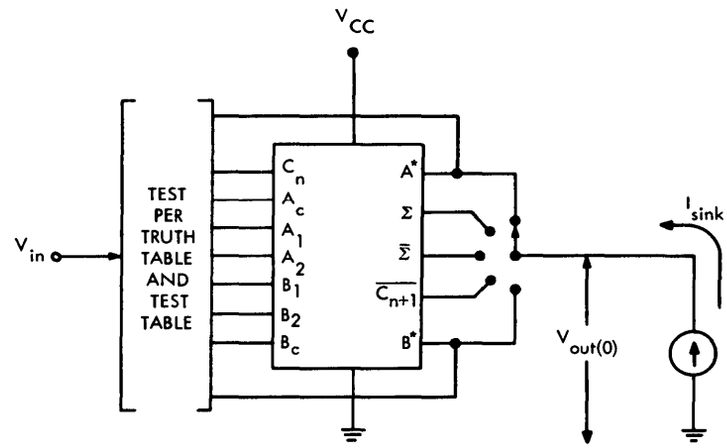
1. Each output is tested separately.

FIGURE 41

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)

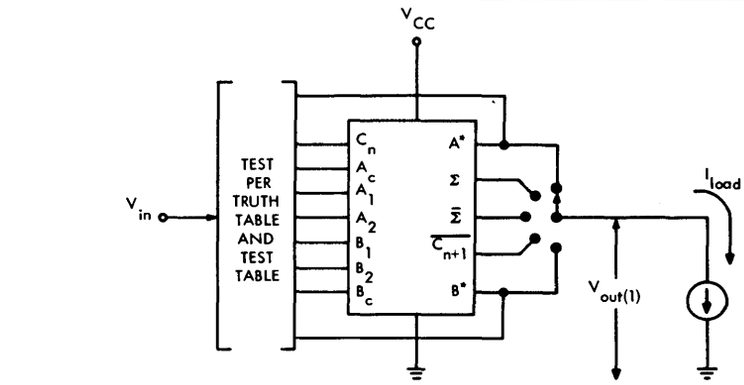


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 42



TEST TABLE

Output Under Test	I_{load} (Min)
Σ or $\overline{\Sigma}$	-400 μA
$\overline{C_{n+1}}$	-200 μA
A★ or B★	-120 μA

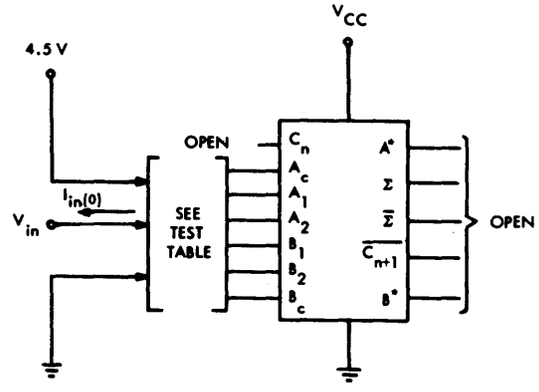
1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

FIGURE 43

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§(continued)

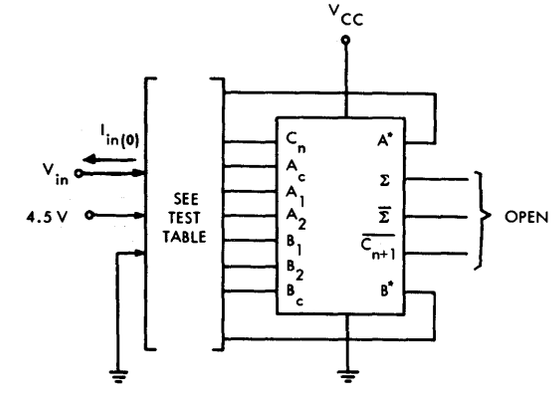


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 44



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_c	A_1 and A_2
B★	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

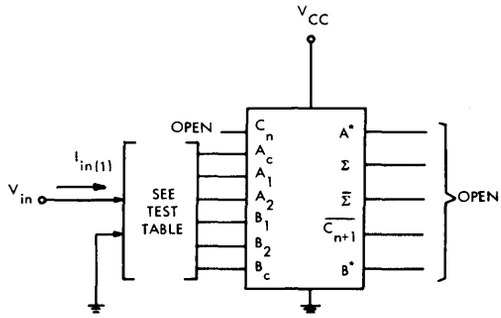
1. Each input is tested separately.

FIGURE 45

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§(continued)



TEST TABLE

Apply V_{in} (Test $I_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

1. Each input is tested separately.

FIGURE 46

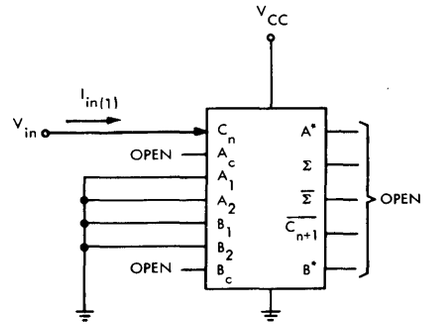
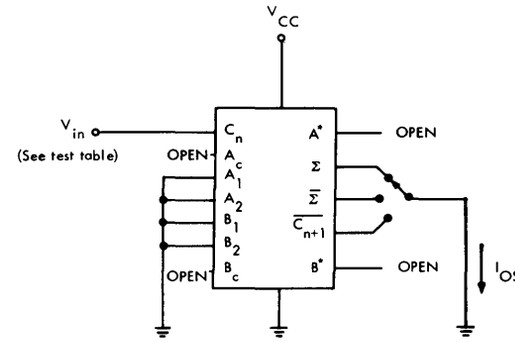


FIGURE 47



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C_n + 1}$	GND

FIGURE 48

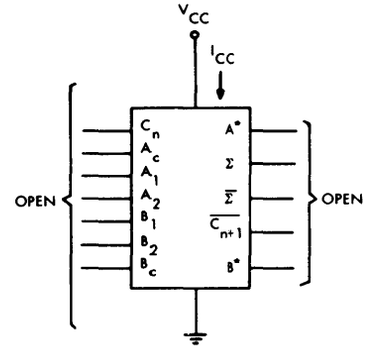
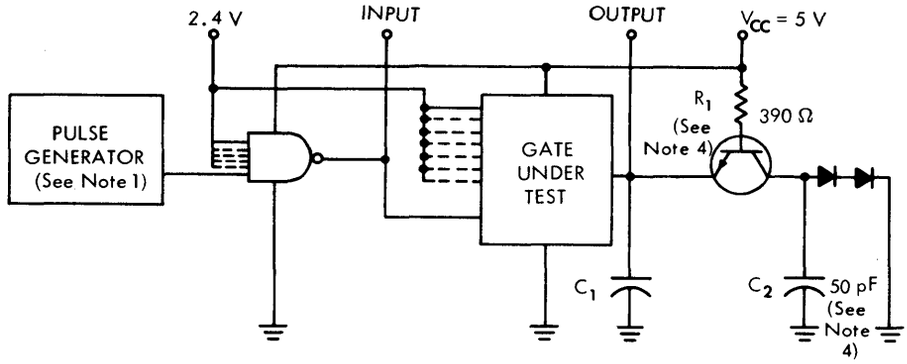


FIGURE 49

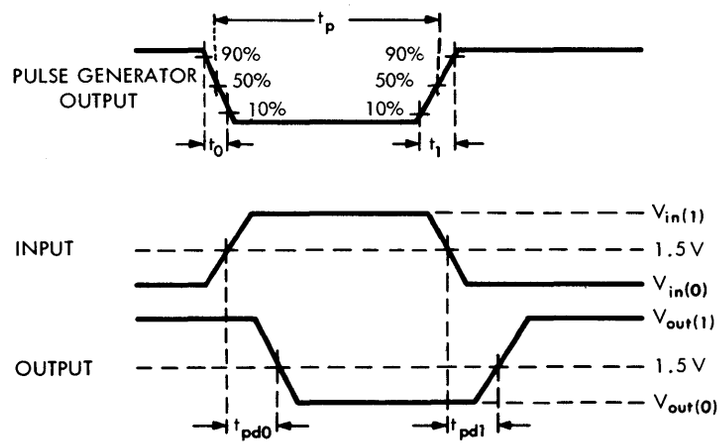
§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



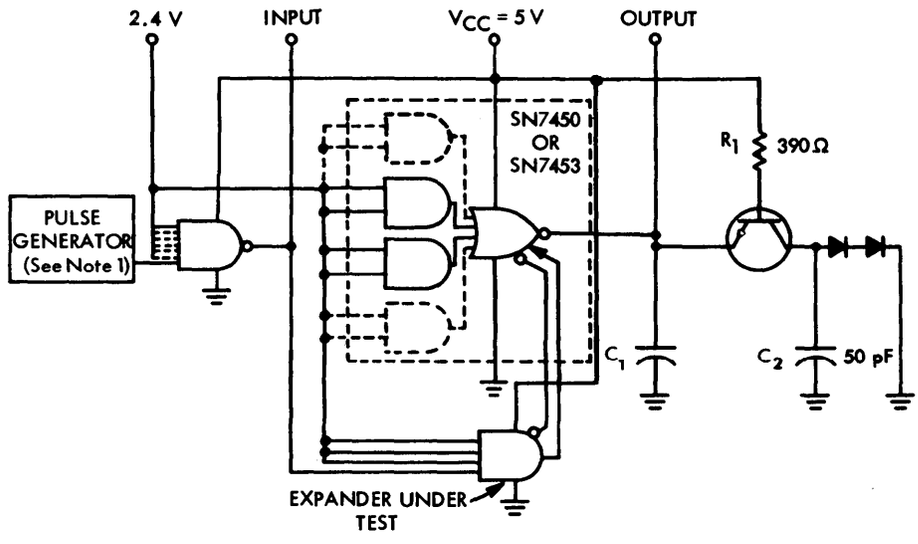
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_0 = t_1 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. Test SN7440 with $R_1 = 130\ \Omega$, $C_2 = 150$ pF.
5. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
6. C_1 includes probe and jig capacitance.

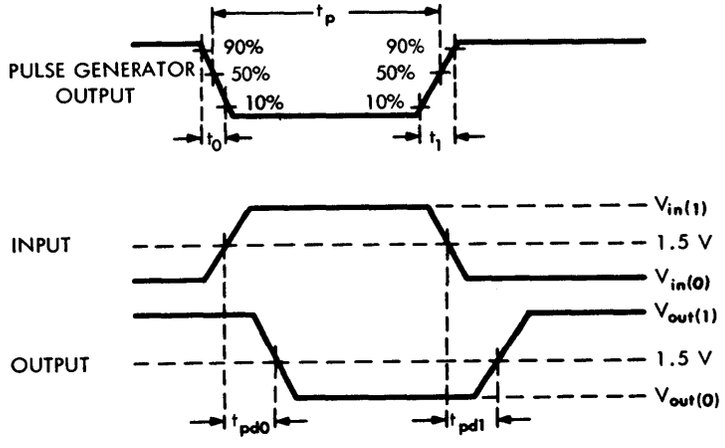
FIGURE 50 — GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



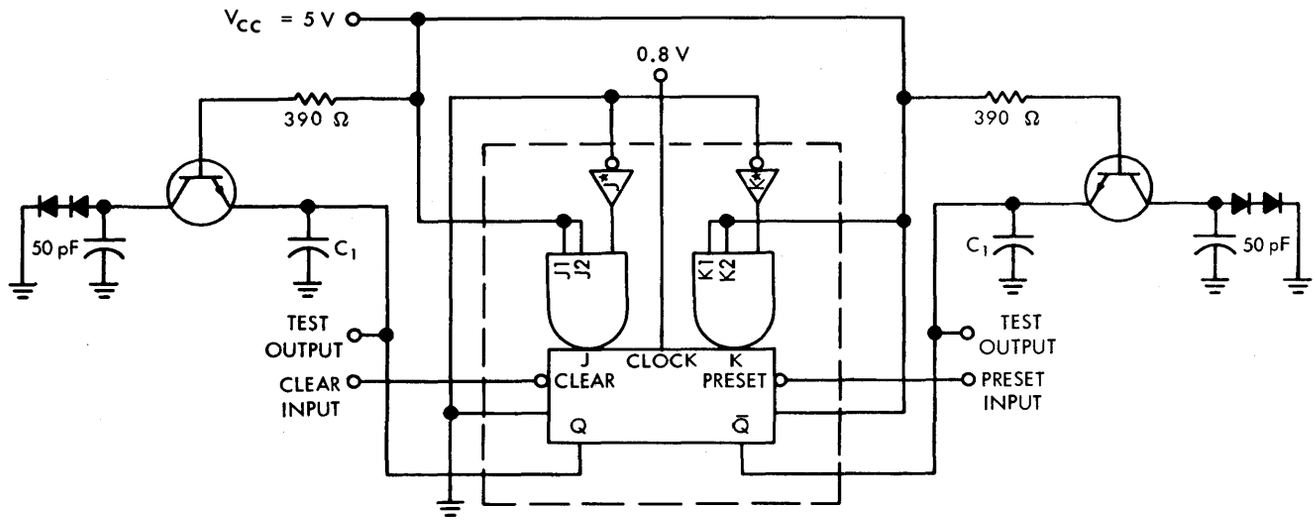
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_0 = t_1 \leq 15$ ns, $t_p = 0.5$ μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. $t_{pd} = \dfrac{t_{pd0} + t_{pd1}}{2}$
5. C_1 includes probe and jig capacitance.

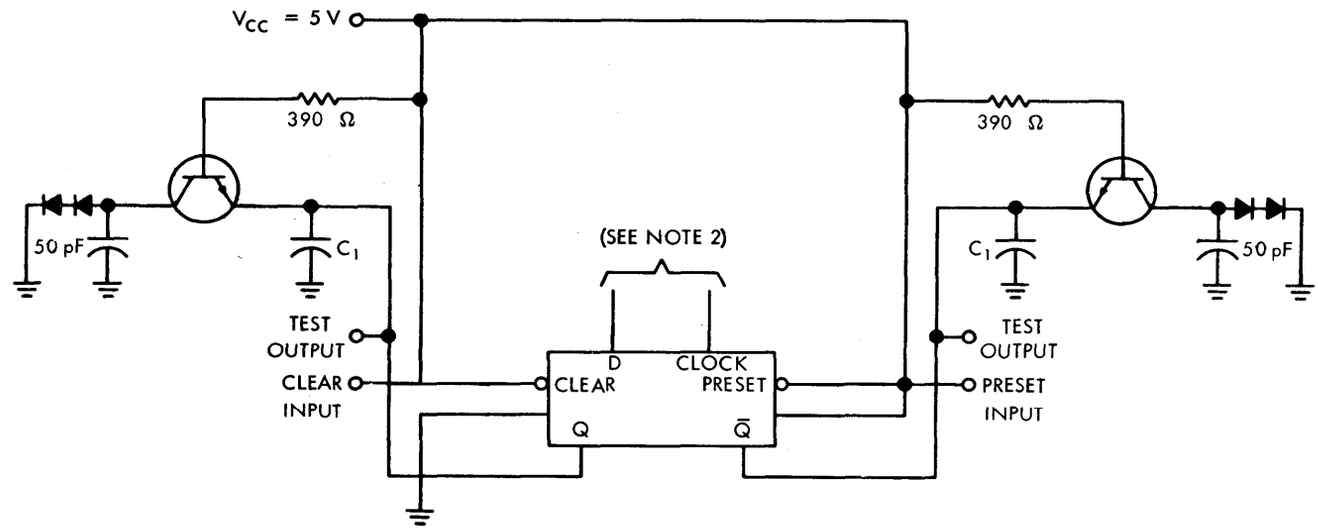
FIGURE 51 — EXPANDER PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT SN7470



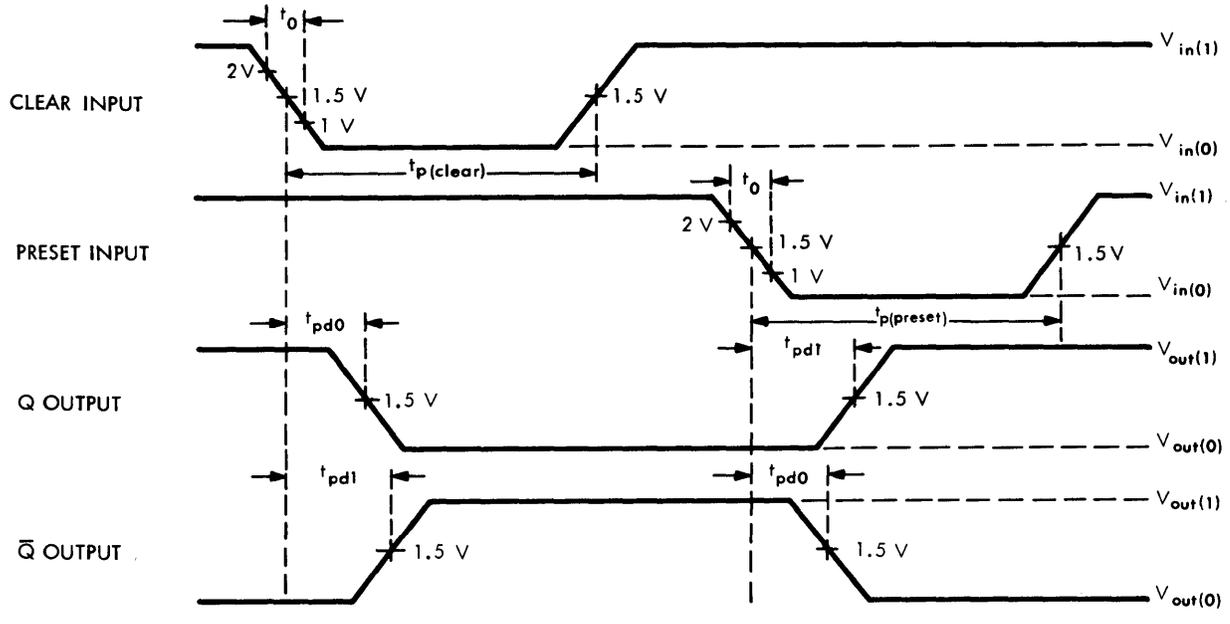
TEST CIRCUIT SN7474

NOTES: 1. Present or clear function of the SN7470 can occur only when clock input is low. Gated inputs are inhibited.
2. Clear and preset inputs of the SN7474 dominate regardless of the state of clock or D inputs.
3. All transistors are 2N2368.
4. All diodes are 1N916.
5. C_1 includes probe and jig capacitance.

FIGURE 52 — SN7470 AND SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



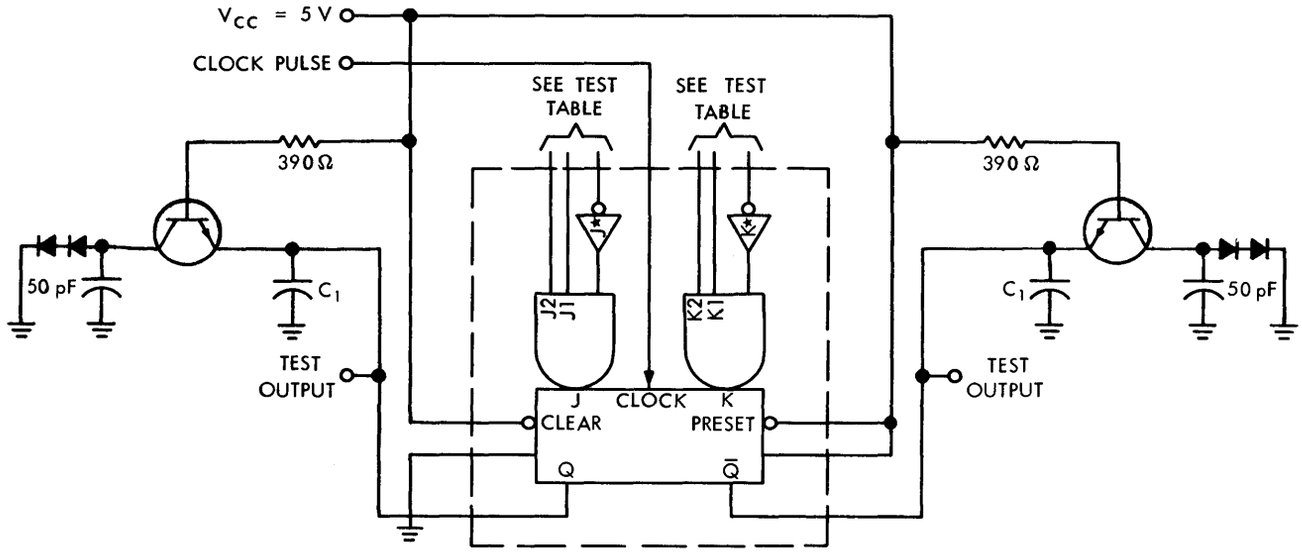
VOLTAGE WAVEFORMS

NOTE 6: Clear or preset input pulse characteristics: $V_{in(0)} = 0.4$ V, $V_{in(1)} = 2.4$ V, $t_0 = 3$ to 6 ns, $t_p = 25$ ns for the SN7470, and $t_p = 30$ ns for SN7474.

FIGURE 52— SN7470 AND SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)

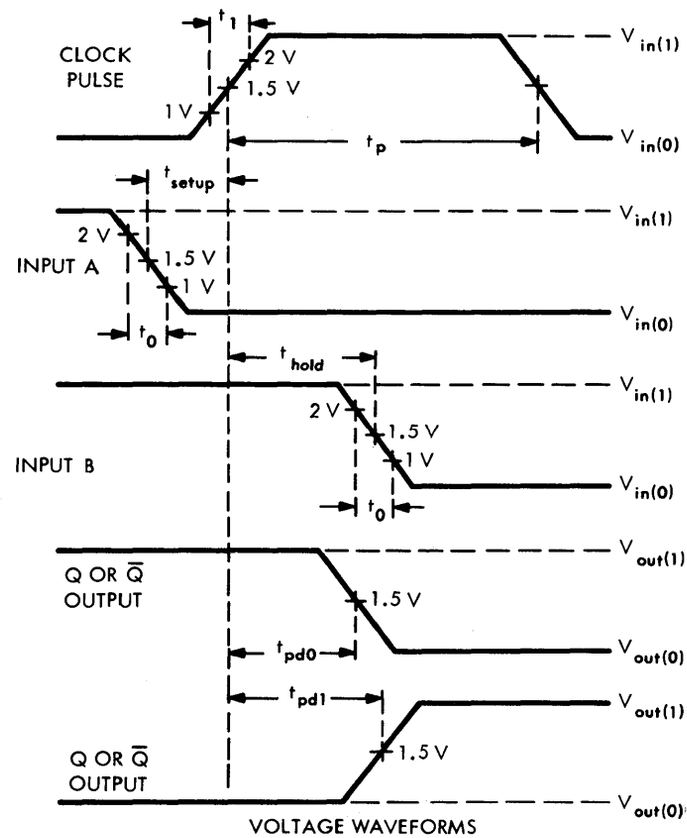
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY + 2.4 V	GND
1	t_{setup} at J★	J★	None	J1, J2, K1, K2	K★
2	t_{hold} at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	t_{setup} at K★	K★	None	J1, J2, K1, K2	J★
4	t_{hold} at K1, K2	None	K1, K2	J1, J2	J★ and K★

NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure t_{setup} and t_{hold}.
2. Clock frequency, t_{pd1}, and t_{pd0} (from clock to output) are measured in the toggle mode. Hold J = K = logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, t_1 = 15 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.
4. Input pulse characteristics: $V_{in(0)}$ = 0.4 V, $V_{in(1)}$ = 2.4 V, t_0 = 3 to 6 ns.
5. All transistors are 2N2368.
6. All diodes are 1N916.
7. C_1 includes probe and jig capacitance.

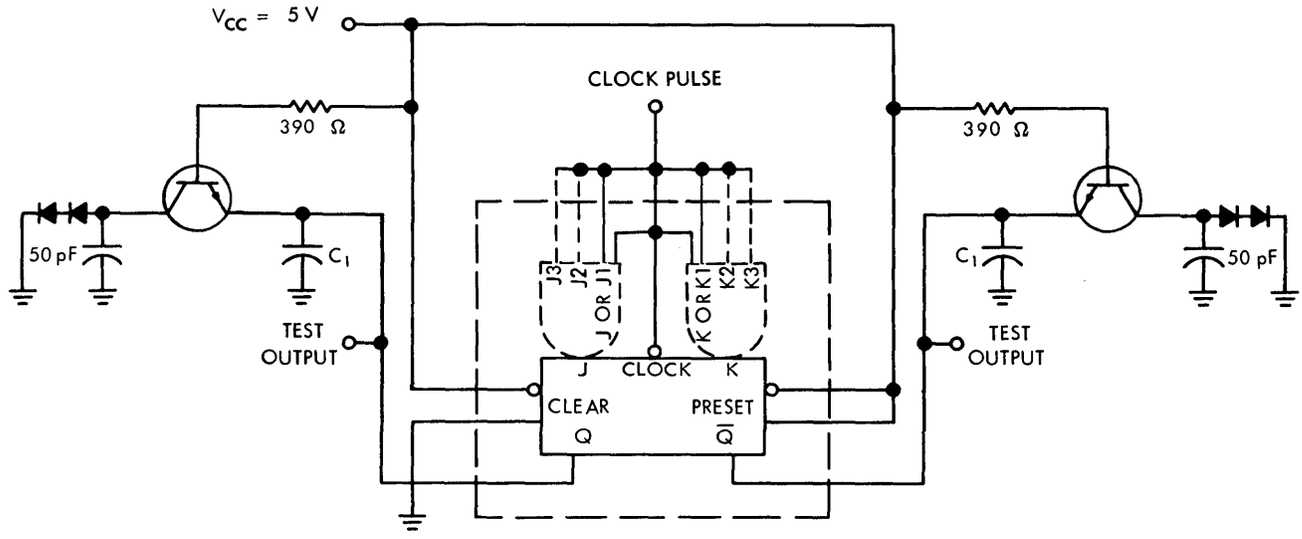


VOLTAGE WAVEFORMS

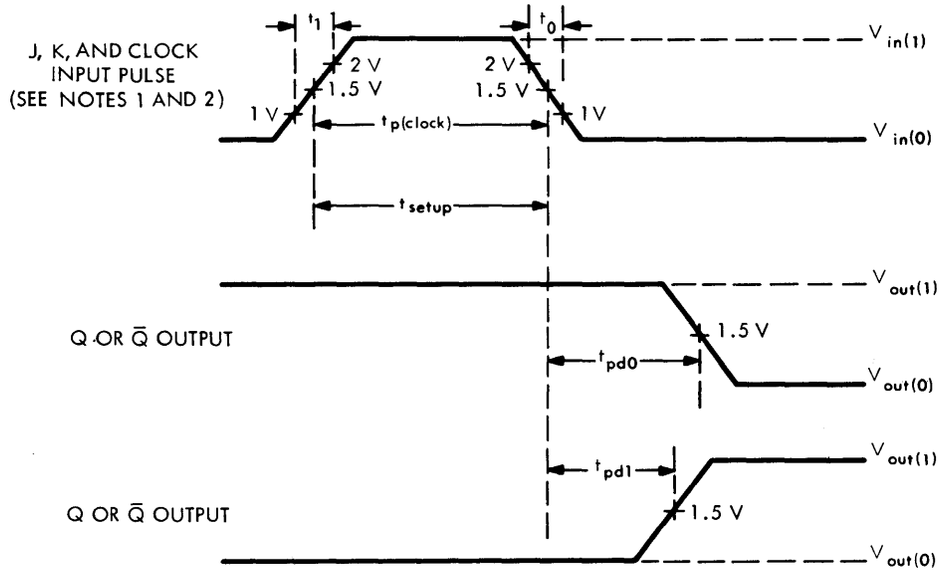
FIGURE 53 — SN7470 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

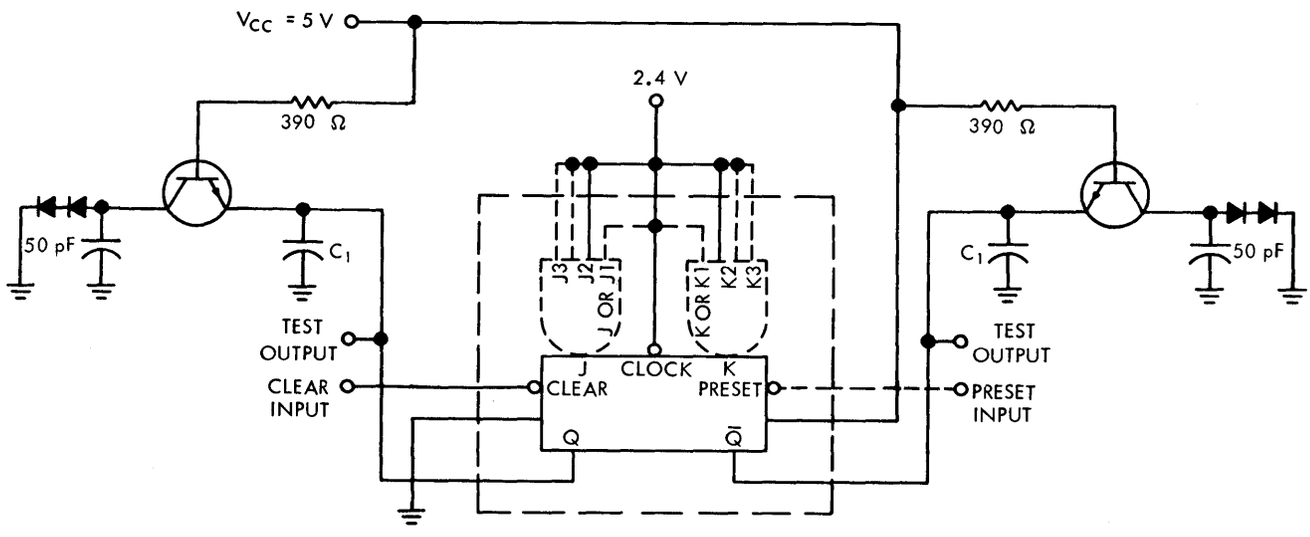
NOTES: 1. Clock, J, and K input pulse characteristics: $V_{in(0)}$ = 0.4 V, $C_{in(1)}$ = 2.4 V, t_1 = t_0 = 15 ns, t_p = 20 ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. For the SN7472, J = J1 • J2 • J3 and K = K1 • K2 • K3.
3. Gated inputs (shown with dotted lines) are for the SN7472 only. The SN7473 Dual Flip-Flop has direct J and K inputs and preset is not available.
4. All transistors are 2N2368.
5. All diodes are 1N916.
6. C_1 includes probe and jig capacitance.

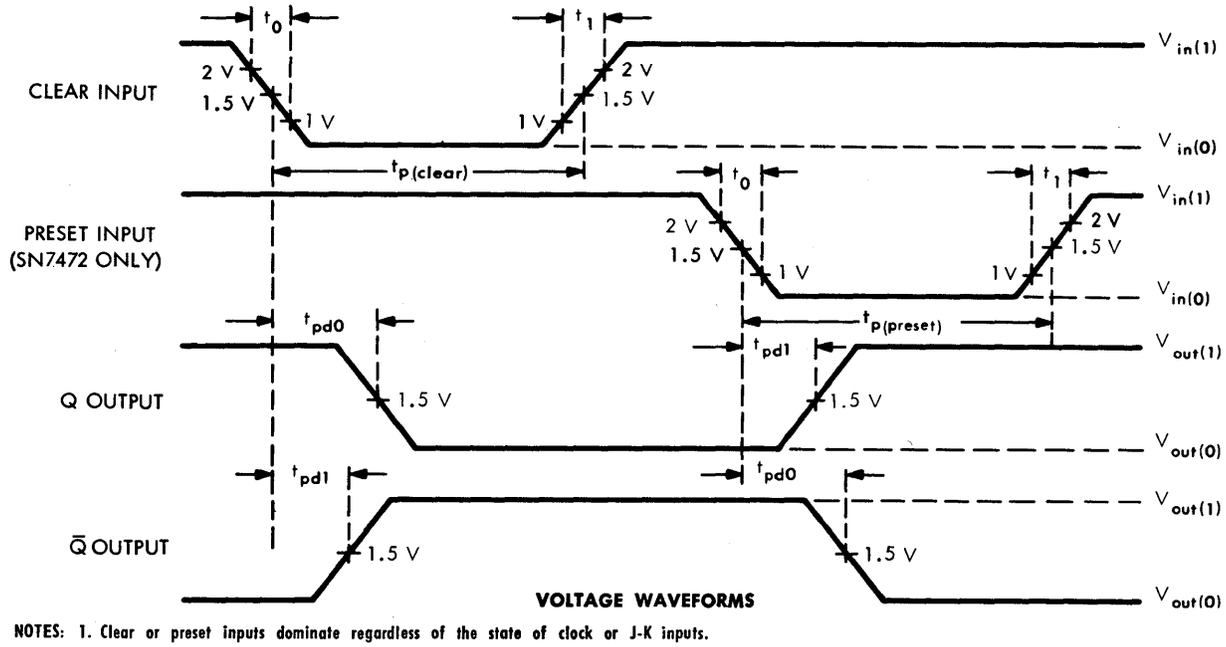
FIGURE 54 — SN7472, SN7473 FLIP-FLOP SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or J-K inputs.

2. *Clear or preset input pulse characteristics:* $V_{in(0)} = 0.4$ V, $V_{in(1)} = 2.4$ V, $t_1 = t_0 = 15$ ns, $t_{p(clear)} = t_{p(preset)} = 25$ ns, and PRR = 1 MHz.

3. Gated inputs (shown with dotted lines) are for the SN7472 only. The SN7473 Dual Flip-Flop has direct J and K inputs and preset is not available.

4. All transistors are 2N2368.

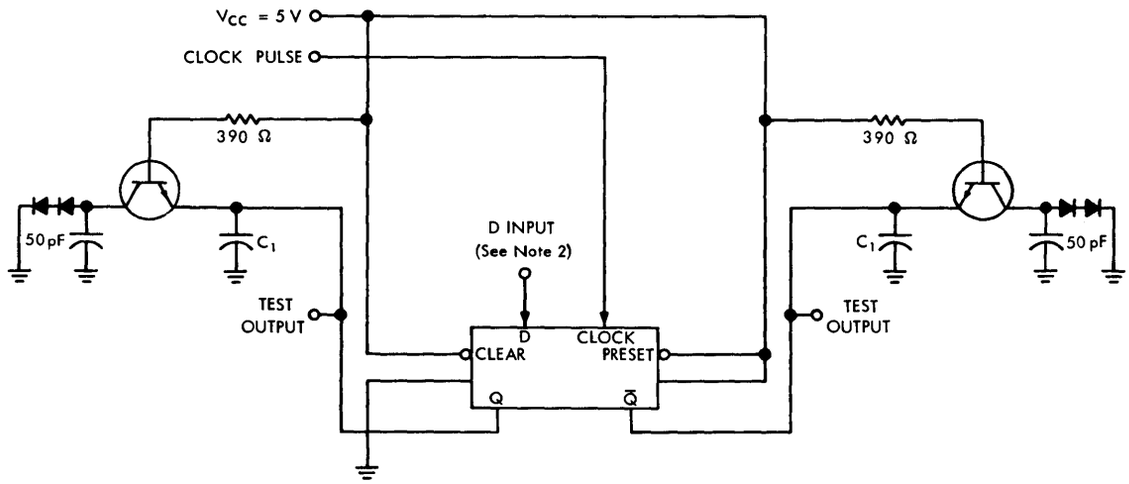
5. All diodes are 1N916.

6. C_1 includes probe and jig capacitance.

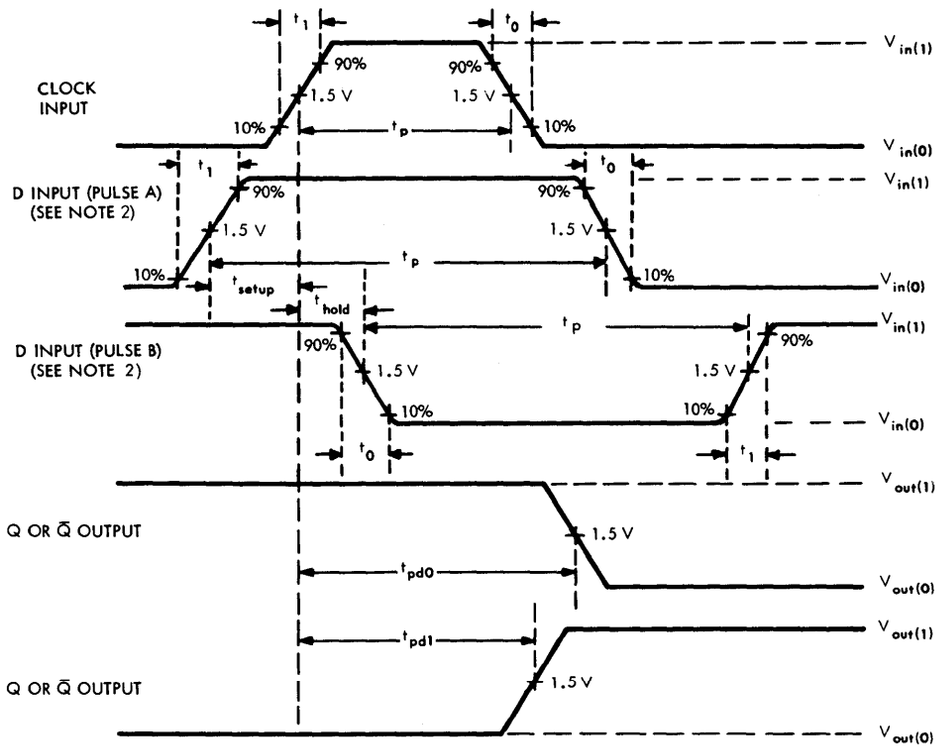
FIGURE 55 — SN7472 AND SN7473 PRESET/CLEAR PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Clock input pulse has the following characteristics: $V_{in(0)} = 0.4$ V, $V_{in(1)} = 2.4$ V, $t_1 = t_0 = 15$ ns, $t_p = 30$ ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. D input (pulse A) is used to measure t_{pd1} at Q and t_{pd0} at $\bar{Q}$. Pulse B is used to measure t_{pd1} at $\bar{Q}$ and t_{pd0} at Q. D input (pulse A) has the following characteristics: $t_1 = t_0 = 15$ ns, $t_{setup} = 20$ ns, $t_p = 60$ ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: $t_1 = t_0 = 15$ ns, $t_{hold} = 5$ ns, $t_p = 60$ ns, and PRR is 50% of the clock PRR.

3. All transistors are 2N2368.

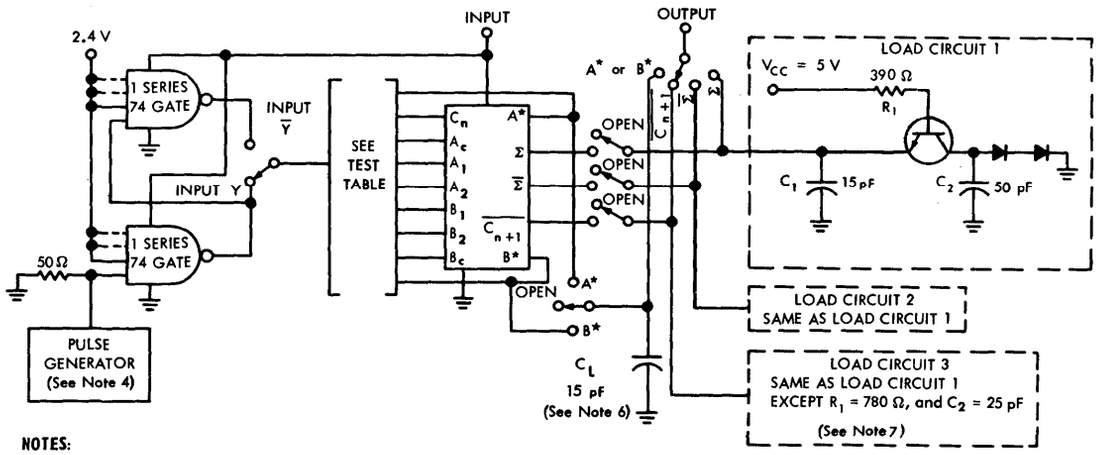
4. All diodes are 1N916.

5. C_1 includes probe and jig capacitance.

FIGURE 56 — SN7474 FLIP-FLOP SWITCHING TIME

PARAMETER MEASUREMENT INFORMATION

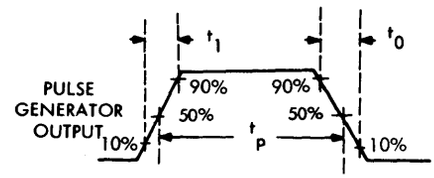
switching characteristics (continued)



NOTES:

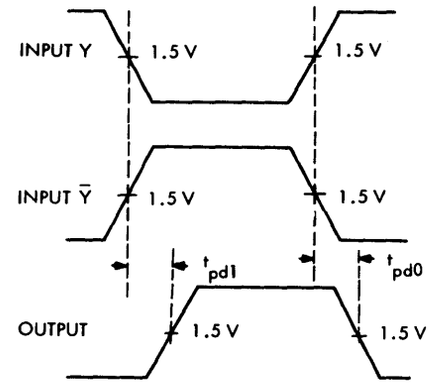
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L and C_1 include probe and jig capacitance.
7. Load circuit 3 simulates output load of 5.
8. All transistors are 2N2368.
9. All diodes are 1N916.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)

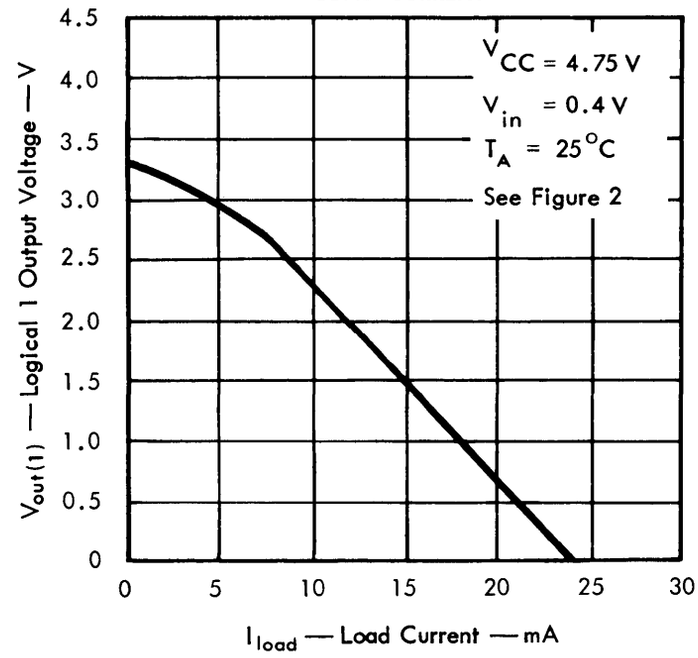


VOLTAGE WAVEFORMS

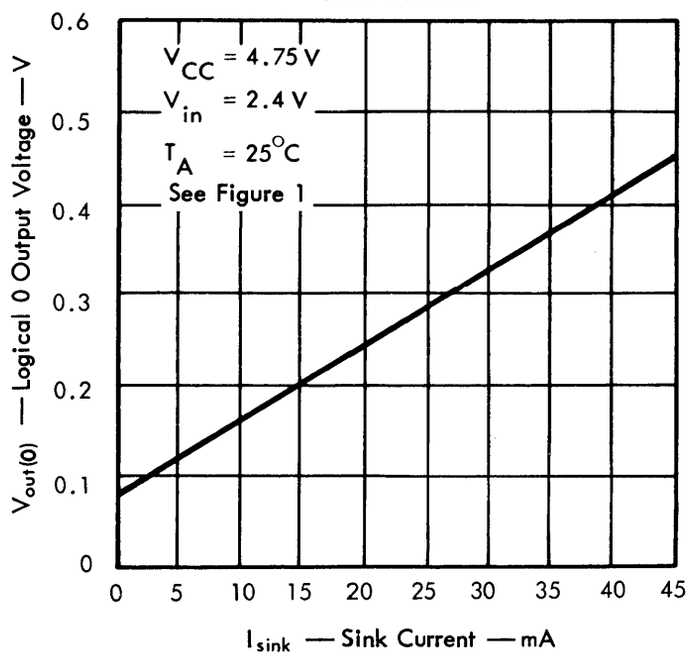
FIGURE 57 — SN7480 SWITCHING TIMES

TYPICAL CHARACTERISTICS §

LOGICAL 1 OUTPUT VOLTAGE vs LOAD CURRENT



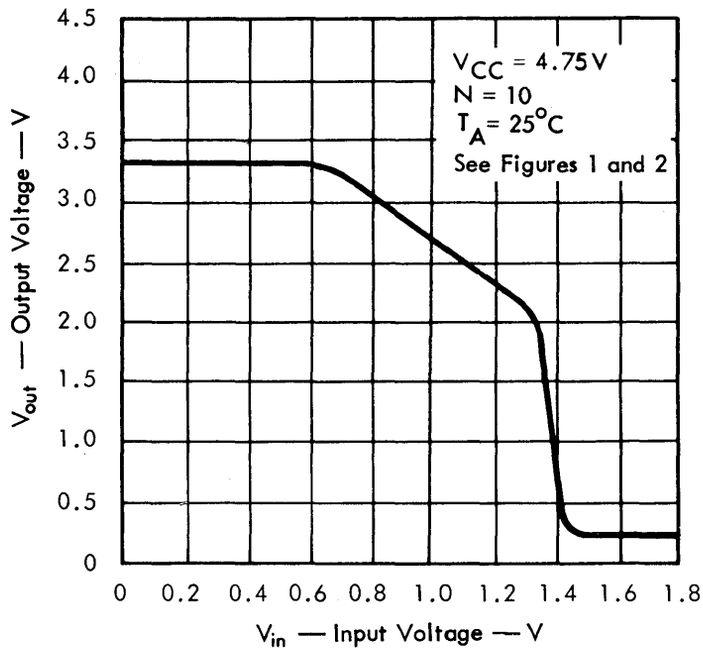
LOGICAL 0 OUTPUT VOLTAGE vs SINK CURRENT



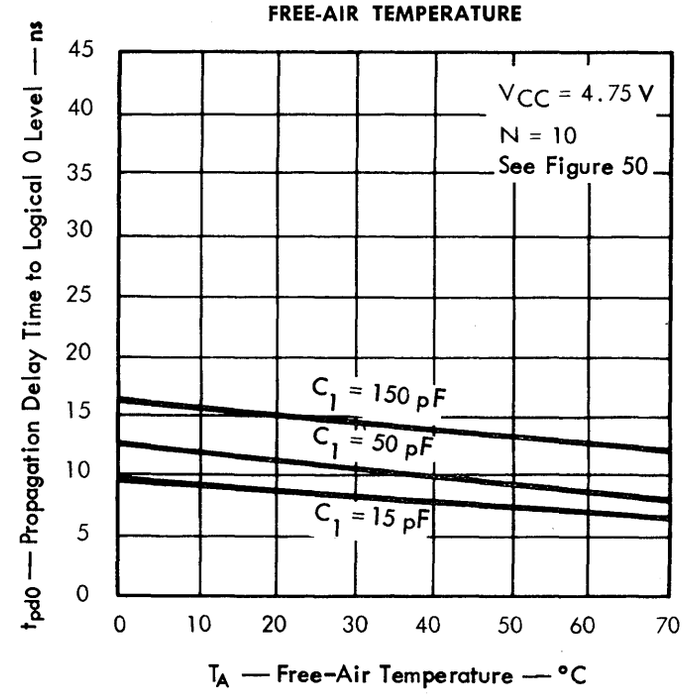
§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.

TYPICAL CHARACTERISTICS §

OUTPUT VOLTAGE vs INPUT VOLTAGE



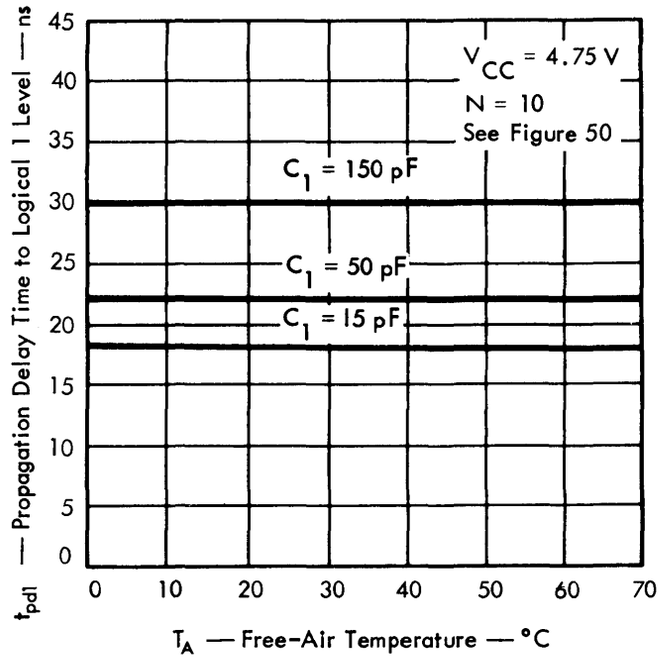
PROPAGATION DELAY TIME TO LOGICAL 0 LEVEL vs FREE-AIR TEMPERATURE



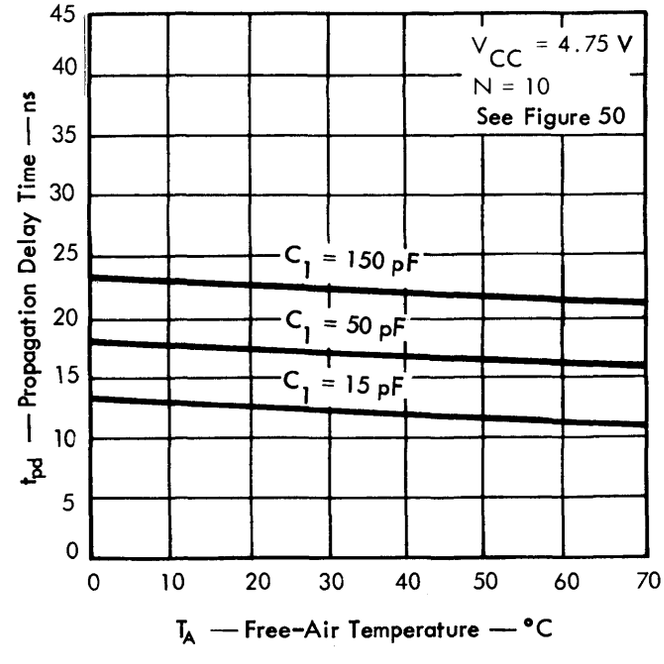
§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.

TYPICAL CHARACTERISTICS §

PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.

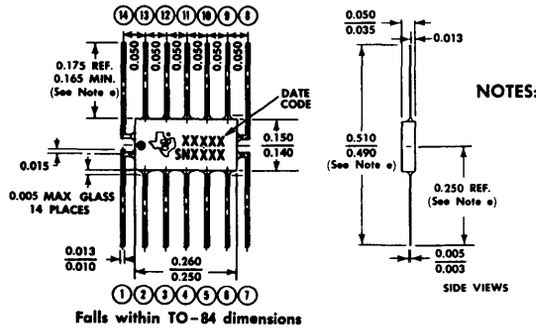
SERIES 74
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

general

Series 74 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 74 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE

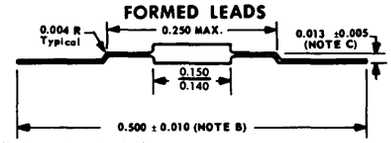


NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.

FORMED LEADS



NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

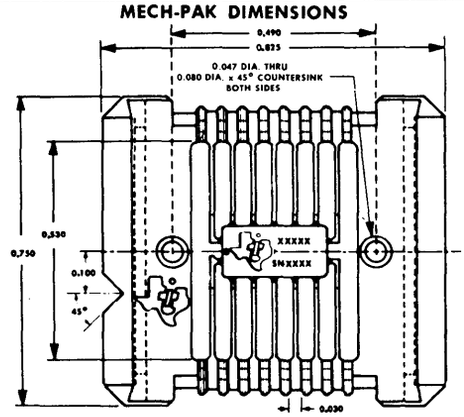
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 74 930
BULLETIN NO. DL-S 669227, NOVEMBER 1966

HIGH-SPEED TTL DIGITAL SEMICONDUCTOR NETWORKS IN DTL PIN CONFIGURATIONS

description

Series 74 930 consists of Texas Instruments high-speed TTL circuits with pin configurations and logic functions that make them electrically compatible and mechanically interchangeable with Series 15 830 DTL circuits. In addition to five interchangeable networks, an 8-input NAND gate and a dual AND-OR-INVERT gate are available.

comparative features

	SERIES 15 830 DTL	SERIES 74 930 TTL
Gate propagation delay time (typically)	**25 ns**	**13 ns**
Fan-out capability (DTL can drive 8 DTL or 5 TTL loads, TTL can drive 10 TTL or 10 DTL loads)	**8**	**10**
Noise immunity (guaranteed)	**350 mV**	**400 mV**

standard line summary

FUNCTION	TYPES	SIMILAR DTL CIRCUIT
Dual 4-Input Positive NAND Gate	SN74 930	SN15 830
Dual 4-Input Positive NAND Buffer	SN74 932	SN15 832
Quadruple 2-Input Positive NAND Gate	SN74 946	SN15 846
Triple 3-Input Positive NAND Gate	SN74 962	SN15 862
8-Input Positive NAND Gate	SN74 965	None
Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN74 966	None
Master-Slave Flip-Flop	SN74 948	SN15 831/SN15 845/SN15 848

specifications

Schematic diagrams, fan-out rules, maximum ratings, temperature ranges, and electrical characteristics are identical to those of the corresponding Series 74 type number.

SERIES 74 930 TYPE	CORRESPONDING SERIES 74 TYPE
SN74 930	SN7420
SN74 932	SN7440
SN74 946	SN7400
SN74 948	See Note 1
SN74 962	SN7410
SN74 965	SN7430
SN74 966	SN7451

NOTE 1: The SN74 948 has no corresponding Series 74 type. Electrical and switching characteristics are included in this data sheet.

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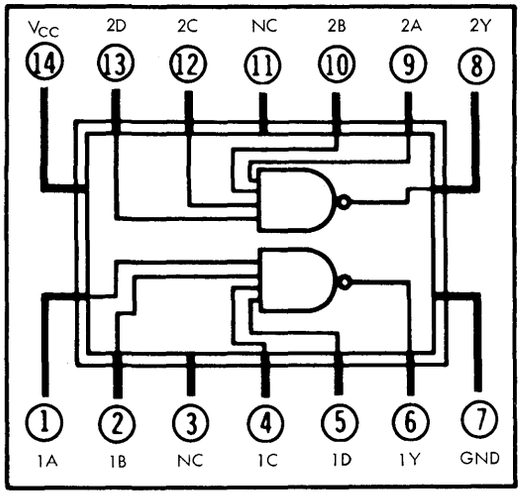
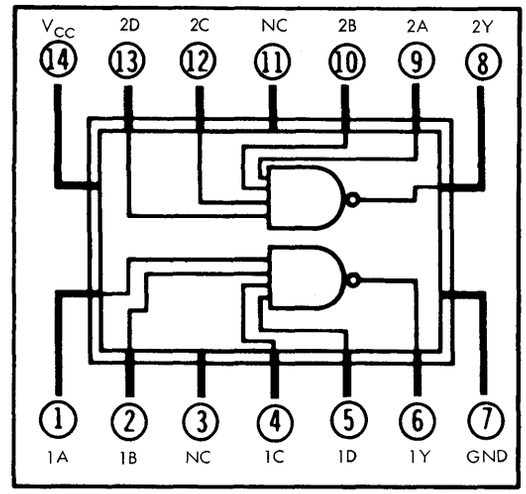
PIN CONFIGURATIONS

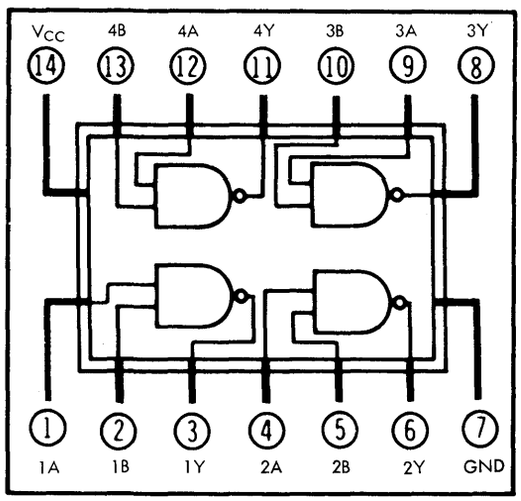
SN74 930
DUAL 4-INPUT POSITIVE NAND GATE



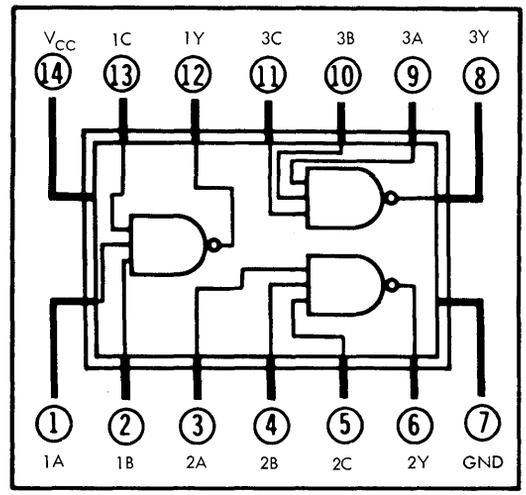
SN74 932
DUAL 4-INPUT POSITIVE NAND BUFFER



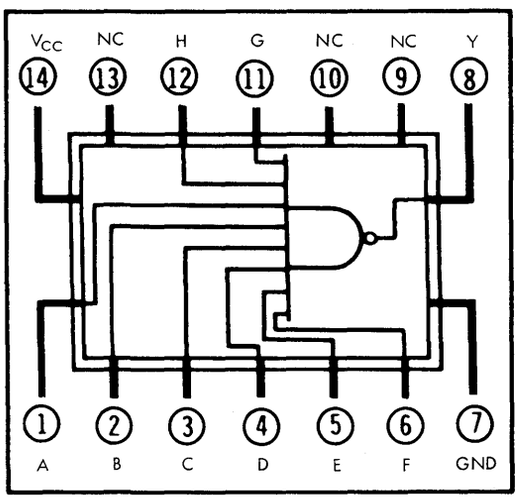
SN74 946
QUADRUPLE 2-INPUT POSITIVE NAND GATE



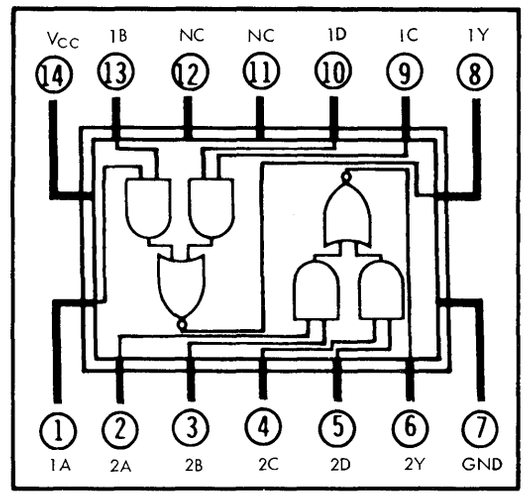
SN74 962
TRIPLE 3-INPUT POSITIVE NAND GATE



SN74 965
8-INPUT POSITIVE NAND GATE



SN74 966
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

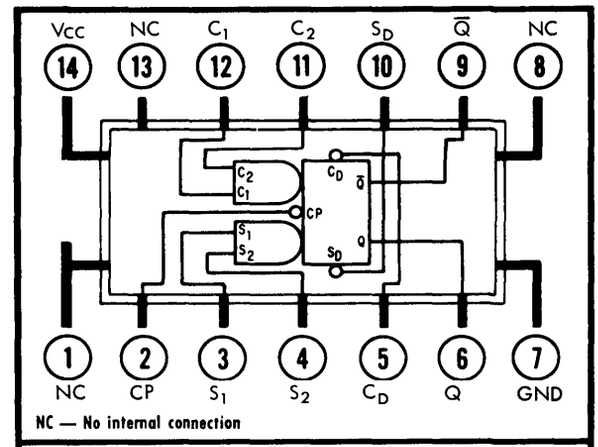


logic

TRUTH TABLES

R-S MODE					J-K MODE		
t_n				t_{n+1}	t_n		t_{n+1}
S_1	S_2	C_1	C_2	Q	S_1	C_1	Q
0	X	0	X	Qn	0	0	Qn
0	X	X	0	Qn	0	1	0
X	0	0	X	Qn	1	0	1
X	0	X	0	Qn	1	1	$\overline{Qn}$
0	X	1	1	0			
X	0	1	1	0			
1	1	0	X	1			
1	1	X	0	1			
1	1	1	1	Indeterminate			

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to C_D sets Q to logical 0

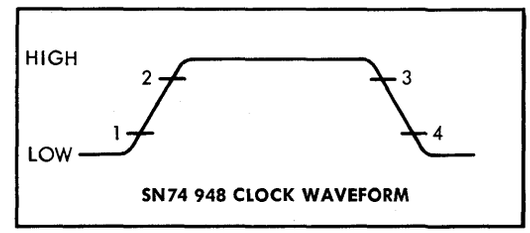
Low input to S_D sets Q to logical 1

C_D and S_D are independent of CP

description

The SN74 948 flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.



SN74 948 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 6)	$\geq$ 20 ns
Width of Direct Set Pulse, $t_{p(SD)}$ (See Figure 7)	$\geq$ 25 ns
Width of Direct Clear Pulse, $t_{p(CD)}$ (See Figure 7)	$\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 6)	applied clock pulse width
Input Hold Time, t_{hold}	$\geq$ 0

electrical characteristics, T_A = 0°C to 70°C

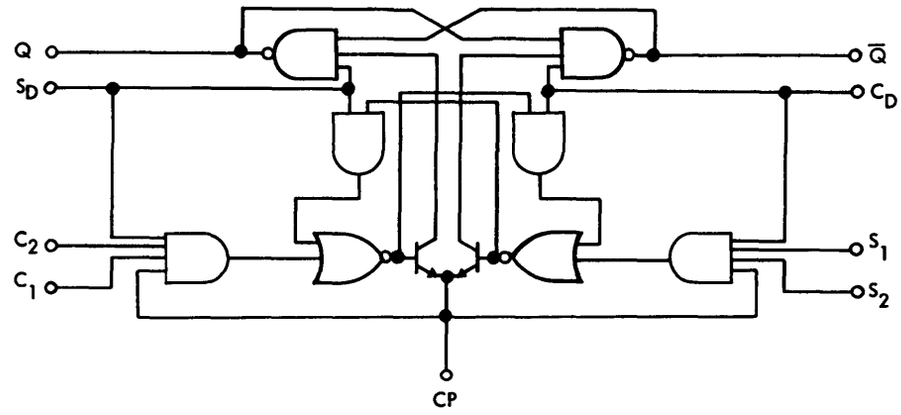
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	1	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Logical 0 input voltage	1	V_{CC} = 4.75V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = 4.75 V, I_{load} = −400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	2	V_{CC} = 4.75 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at C_1, C_2, S_1, or S_2	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at C_D or S_D	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			−3.2	mA
$I_{in(0)}$	Logical 0 level input current at CP	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			−4.8	mA
$I_{in(1)}$	Logical 1 level input current at C_1, C_2, S_1, or S_2	4	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_D or S_D	4	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at CP	4	V_{CC} = 5.25 V, V_{in} = 2.4 V			120	μA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current †	5	V_{CC} = 5.25 V, V_{in} = 0	−18		−57	mA
I_{CC}	Supply current	4	V_{CC} = 5 V, V_{in} = 5 V		8		mA

† Not more than one output should be shorted at a time.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

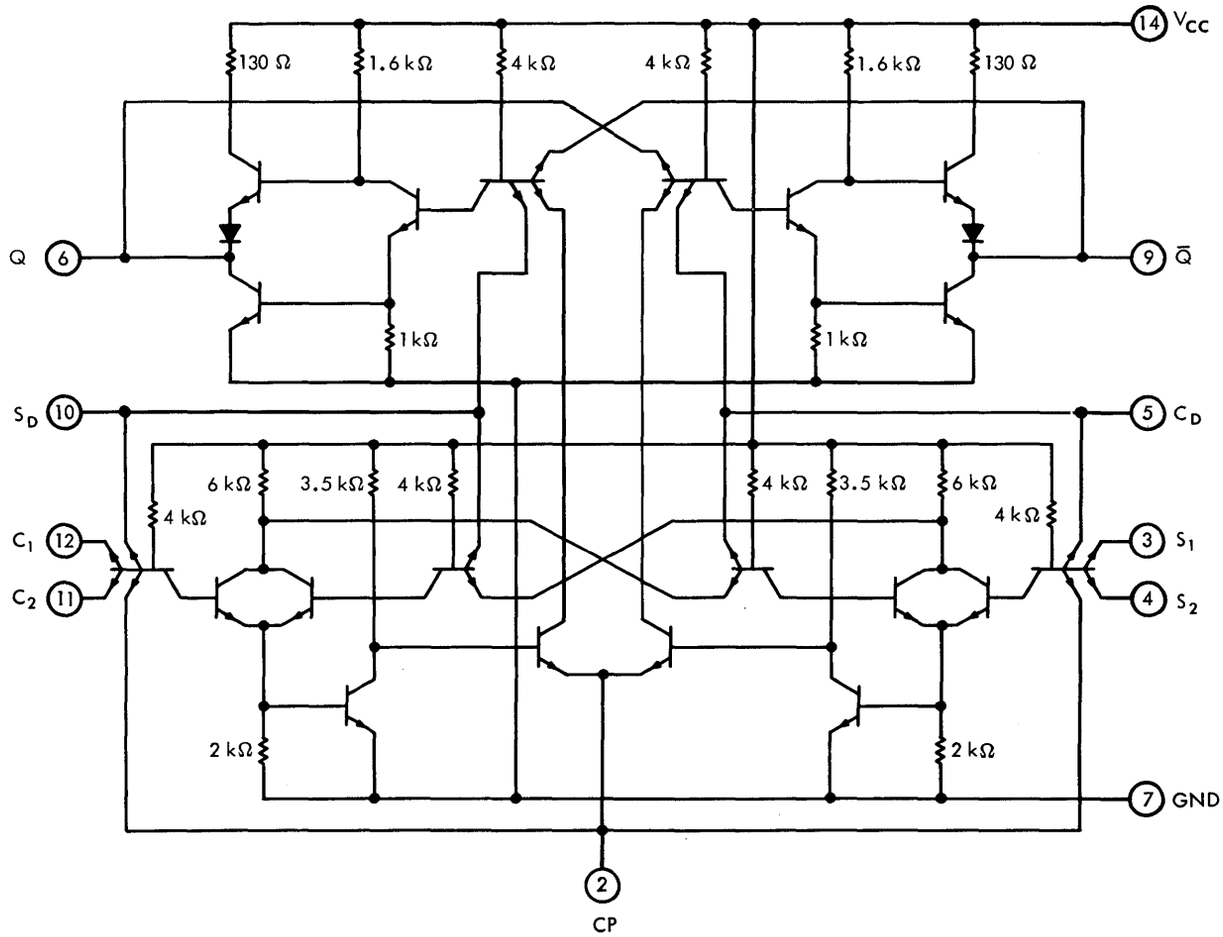
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	6		10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from C_D or S_D to output	7			26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from C_D or S_D to output	7			34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from C_1, C_2, S_1, or S_2 to output	6		10	26	50	ns
t_{pd0}	Propagation delay time to logical 1 level from C_1, C_2, S_1, or S_2 to output	6		10	34	50	ns

functional block diagram

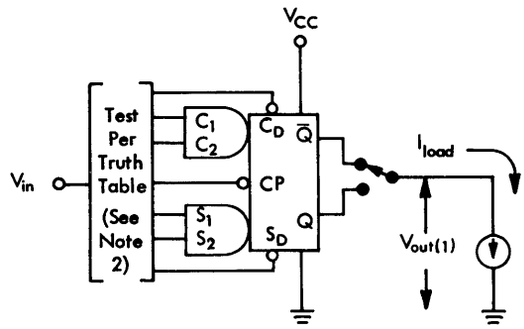


schematic



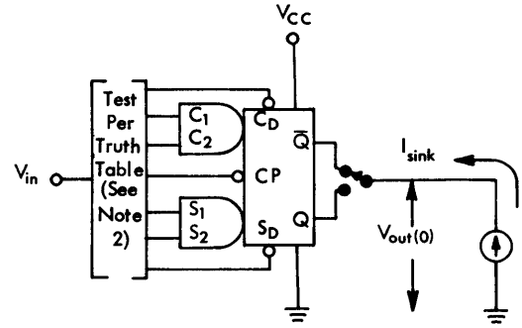
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



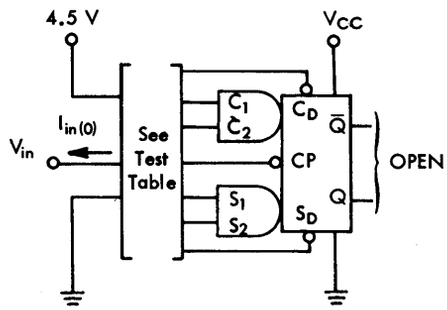
1. *Each output is tested separately.*
2. Direct inputs C_D and S_D are tested for proper operation.

FIGURE 1



1. *Each output is tested separately.*
2. Direct inputs C_D and S_D are tested for proper operation.

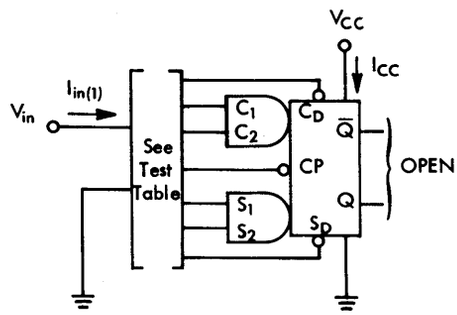
FIGURE 2



1. Each input is tested separately.

TEST TABLE		
Apply V_{in} (Test I_{in})	Apply Momentary GND, Then 4.5 V	Apply 4.5 V
CP	C_D	C_1, C_2, S_1, S_2, and S_D
CP	S_D	C_1, C_2, S_1, S_2, and C_D
C_D	None	S_1, S_2, and CP
S_D	None	C_1, C_2, and CP
C_1	None	C_2, S_D, and CP
C_2	None	C_1, S_D, and CP
S_1	None	S_2, C_D, and CP
S_2	None	S_1, C_D, and CP

FIGURE 3



1. Each input is tested separately.
2. When testing I_{CC}, all inputs and outputs are open.

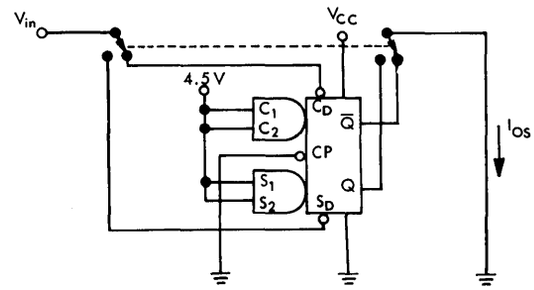
TEST TABLE	
Apply V_{in} (Test I_{in})	Ground
CP	C_D, S_D, C_1, C_2, S_1, and S_2
C_D	CP, S_1, and S_2
S_D	CP, C_1, and C_2
C_1	CP, S_D, and C_2
C_2	CP, S_D, and C_1
S_1	CP, C_D, and S_2
S_2	CP, C_D, and S_1

FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

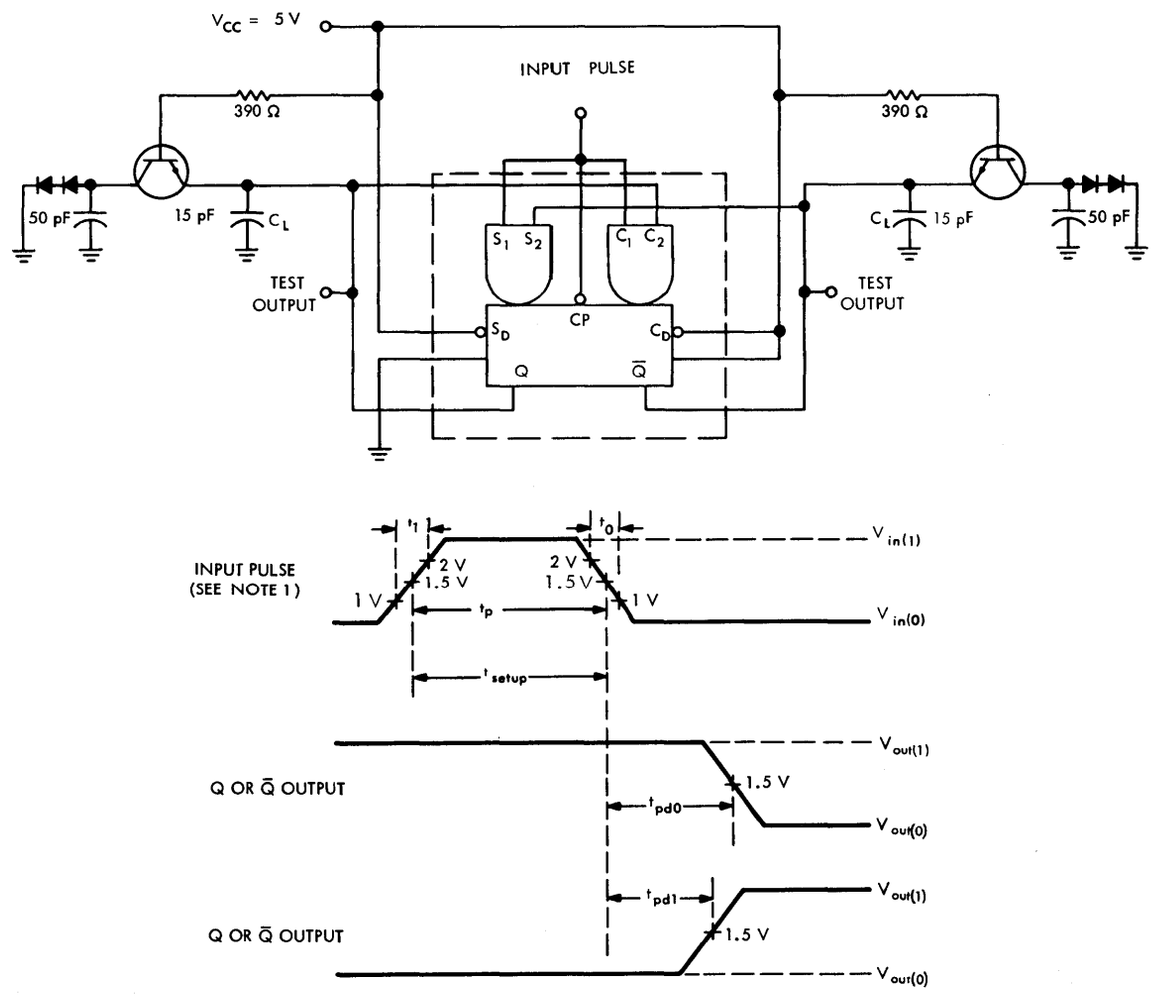


1. Each output is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow.

switching characteristics



NOTES: 1. Input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 \leq 15$ ns, $t_p = 20$ ns, and PRR = 1 MHz. When testing f_{clock}, vary PRR.

2. All transistors are 2N2368.

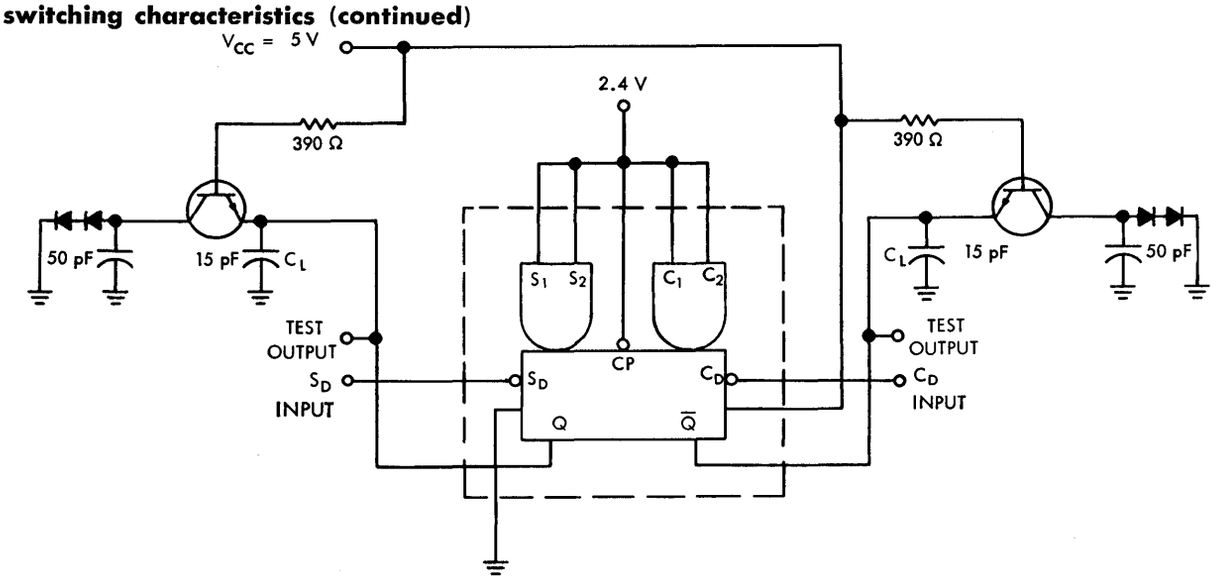
3. All diodes are 1N916.

4. C_L includes probe and jig capacitance.

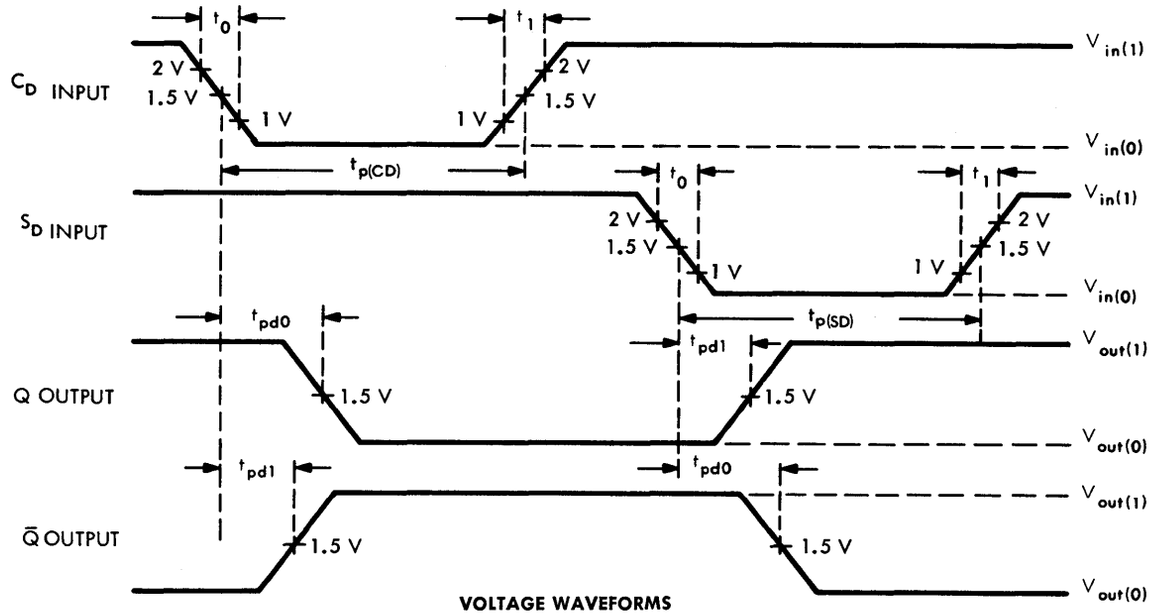
FIGURE 6 — PROPAGATION DELAY TIMES FROM CLOCKED INPUTS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. C_D or S_D inputs dominate regardless of the state of clock, C_1, C_2 or S_1, S_2 inputs.

2. C_D or S_D input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 \leq 15$ ns, $t_{p(CD)} = t_{p(SD)} = 25$ ns, and PRR = 1 MHz.

3. All transistors are 2N2368.

4. All diodes are 1N916.

5. C_L includes probe and jig capacitance.

FIGURE 7 — C_D AND S_D PROPAGATION DELAY TIMES

SERIES 74N
BULLETIN NO. DL-S 668940, OCTOBER 1966

TRANSISTOR-TRANSISTOR-LOGIC SEMICONDUCTOR NETWORKS IN MOLDED PLUG-IN PACKAGES

description

Series 74N consists of the Series 74 general-purpose TTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 70°C.

features

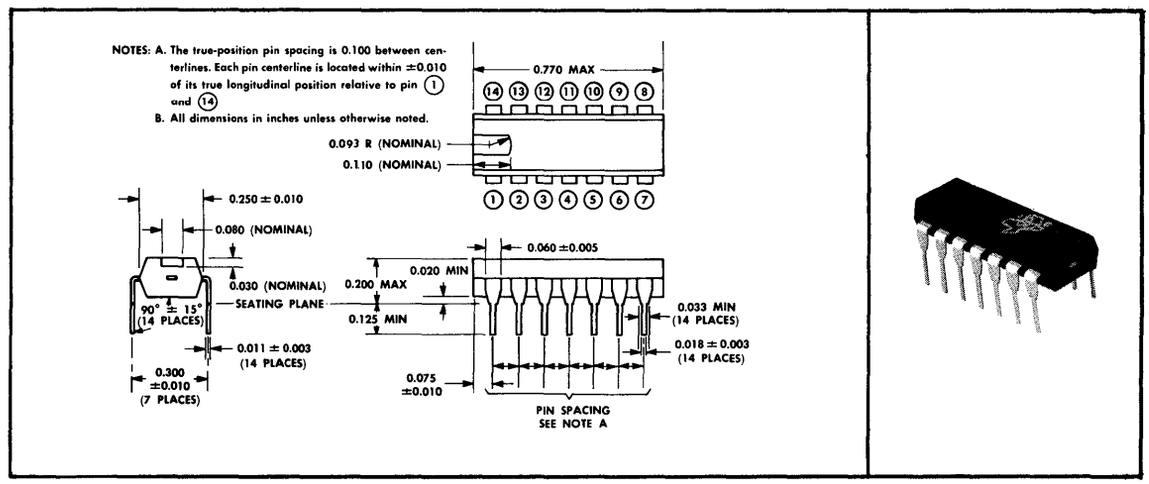
- **high speed — typical gate propagation delay time of 13 ns**
- **high d-c noise margin — typically 1 V**
- **low power dissipation — 10 mW per gate at 50% duty cycle**
- **low output impedance — less than 100 Ω at logical 1 output state**
- **full fan-out of 10**
- **plug-in configuration ideal for flow-soldering techniques**
- **pins on 100-mil grid spacings for industrial-type circuit-boards**

specifications, logic symbols, and terminal designations

Schematic diagrams, fan-out rules, maximum ratings, and electrical characteristics for Series 74N networks are identical to those of the corresponding Series 74 type number. Terminal designations for the Series 74N networks are shown in this data sheet.

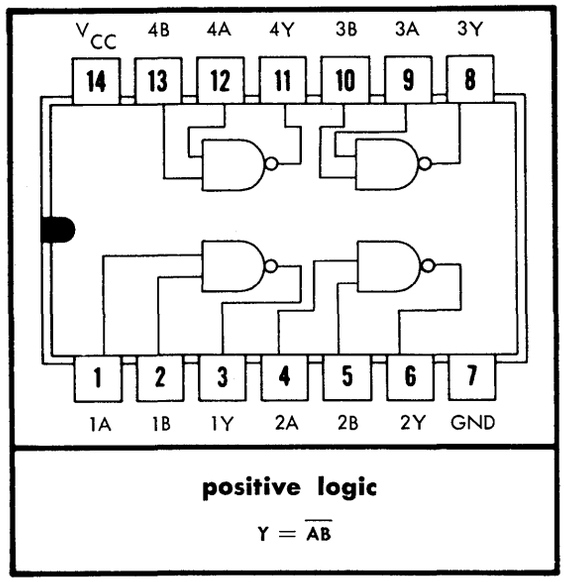
mechanical data

Series 74N networks are mounted on a 14-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions.



†Patented by Texas Instruments

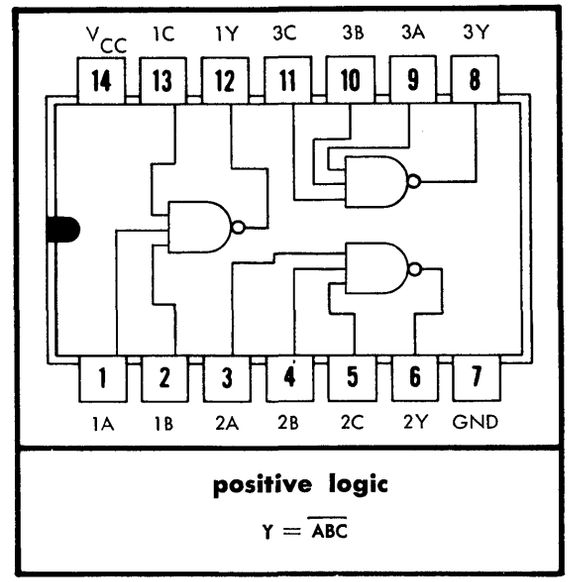
SN7400N
QUADRUPLE 2-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{AB}$

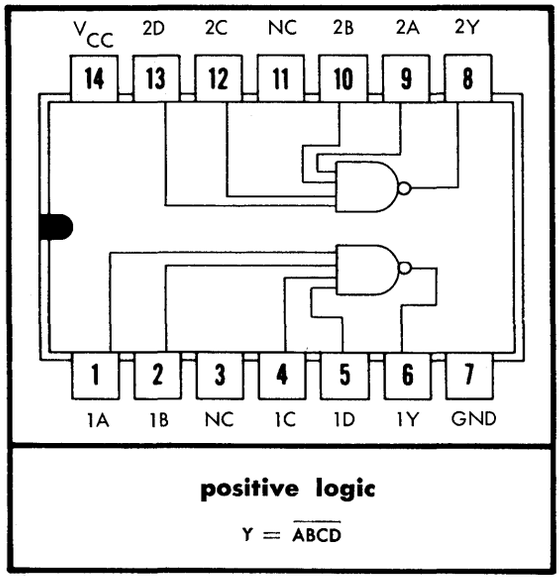
SN7410N
TRIPLE 3-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{ABC}$

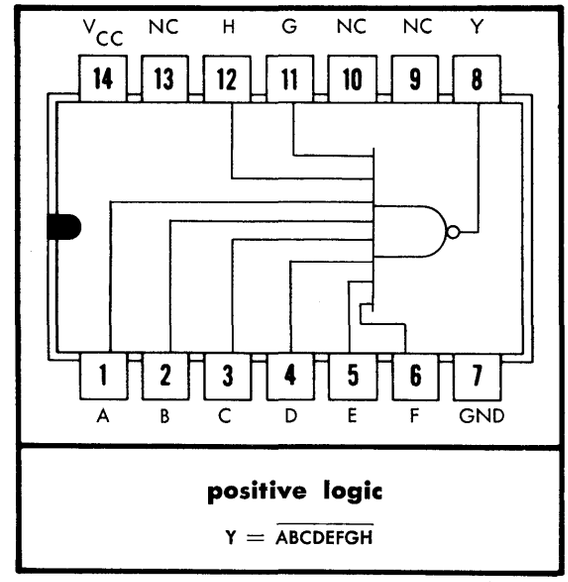
SN7420N
DUAL 4-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{ABCD}$

SN7430N
8-INPUT POSITIVE NAND GATE

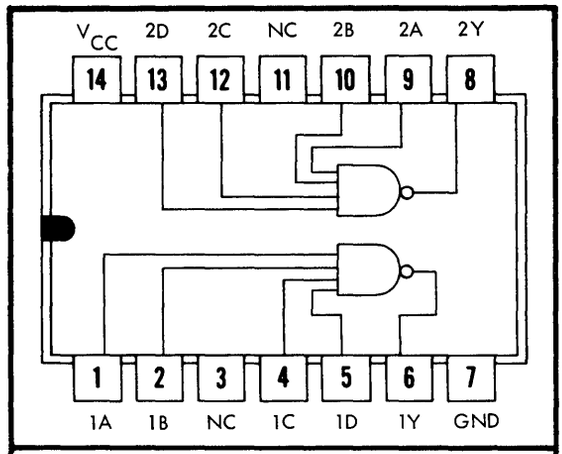


positive logic

$Y = \overline{ABCDEFGH}$

NC — No internal connection.
†Patented by Texas Instruments

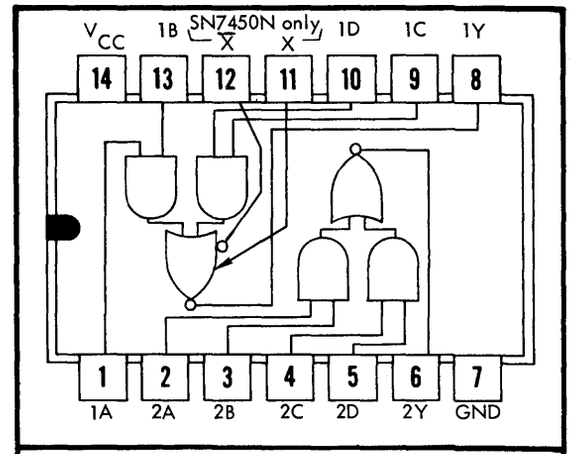
SN7440N
DUAL 4-INPUT POSITIVE NAND BUFFER



positive logic

$Y = \overline{ABCD}$

SN7450N/SN7451N
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

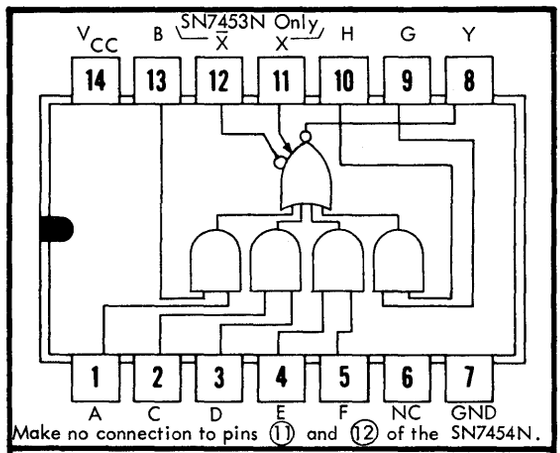


positive logic

$Y = \overline{(AB) + (CD) + X}$
$X = ABCD$ from SN7460N

NOTE: Expander nodes X and $\overline{X}$ are on the SN7450N only.
Make no external connection to pins (11) and (12) of the SN7451N.

SN7453N, SN7454N
4-WIDE 2-INPUT AND-OR-INVERT GATES

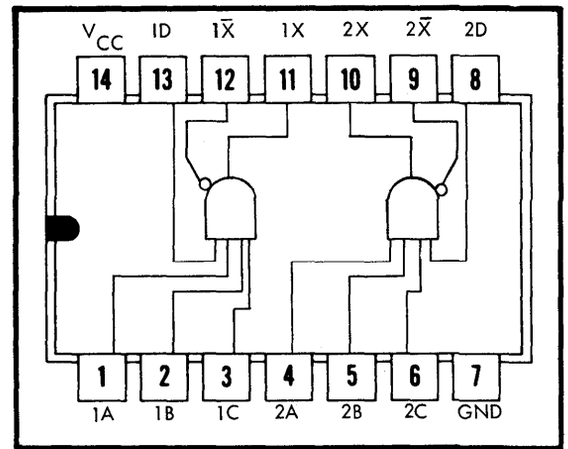


positive logic

$Y = \overline{(AB) + (CD) + (EF) + (GH) + X}$
$X = ABCD$ from SN7460N

NOTE: Expander nodes X and $\overline{X}$ are on the SN7453N only.

SN7460N
DUAL 4-INPUT EXPANDER



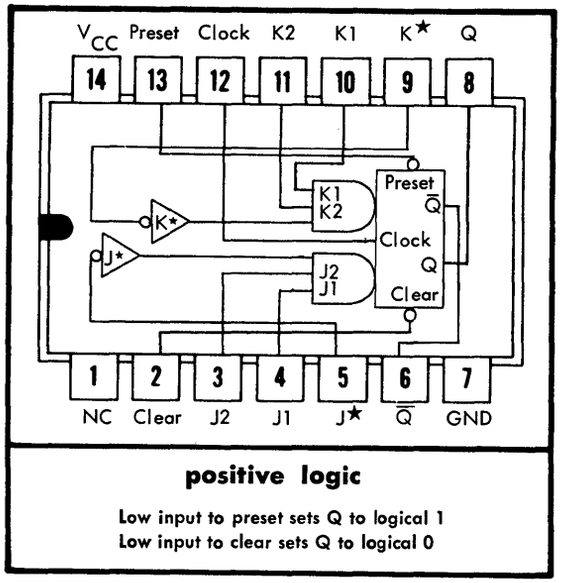
positive logic

$X = ABCD$

NOTE: Connect pin (9) or (12) to pin (12) of SN7450N or SN7453N.
Connect pin (10) or (11) to pin (11) of SN7450N or SN7453N.

NC — No internal connection.
†Patented by Texas Instruments

SN7470N
J-K FLIP-FLOP



positive logic

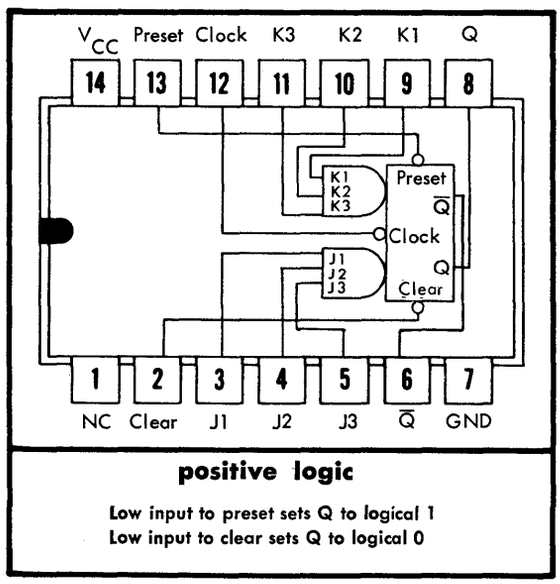
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

NOTE: Clock must be at logical 0 prior to the application of preset or clear functions.

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. $J = J1 \cdot J2 \cdot \overline{J★}$
2. $K = K1 \cdot K2 \cdot \overline{K★}$
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.
5. If inputs J★ or K★ are not used they must be grounded.

SN7472N
J-K MASTER-SLAVE FLIP-FLOP



positive logic

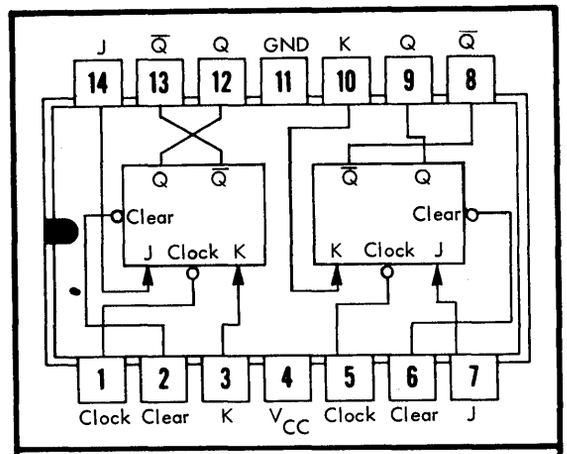
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.

NC — No internal connection.
†Patented by Texas Instruments

SN7473N
DUAL J-K MASTER-SLAVE FLIP-FLOP



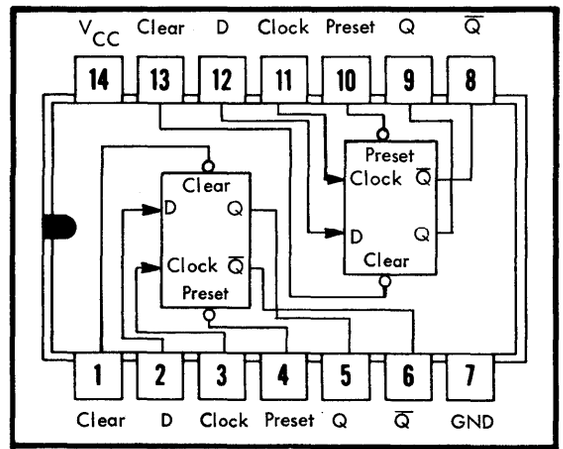
positive logic

Low input to clear sets Q to logical 0 regardless of clock state.

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

SN7474N
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



positive logic

a. Low input to clear sets Q to logical 0.
b. Low input to preset sets Q to logical 1.
c. Clear or preset inputs dominate regardless of clock and D inputs

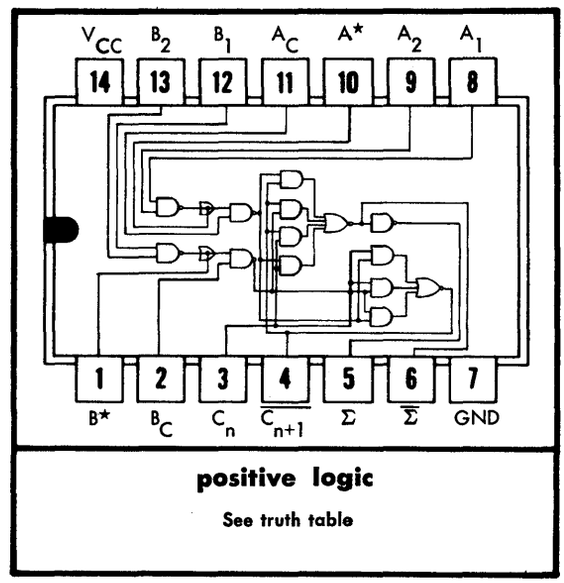
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

†Patented by Texas Instruments

SN7480N
GATED FULL ADDER



positive logic

See truth table

TRUTH TABLE
(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES: 1. $A = \overline{A★ \cdot A_C}$, $B = \overline{B★ \cdot B_C}$ where $A★ = \overline{A_1 \cdot A_2}$ and $B★ = \overline{B_1 \cdot B_2}$.
2. When A★ or B★ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A★ or B★ respectively must be open, or used to perform Dot-OR logic.

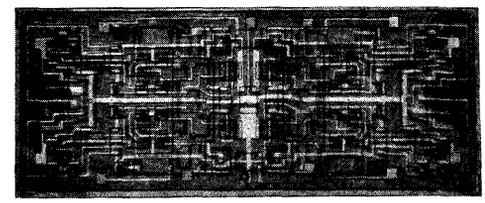
†Patented by Texas Instruments

SERIES 73
BULLETIN NO. DL-S 669019, OCTOBER 1966
REPLACES BULLETIN NO. DL-S 657650, JULY 1965

DIGITAL SEMICONDUCTOR NETWORKS FOR INDUSTRIAL APPLICATIONS

application

Series 73 semiconductor networks are ideally suited for general-purpose digital applications, including computer, data handling, and control systems. Series 73 is designed and characterized for use in environmental conditions found in industrial applications.



DUAL J-K FLIP-FLOP BAR

features

LOW SYSTEM COST

- **multifunction devices offering lowest cost per logic function**

ADVANCED PERFORMANCE

- **optimum speed/power ratio for industrial applications**
- **guaranteed d-c margin**
- **high a-c noise rejection from low output impedance**
- **waveshape integrity maintained over rated temperature and loading conditions by double-ended output stage**

EASE OF DESIGN

- **most complete industrial family available — 14 networks**
- **modified DTL circuitry simplifies system design**
- **fan-out of 10 from each output**

description

Series 73 is a compatible line of digital semiconductor networks capable of performing all basic and some special logic functions. All basic logic functions are offered as multi-function networks. Utilization of this complete line of compatible networks reduces systems engineering design time, while the use of multi-function networks reduces system cost per logic function.

Series 73 logic employs a modified form of diode-transistor logic (DTL) where transistors replace conventional diodes in order to improve circuit performance. Input transistors improve drive capability while offset transistors improve switching speed. The Series 73 low-impedance output stage maintains symmetrical waveshapes over wide ranges of d-c fan-out, capacitive loads, and operating temperatures. The low-impedance output also provides for a high degree of protection against capacitively coupled noise transients on system information lines.

CONTENTS

†Patented by Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SERIES 73
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS

typical operating characteristics, $T_A = 0°C$ to $70°C$, supply voltage $V_{CC} = 3$ v to 4 v

Speed: Gate Propagation Delay	35 nsec
Flip-flop Toggle Rate	4 Mc
Fan-Out Capability of Each Output	10
Fan-In With Expanders	25 max
D-C Margin: At Logical 1	300 mv
At Logical 0	200 mv
Output Impedance	$< 50\ \Omega$
Average Power Dissipation: Per Gate	12 mw
Per Flip-flop	40 mw

design characteristics

Series 73 is a compatible line of digital semiconductor intergrated circuits built and characterized for medium-speed applications (up to 4 Mc) in industrial environments. The networks are fabricated from triple-diffused planar silicon, and employ a modified form of diode-transistor logic selected to take advantage of inherent integrated-circuit characteristics.

As in conventional diode logic (Figure A), logic is performed at node A of a Series 73 gate (Figure B).

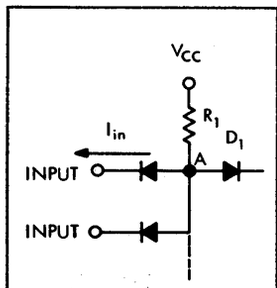


FIGURE A. Diode AND Logic

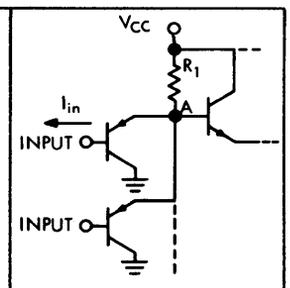


FIGURE B. Series 73 AND Logic

The gain of the p-n-p transistors replacing the input diodes increases the effective drive capability of the preceding stage. The voltage at node A is now a function of I_{in}, R_1, and the p-n-p transistor gain, rather than only I_{in} and R_1 as in diode logic. The effect of the transistor gain is to minimize the importance of the resistor value in the circuit's performance. Since silicon resistors have inherently wide production tolerances and high temperature coefficients, the transistor gain makes fabrication of Series 73 networks more economical while assuring greater stability over the temperature range.

The n-p-n transistor which replaces the offset diode D_1 also has gain, increasing the circuit drive capability and improving the waveshapes at node A.

This basic AND logic configuration is coupled with an inverting double-ended output stage (Figure C) in each Series 73 gate.

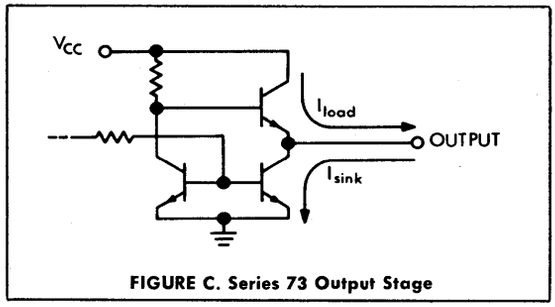


FIGURE C. Series 73 Output Stage

The most important feature of the Series 73 output stage is its ability to supply load and sink current with low output impedance. This provides high d-c fan-out to both types of loads and simplifies interface design. Low output impedance in either state ensures that turn-on and turn-off waveshapes will remain sharp and symmetrical over a wide range of d-c and capacitive loadings throughout the temperature range. The low output impedance of each output ensures that every information line will have a low-impedance termination, providing valuable protection against a-c coupled noise transients.

All Series 73 networks are fabricated using a 4-step planar diffusion process. First, an n-type diffusion is made in the p-type substrate, forming the n-p-n collectors only. A second n-type diffusion is made forming the base area of the p-n-p transistors, isolation region of the resistors, one section of the capacitors, and further forming the n-p-n collectors. This sequence reduces the n-p-n transistor $r_{CE(sat)}$ to approximately 30 ohms, while keeping the p-n-p base width narrow and the gain high (typically 12). The next step is a p-type diffusion which forms the p-n-p emitters, n-p-n bases, resistors, and another portion of the capacitors. The final diffusion is an n-type, forming the n-p-n emitters and completing the capacitors.

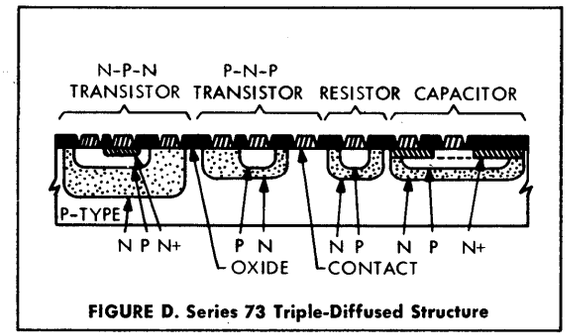
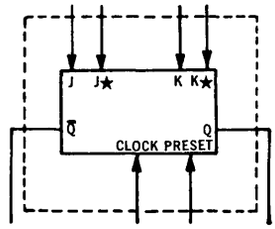


FIGURE D. Series 73 Triple-Diffused Structure

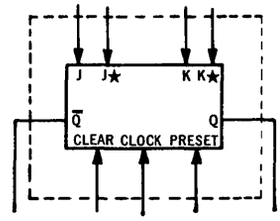
standard line summary

SN7300 See Page 6505



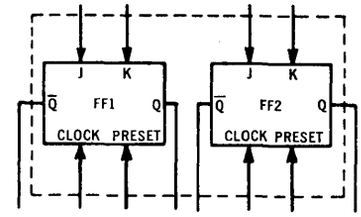
J-K FLIP-FLOP WITH PRESET

SN7301 See Page 6507



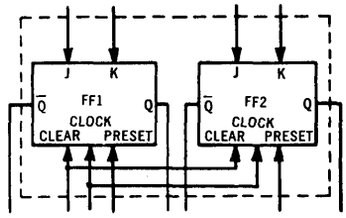
J-K FLIP-FLOP WITH PRESET AND CLEAR

SN7302 See Page 6509



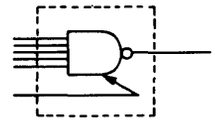
DUAL J-K FLIP-FLOP WITH PRESET

SN7304 See Page 6511



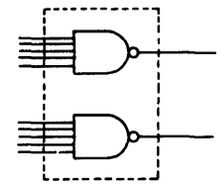
DUAL J-K
FLIP-FLOP WITH PRESET AND CLEAR

SN7310 See Page 6513



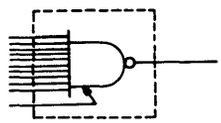
5-INPUT EXPANDABLE NAND/NOR GATE

SN7311 See Page 6515



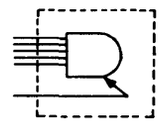
DUAL 5-INPUT NAND/NOR GATE

SN7315 See Page 6516



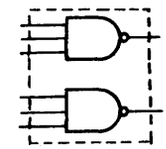
10-INPUT EXPANDABLE NAND/NOR GATE

SN7320 See Page 6517



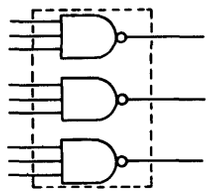
5-INPUT EXPANDER

SN7330 See Page 6518



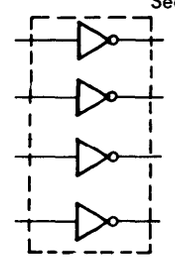
DUAL 3-INPUT NAND/NOR GATE

SN7331 See Page 6519



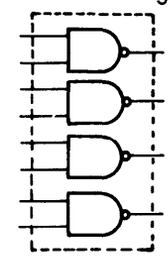
TRIPLE 3-INPUT NAND/NOR GATE

SN7350 See Page 6520



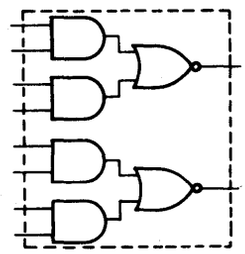
QUADRUPLE INVERTER/DRIVER

SN7360 See Page 6521



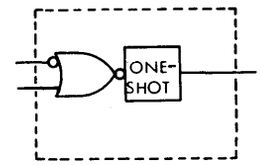
QUADRUPLE 2-INPUT NAND/NOR GATE

SN7370 See Page 6522



DUAL AND-OR-INVERT GATE

SN7380 See Page 6523



ONE-SHOT
MONOSTABLE MULTIVIBRATOR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) . . . . . +7 v
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . V_{CC}
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 125°C

NOTES: 1. *Voltage values are with respect to network ground terminal.*
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 73 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input current requirements

Weighted values of input current requirements reflect worst-case conditions for T_A = 0° to 70°C and V_{CC}=3 to 4 v. One positive load (N+ =1) requires current into the input at a logical 1 voltage level (0.5 ma at V_{CC}=3 v, and 0.8 ma at V_{CC}=4 v). One negative load (N— =1) requires current out of the input at a logical 0 voltage level (–0.2 ma). Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS

NETWORK	TYPE	INPUT	N+ LOADS	N– LOADS
FLIP-FLOPS	7300, 7301 7302	J, J★, K, K★, Preset, Clear	1	0
		Clock	2.5	2.5
	7304	J, K, Preset	1	0
		Clear	2	0
		Clock	5	5
GATES AND EXPANDER	7310, 7311 7315, 7320 7330, 7331 7360, 7370	Each Input	0	1
ONE-SHOT	7380	T, T★	1	0
INVERTER	7350	Each Input	2	0

output drive capability

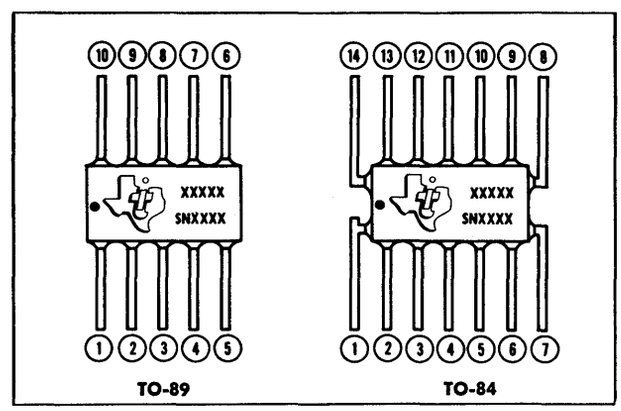
Weighted values of fan-out reflect the ability of an output to drive current to N + loads and sink current from N– loads under worst-case conditions. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF FAN-OUT

NETWORK	OUTPUT	N+ LOADS	N– LOADS
FLIP-FLOPS, GATES, AND ONE-SHOT	Each Output	10	10
INVERTER (SN7350)	Each Output	10	10
	4 Inverters in parallel	40	40

pin identification

Pin identification for Series 73 networks is shown in the illustration at the right. Symbolization on package denotes orientation. For dimensions see mechanical data.



TO-89 TO-84

logic

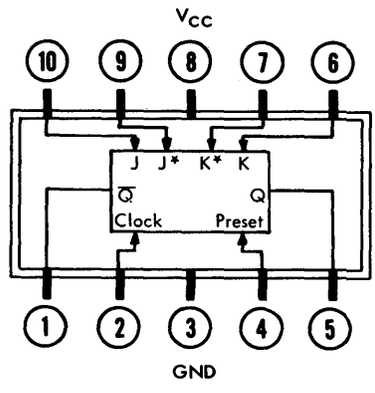
TRUTH TABLES

J★ = K★ = 1		
t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

J = K = 0		
t_n		t_{n+1}
J★	K★	Q
0	0	$\overline{Q}$n
0	1	1
1	0	0
1	1	Qn

ADDITIONAL INPUT LOGIC COMBINATIONS				
t_n				t_{n+1}
J	K	J★	K★	Q
0	1	0	0	$\overline{Q}$n
1	0	0	0	$\overline{Q}$n
1	1	0	0	$\overline{Q}$n
0	1	0	1	$\overline{Q}$n
1	1	0	1	$\overline{Q}$n
1	0	1	0	$\overline{Q}$n
1	1	1	0	$\overline{Q}$n
1	0	0	1	1
0	1	1	0	0

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse



positive logic

High input to preset sets Q to logical 1

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N− 10
Fall Time of Clock Pulse, $t_{f(clock)}$ . . . . . 20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(clock)}$ . . . . . 50 nsec

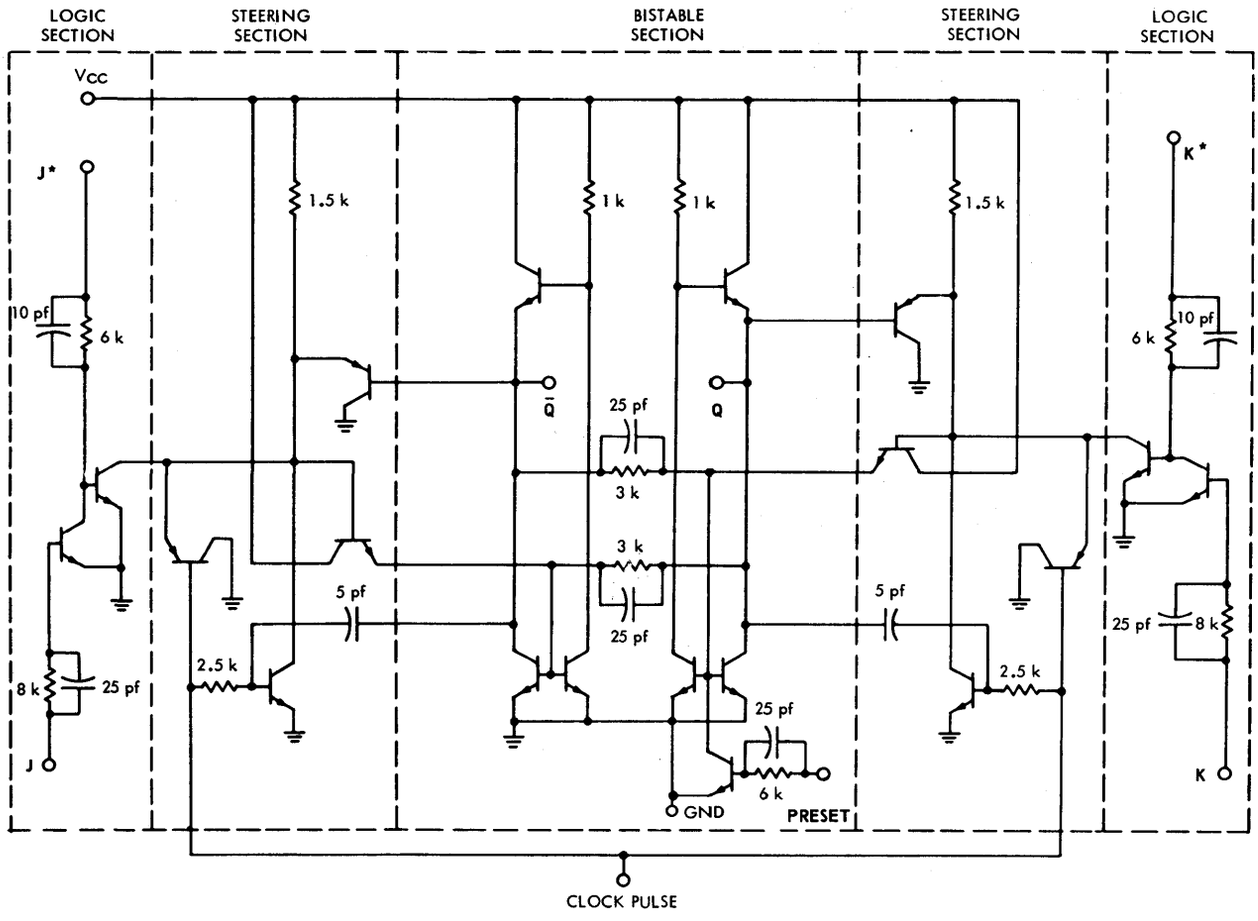
electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, J★, K★, and preset inputs	1	V_{CC} = 3 v	1.7		3	v
			V_{CC} = 4 v	2.4		4	v
$V_{in(1)}$	Input voltage required to ensure logical 1 at clock input	2	V_{CC} = 3 v	1.5		3	v
			V_{CC} = 4 v	2.2		4	v
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, J★, K★, preset, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 v, N+ = 10 (I_{load} = −5 ma)	1.7			v
			V_{CC} = 4 v, N+ = 10 (I_{load} = −8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	3	V_{CC} = 3 v, N− = 10 (I_{sink} = 2 ma)			0.3	v
			V_{CC} = 4 v, N− = 10 (I_{sink} = 2 ma)			0.3	v
I_{in}	J, K, J★, K★, and preset input current	3	V_{in} = 1.7 v			0.5	ma
			V_{in} = 2.6 v			0.8	ma
I_{in}	Clock input current	3	V_{in} = 1.7 v			1.25	ma
			V_{in} = 2.4 v			2	ma
			V_{in} = 0.3 v			−0.5	ma
$I_{CC(av)}$	Average supply current	4	V_{CC} = 3 v, N+ = N− = 0, Toggle = 1 Mc, T_A = 25°C		9		ma
			V_{CC} = 4 v, N+ = N− = 0, Toggle = 1 Mc, T_A = 25°C		13		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, $N+ = N- = 0$

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	19	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J, J★, K and K★ Input:* $V_{in}=V_{CC}$ *Preset Input:* $V_{in}=0$	20	30	nsec
t_r	Rise Time			20	45	nsec
t_s	Storage Time			40	60	nsec
t_f	Fall Time			25	40	nsec
$t_{set(1)}$	Time to Set a Logical 1: J or K	20	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J, J★, K or K★ Input:* $V_{in(1)}=2.5$ v, $V_{in(0)}=0$, $t_r=t_f=50$ nsec	50		nsec
	J★ or K★			35		nsec
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		nsec
	J★ or K★			40		nsec
t_{preset}	Preset Time	21	*Clock Input:* $V_{in}=0$ *Preset Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	55		nsec

schematic



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

logic

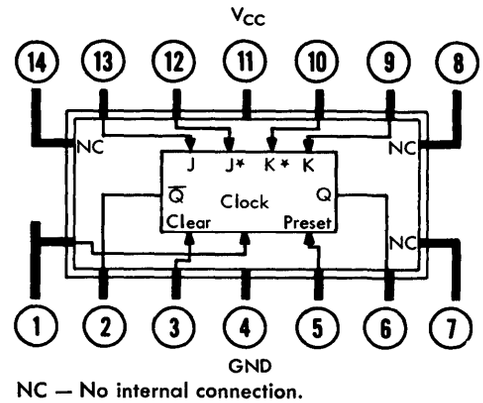
TRUTH TABLES

J★=K★=1		
t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

J=K=0		
t_n		t_{n+1}
J★	K★	Q
0	0	$\overline{Q}$n
0	1	1
1	0	0
1	1	Qn

ADDITIONAL INPUT LOGIC COMBINATIONS				
t_n				t_{n+1}
J	K	J★	K★	Q
0	1	0	0	$\overline{Q}$n
1	0	0	0	$\overline{Q}$n
1	1	0	0	$\overline{Q}$n
0	1	0	1	$\overline{Q}$n
1	1	0	1	$\overline{Q}$n
1	0	1	0	$\overline{Q}$n
1	1	1	0	$\overline{Q}$n
1	0	0	1	1
0	1	1	0	0

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse



NC — No internal connection.

positive logic

High input to preset sets Q to logical 1
High input to clear sets Q to logical 0

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10
Fall Time of Clock Pulse, $t_{f(clock)}$ . . . . . 20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(clock)}$ . . . . . 50 nsec

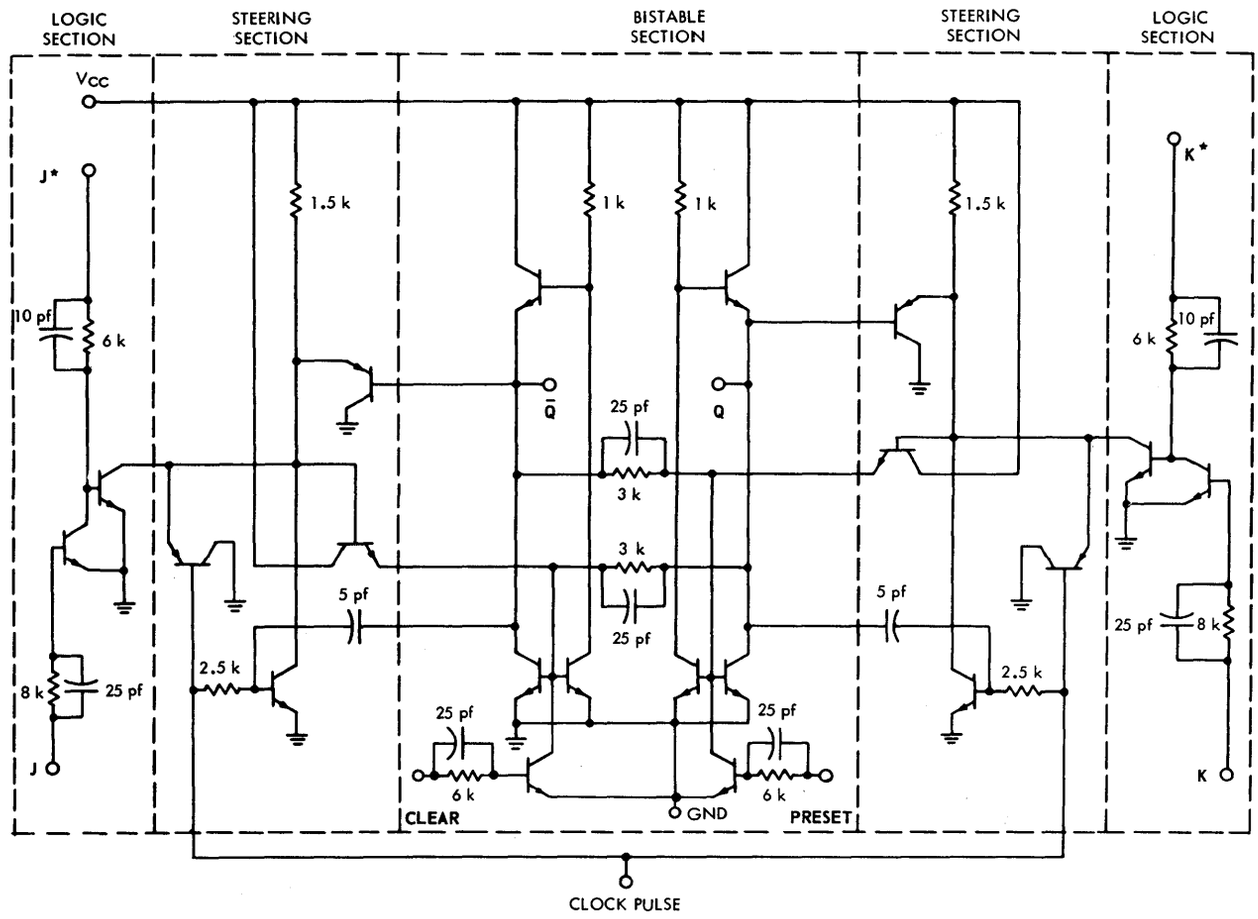
electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, J★, K★, preset, and clear inputs	1	V_{CC}=3 v	1.7		3	v
			V_{CC}=4 v	2.4		4	v
$V_{in(1)}$	Input voltage required to ensure logical 1 at clock input	2	V_{CC}=3 v	1.5		3	v
			V_{CC}=4 v	2.2		4	v
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, J★, K★, preset, clock, and clear inputs	1, 2		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC}=3 v, N+=10 (I_{load}=–5 ma)	1.7			v
			V_{CC}=4 v, N+=10 (I_{load}=–8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	3	V_{CC}=3 v, N–=10 (I_{sink}=2 ma)			0.3	v
			V_{CC}=4 v, N–=10 (I_{sink}=2 ma)			0.3	v
I_{in}	J, K, J★, K★, preset, and clear input current	3	V_{in}=1.7 v			0.5	ma
			V_{in}=2.6 v			0.8	ma
I_{in}	Clock input current	3	V_{in}=1.7 v			1.25	ma
			V_{in}=2.4 v			2	ma
			V_{in}=0.3 v			–0.5	ma
$I_{CC(av)}$	Average supply current	4	V_{CC}=3 v, N+=N–=0, Toggle=1 Mc, T_A=25°C		9		ma
			V_{CC}=4 v, N+=N–=0, Toggle=1 Mc, T_A=25°C		13		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, $N+ = N- = 0$

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	19	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J, J★, K and K★ Input:* $V_{in}=V_{CC}$ *Preset Input:* $V_{in}=0$ *Clear Input:* $V_{in}=0$	20	30	nsec
t_r	Rise Time			20	45	nsec
t_s	Storage Time			40	60	nsec
t_f	Fall Time			25	40	nsec
$t_{set(1)}$	Time to Set a Logical 1: J or K	20	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J, J★, K or K★ Input:* $V_{in(1)}=2.5$ v, $V_{in(0)}=0$, $t_r=t_f=50$ nsec	50		nsec
	J★ or K★			35		nsec
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		nsec
	J★ or K★			40		nsec
t_{preset}	Preset Time	21	*Clock Input:* $V_{in}=0$ *Preset Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	55		nsec
t_{clear}	Clear Time	21	*Clock Input:* $V_{in}=0$ *Clear Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	75		nsec

schematic



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

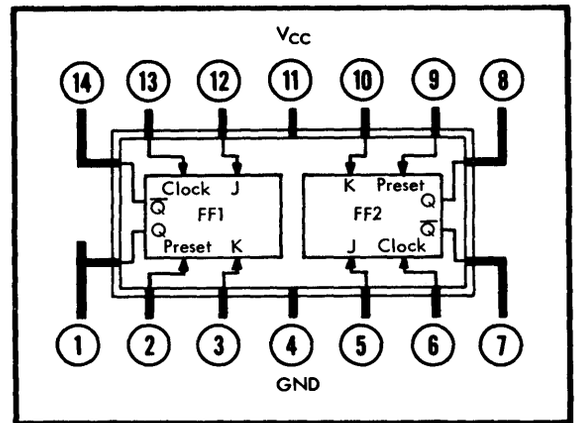
logic

TRUTH TABLE
EACH FLIP-FLOP

t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse



positive logic

High input to preset sets Q to logical 1

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10
Fall Time of Clock Pulse, $t_{f(clock)}$ . . . . . 20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(clock)}$ . . . . . 50 nsec

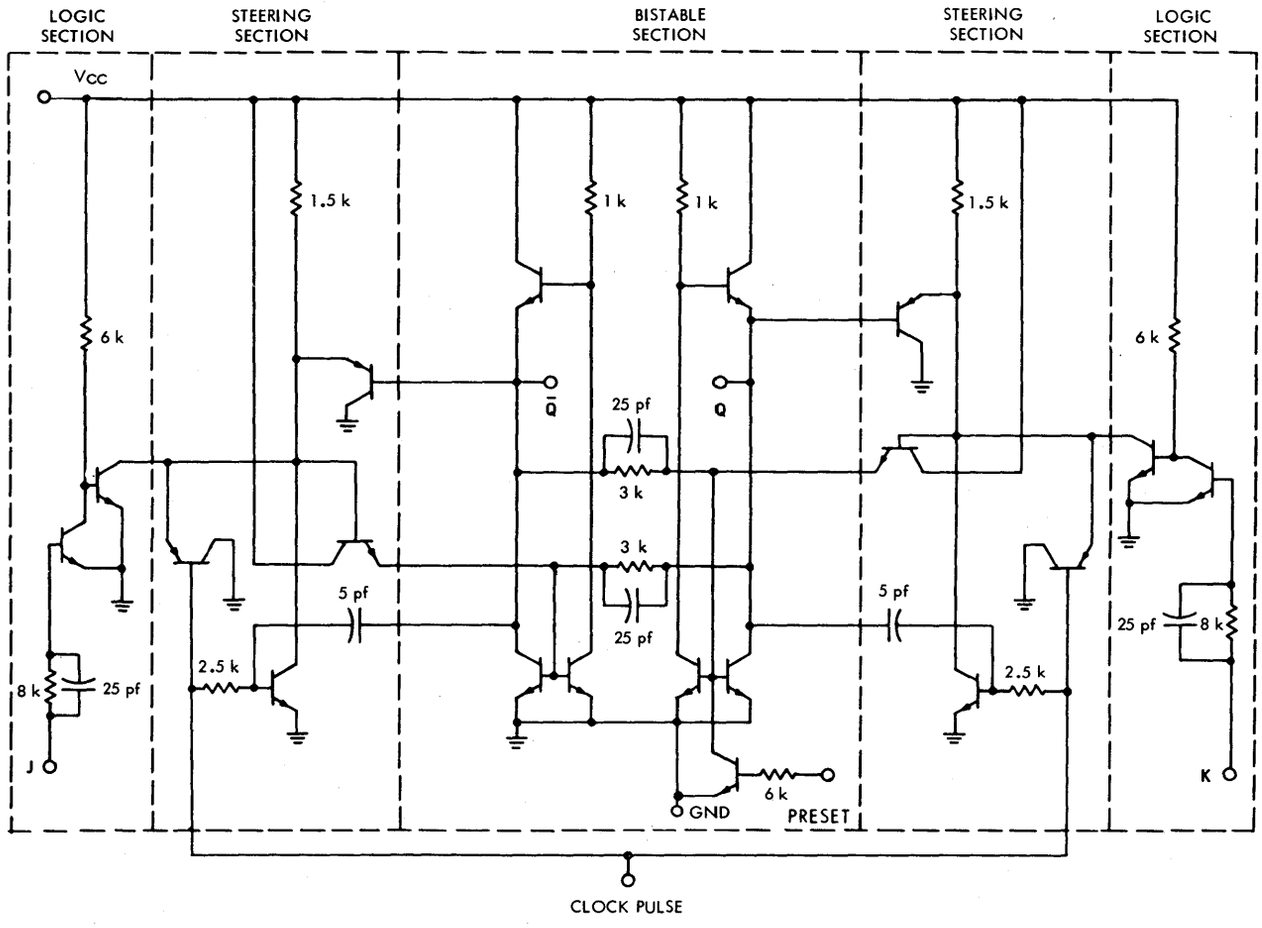
electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, and preset inputs	1	V_{CC} = 3 v	1.7		3	v
			V_{CC} = 4 v	2.4		4	v
$V_{in(1)}$	Input voltage required to ensure logical 1 at clock input	2	V_{CC} = 3 v	1.5		3	v
			V_{CC} = 4 v	2.2		4	v
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, preset, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 v, N+ = 10 (I_{load} = –5 ma)	1.7			v
			V_{CC} = 4 v, N+ = 10 (I_{load} = –8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	3	V_{CC} = 3 v, N– = 10 (I_{sink} = 2 ma)			0.3	v
			V_{CC} = 4 v, N– = 10 (I_{sink} = 2 ma)			0.3	v
I_{in}	J, K, and preset input current	3	V_{in} = 1.7 v			0.5	ma
			V_{in} = 2.6 v			0.8	ma
I_{in}	Clock input current	3	V_{in} = 1.7 v			1.25	ma
			V_{in} = 2.4 v			2	ma
			V_{in} = 0.3 v			–0.5	ma
$I_{CC(av)}$	Average supply current (each flip-flop)	4	V_{CC} = 3 v, N+ = N– = 0, Toggle = 1 Mc, T_A = 25°C		9		ma
			V_{CC} = 4 v, N+ = N– = 0, Toggle = 1 Mc, T_A = 25°C		13		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N+ = N– = 0

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	19	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f = 1 Mc *J and K Input:* $V_{in}=V_{CC}$ *Preset Input:* $V_{in}=0$	20	30	nsec
t_r	Rise Time			20	45	nsec
t_s	Storage Time			40	60	nsec
t_f	Fall Time			25	40	nsec
$t_{set(1)}$	Time to Set a Logical 1: J or K	20	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f = 1 Mc	50		nsec
$t_{set(0)}$	Time to Set a Logical 0: J or K		*J or K Input:* $V_{in(1)}=2.5$ v, $V_{in(0)}=0$, $t_r=t_f=50$ nsec	40		nsec
t_{preset}	Preset Time	21	*Clock Input:* $V_{in}=0$ *Preset Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	75		nsec

schematic (each flip-flop)



NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

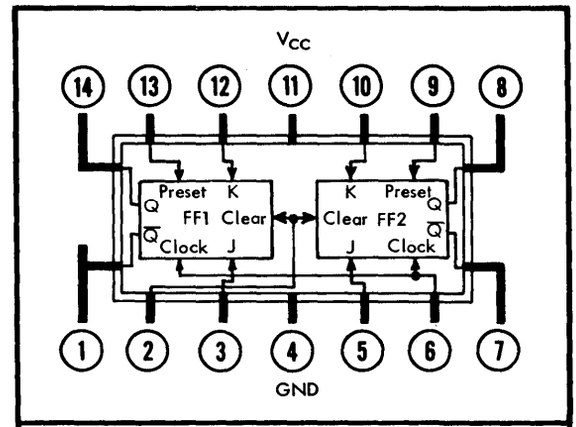
logic

TRUTH TABLE
EACH FLIP-FLOP

t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}n$

t_n = Bit time before clock pulse

t_{n+1} = Bit time after clock pulse



positive logic
High input to preset sets Q to logical 1
High input to clear sets Q1 and Q2 to logical 0

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10
Fall Time of Clock Pulse, $t_{f(clock)}$ . . . . . 20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(clock)}$ . . . . . 50 nsec

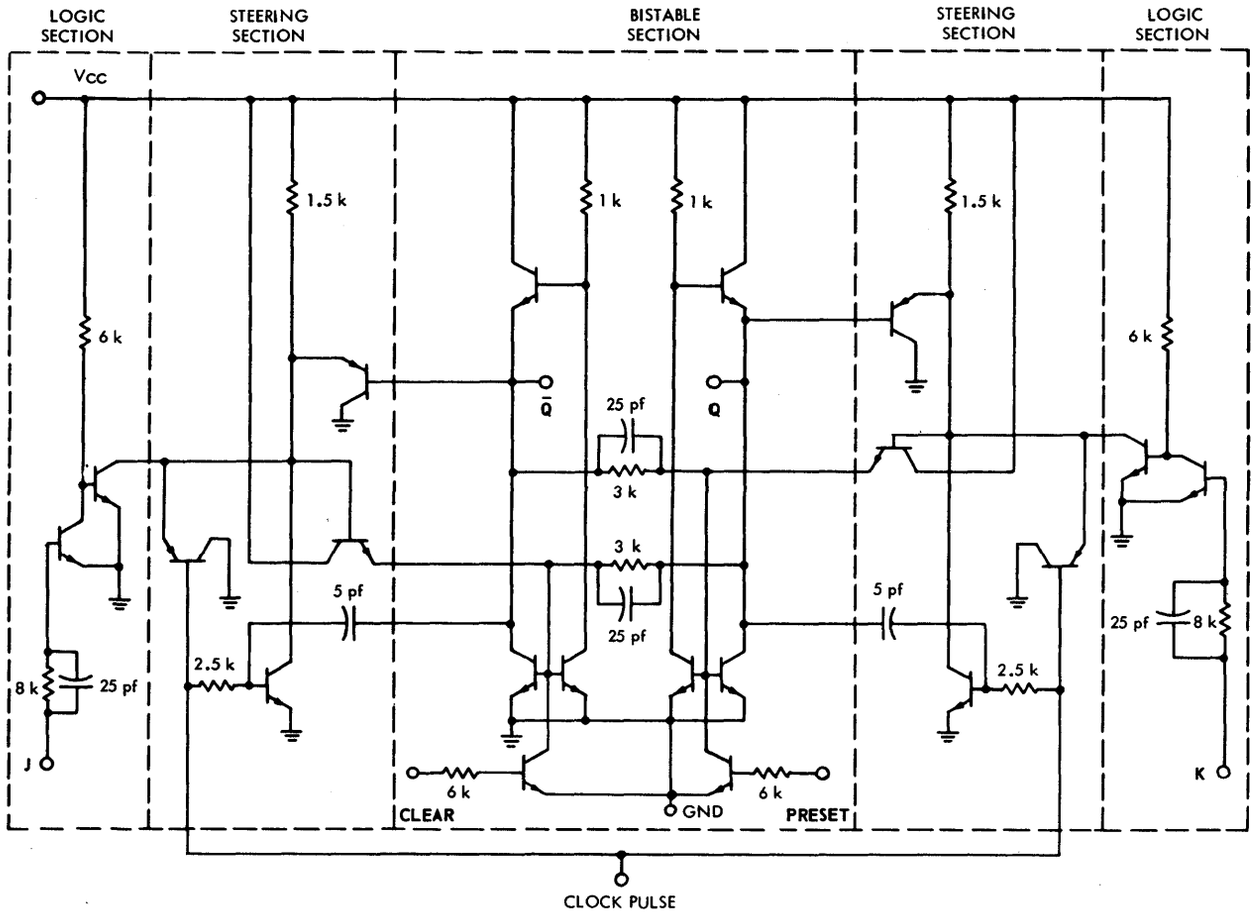
electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at J, K, preset, and clear inputs	1	V_{CC} = 3 v	1.7		3	v
			V_{CC} = 4 v	2.4		4	v
$V_{in(1)}$	Input voltage required to ensure logical 1 at clock input	2	V_{CC} = 3 v	1.5		3	v
			V_{CC} = 4 v	2.2		4	v
$V_{in(0)}$	Input voltage required to ensure logical 0 at J, K, preset, clear, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	3	V_{CC} = 3 v, N+ = 10 (I_{load} = –5 ma)	1.7			v
			V_{CC} = 4 v, N+ = 10 (I_{load} = –8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	3	V_{CC} = 3 v, N– = 10 (I_{sink} = 2 ma)			0.3	v
			V_{CC} = 4 v, N– = 10 (I_{sink} = 2 ma)			0.3	v
I_{in}	J, K, and preset input current	3	V_{in} = 1.7 v			0.5	ma
			V_{in} = 2.6 v			0.8	ma
I_{in}	Clock input current	3	V_{in} = 1.7 v			2.5	ma
			V_{in} = 2.4 v			4	ma
			V_{in} = 0.3 v			–1	ma
I_{in}	Clear input current	3	V_{in} = 1.7 v			1	ma
			V_{in} = 2.6 v			1.6	ma
$I_{CC(av)}$	Average supply current (each flip-flop)	4	V_{CC} = 3 v, N+ = N– = 0, Toggle = 1 Mc, T_A = 25°C		9		ma
			V_{CC} = 4 v, N+ = N– = 0, Toggle = 1 Mc, T_A = 25°C		13		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N+ = N– = 0

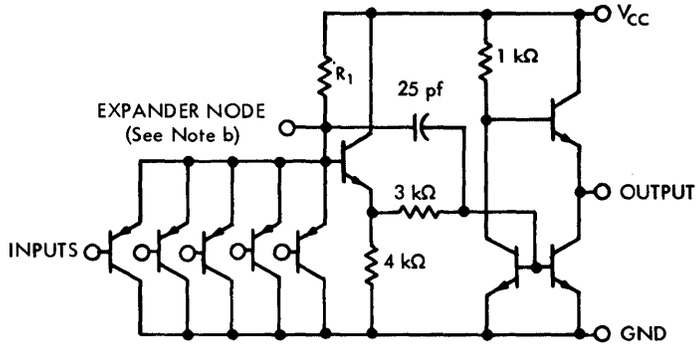
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	19	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J and K Input:* $V_{in}=V_{CC}$ *Preset Input:* $V_{in}=0$ *Clear Input:* $V_{in}=0$	20	30	nsec
t_r	Rise Time			20	45	nsec
t_s	Storage Time			40	60	nsec
t_f	Fall Time			25	40	nsec
$t_{set(1)}$	Time to Set a Logical 1: J or K	20	*Clock Input:* $V_{in}=2.5$ v, $t_f=20$ nsec, $t_p=500$ nsec, f=1 Mc *J or K Input:* $V_{in(1)}=2.5$ v, $V_{in(0)}=0$, $t_r=t_f=50$ nsec	50		nsec
$t_{set(0)}$	Time to Set a Logical 0: J or K			40		nsec
t_{preset}	Preset Time	21	*Clock Input:* $V_{in}=0$ *Preset Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	75		nsec
t_{clear}	Clear Time	21	*Clock Input:* $V_{in}=0$ *Clear Input:* $V_{in}=2.5$ v, $t_f=50$ nsec	100		nsec

schematic (each flip-flop)



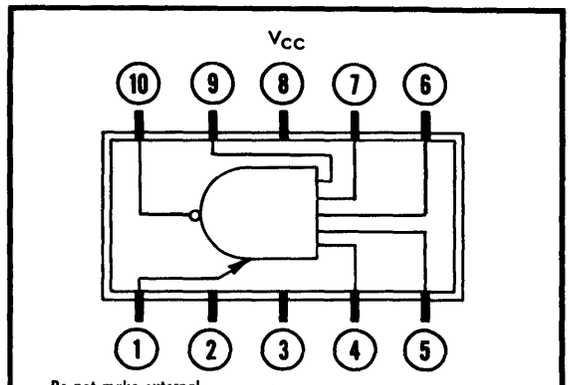
NOTES: a. Component values shown are nominal.
b. Resistor values are in ohms.

schematic



NOTES: a. Component values shown are nominal

b. Four SN7320 expanders may be fanned into one SN7310 to provide a total fan-in of 25. If expander is not used leave pin ① open.



positive logic

$10 = \overline{4 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 1}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out Into Positive Loads, N+ 10
Maximum Fan-out Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output.	5	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(1)X}$	Input voltage required at expander node (pin ①) to ensure logical 0 (on level) at output	8	$V_{CC}=3$ v	2.1		3	v
			$V_{CC}=4$ v	2.9		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{in(0)X}$	Input voltage required at expander node (pin ①) to ensure logical 1 (off level) at output	7	$T_A=0°C$	0		1.2	v
			$T_A=70°C$	0		1	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v

Characteristics continued next page.

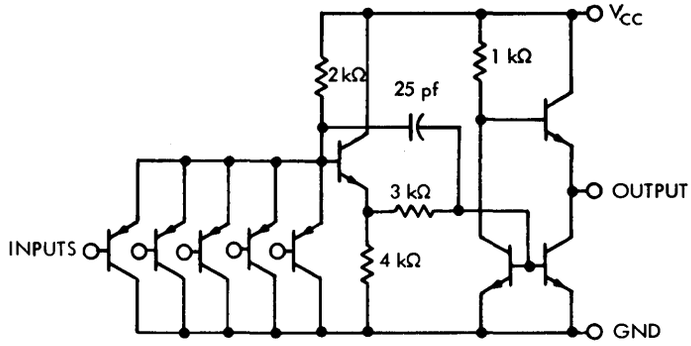
electrical characteristics continued

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{in}	Input current (each input)	6	$V_{in}=0.3$ v, N+ = N− = 0			−0.2	ma
$I_{CC(on)}$	On level supply current	9	$V_{CC}=V_{in}=3$ v, N+ = N− = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N− = 0, $T_A=25°C$		4.5		ma
$I_{CC(off)}$	Off level supply current	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N− = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N− = 0, $T_A=25°C$		1.6		ma
$R_{1(eff)}$	R_1 Effective resistance	10	$T_A=0°C$	1.35		2.6	k Ω
			$T_A=70°C$	1.5		2.8	k Ω

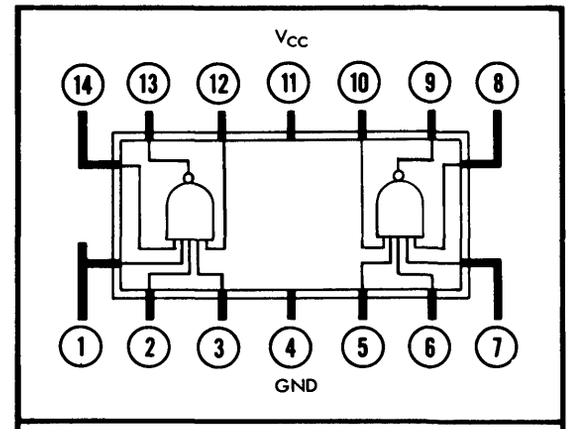
switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N− = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input* : $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	35	45	nsec
t_r	Rise Time			40	50	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			30	40	nsec
t_{pd}	Propagation Delay Time	23		30		nsec

schematic (each gate)



Component values shown are nominal



positive logic

$9 = \overline{5 \cdot 6 \cdot 7 \cdot 8 \cdot 10}$ $13 = \overline{1 \cdot 2 \cdot 3 \cdot 12 \cdot 14}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

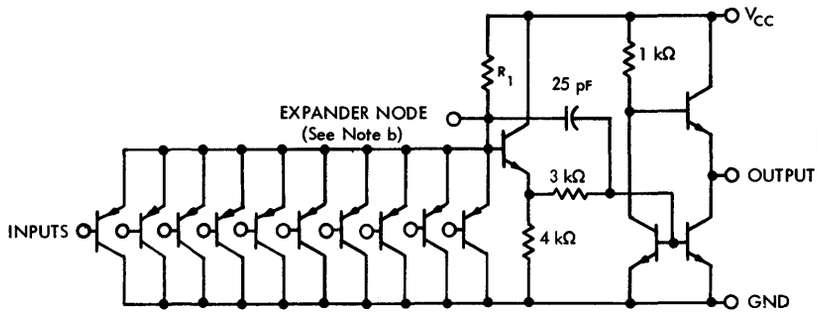
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
I_{in}	Input current (each input)	6	$V_{in}=0.3$ v, N+ = N– = 0			–0.2	ma
$I_{CC(on)}$	On level supply current (each gate)	9	$V_{CC}=V_{in}=3$ v, N+ = N– = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N– = 0, $T_A=25°C$		4.5		ma
$I_{CC(off)}$	Off level supply current (each gate)	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.6		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N– = 1

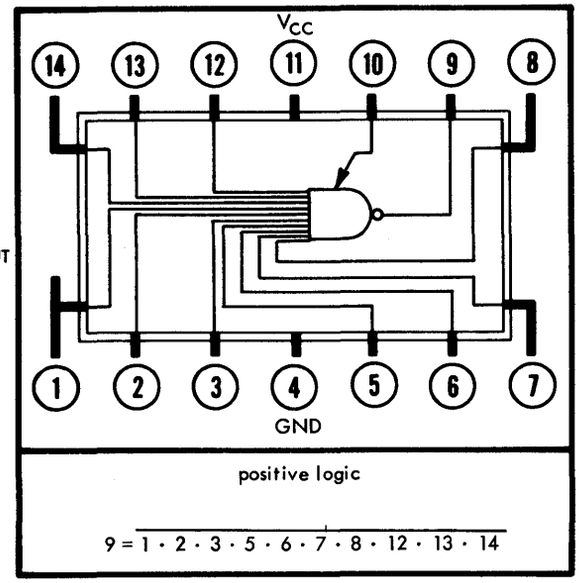
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	20	30	nsec
t_r	Rise Time			25	45	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			25	40	nsec
t_{pd}	Propagation Delay Time	23		25		nsec

TYPE SN7315
10-INPUT EXPANDABLE NAND/NOR GATE

schematic



NOTES: a. Component values shown are nominal.
b. Three SN7320 expanders may be fanned into one SN7315 to provide a total fan-in of 25. If expander is not used leave pin (10) open.



recommended operating conditions

Supply Voltage, V_{CC}	3 v to 4 v
Maximum Fan-out Into Positive Loads, N+	10
Maximum Fan-out Into Negative Loads, N–	10

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output.	5	V_{CC}=3 v	1.7		3	v
			V_{CC}=4 v	2.4		4	v
$V_{in(1)X}$	Input voltage required at expander node (pin (10)) to ensure logical 0 (on level) at output	8	V_{CC}=3 v	2.1		3	v
			V_{CC}=4 v	2.9		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{in(0)X}$	Input voltage required at expander node (pin (10)) to ensure logical 1 (off level) at output	7	T_A=0°C	0		1.2	v
			T_A=70°C	0		1	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	V_{CC}=3 v, V_{in}=0.4 v, N+=10 (I_{load}=–5 ma)	1.7			v
			V_{CC}=4 v, V_{in}=0.4 v, N+=10 (I_{load}=–8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	V_{CC}=3 v, V_{in}=1.7 v, N–=10 (I_{sink}=2 ma)			0.3	v
			V_{CC}=4 v, V_{in}=2.4 v, N–=10 (I_{sink}=2 ma)			0.3	v
I_{in}	Input current (each input)	6	V_{in}=0.3 v, N+=N–=0			–0.2	ma
$I_{CC(on)}$	On level supply current	9	V_{CC}=V_{in}=3 v, N+=N–=0, T_A=25°C		3.3		ma
			V_{CC}=V_{in}=4 v, N+=N–=0, T_A=25°C		4.5		ma

Characteristics continued next page.

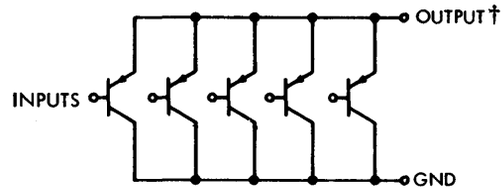
electrical characteristics continued

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(off)}$	Off level supply current	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N− = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N− = 0, $T_A=25°C$		1.6		ma
$R_{1(eff)}$	R_1 Effective resistance	10	$T_A=0°C$	1.35		2.6	kΩ
			$T_A=70°C$	1.5		2.8	kΩ

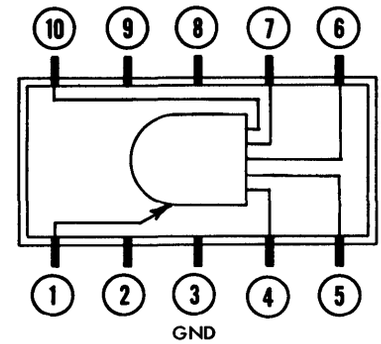
switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N− = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	35	45	nsec
t_r	Rise Time			40	50	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			30	40	nsec
t_{pd}	Propagation Delay Time	23		30		nsec

schematic



† Connect output to expander node of SN7310 (pin ①) or SN7315 (pin ⑩).



Do not make external connection at pins ②, ⑧, or ⑨.

positive logic

1 = 4 • 5 • 6 • 7 • 10

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

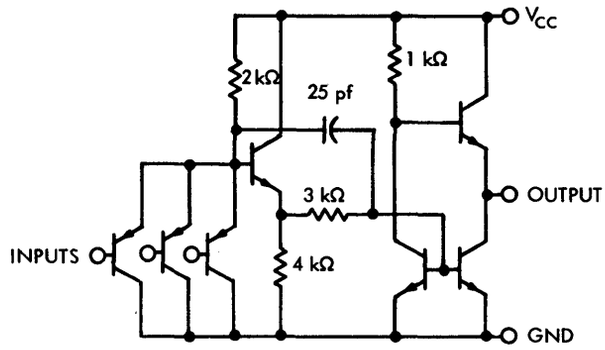
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
I_{in}	Input Current (each input)	11	$V_{in}=0.3$ v		−0.2	ma
$V_{out(0)X}$	Expander node output voltage (off level) with logical 0 at any input	11	$V_{CC}=4$ v, $V_{in}=0.3$ v, $T_A=0°C$		1.2	v
			$V_{CC}=4$ v, $V_{in}=0.3$ v, $T_A=70°C$		1	v
$V_{out(1)X}$	Expander node output voltage (on level) with logical 1 at all inputs	12	$V_{CC}=3$ v, $V_{in}=1.7$ v	2.1		v
			$V_{CC}=4$ v, $V_{in}=2.6$ v	2.9		v

NOTES: The SN7320 $V_{in(1)}$ and $V_{in(0)}$ limits are the same as defined for the SN7310 and the SN7315.

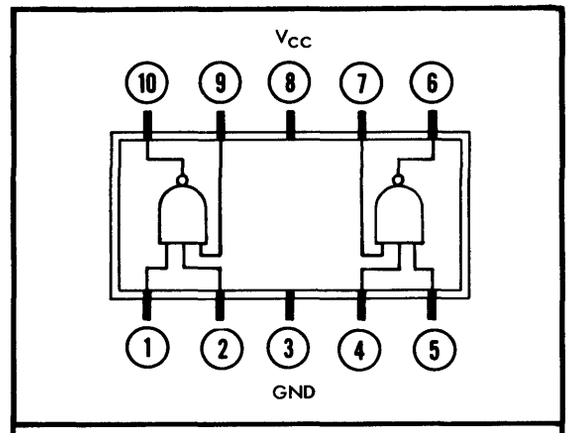
Four SN7320 expanders may be fanned into one SN7310 to provide a total fan-in of 25. Three SN7320 expanders may be fanned into one SN7315 to provide a total fan-in of 25.

TYPE SN7330
DUAL 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



positive logic

$6 = \overline{4 \cdot 5 \cdot 7}$ $\quad 10 = \overline{1 \cdot 2 \cdot 9}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

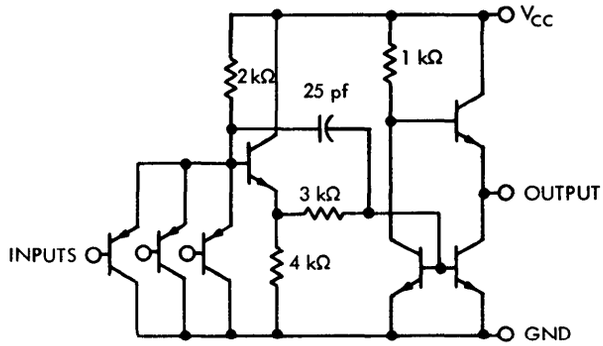
electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
I_{in}	Input current (each input)	6	$V_{in}=0.3$ v, N+ = N– = 0			–0.2	ma
$I_{CC(on)}$	On level supply current (each gate)	9	$V_{CC}=V_{in}=3$ v, N+ = N– = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N– = 0, $T_A=25°C$		4.5		ma
$I_{CC(off)}$	Off level supply current (each gate)	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.6		ma

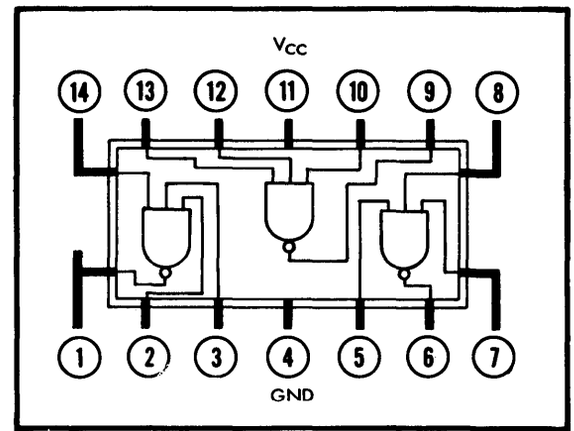
switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	20	30	nsec
t_r	Rise Time			25	45	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			25	40	nsec
t_{pd}	Propagation Delay Time	23		25		nsec

schematic (each gate)



Component values shown are nominal.



positive logic

$1 = \overline{2 \cdot 3 \cdot 14}$ $6 = \overline{5 \cdot 7 \cdot 8}$ $9 = \overline{10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

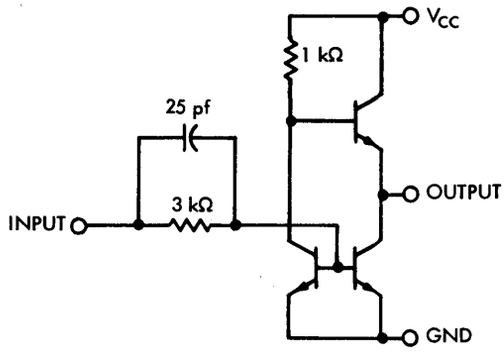
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
I_{in}	Input current (each input)	6	$V_{in}=0.3$ v, N+ = N– = 0			–0.2	ma
$I_{CC(on)}$	On level supply current (each gate)	9	$V_{CC}=V_{in}=3$ v, N+ = N– = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N– = 0, $T_A=25°C$		4.5		ma
$I_{CC(off)}$	Off level supply current (each gate)	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.6		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N– = 1

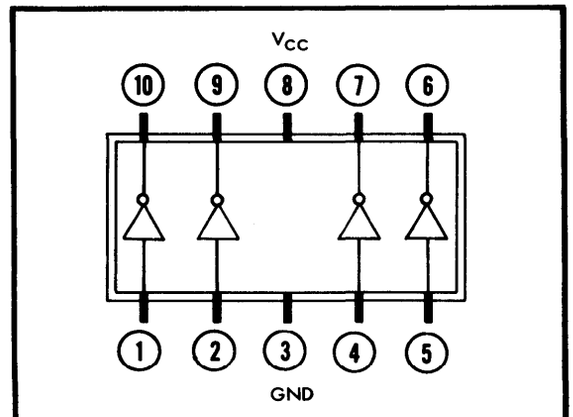
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	20	30	nsec
t_r	Rise Time			25	45	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			25	40	nsec
t_{pd}	Propagation Delay Time	23		25		nsec

TYPE SN7350
QUADRUPLE INVERTER/DRIVER

schematic (each inverter)



Component values shown are nominal



positive logic

$6 = \overline{5}$ $\quad 9 = \overline{2}$

$7 = \overline{4}$ $\quad 10 = \overline{1}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v

Maximum Fan-out From Each Output Into Positive Loads, N+ 10

Maximum Fan-out From Each Output Into Negative Loads, N– 10

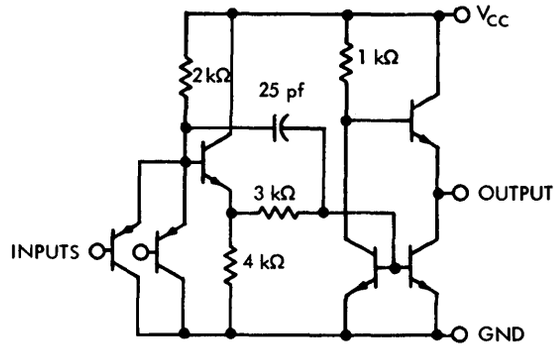
electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required to ensure logical 0 (on level) at output	13	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(0)}$	Logical 0 input voltage required to ensure logical 1 (off level) *at output*	13		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	13	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	13	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
I_{in}	Input current	13	$V_{CC}=3$ v, $V_{in}=1.7$ v, N+ = N– = 0			1	ma
			$V_{CC}=4$ v, $V_{in}=2.6$ v, N+ = N– = 0			1.6	ma
$I_{CC(on)}$	On level supply current (each inverter)	13	$V_{CC}=V_{in}=3$ v, N+ = N– = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N– = 0, $T_A=25°C$		4.5		ma

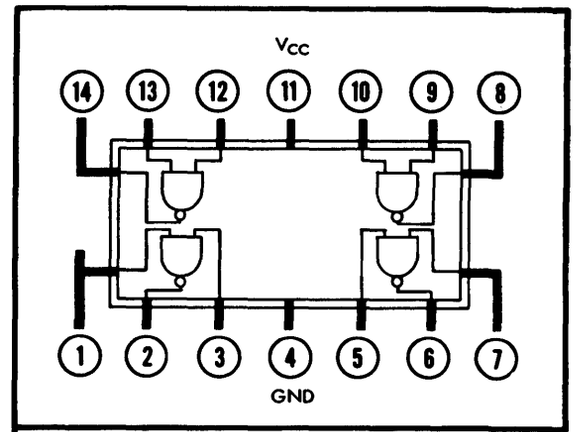
switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	20	30	nsec
t_r	Rise Time			25	45	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			25	40	nsec
t_{pd}	Propagation Delay Time	23		25		nsec

schematic (each gate)



Component values shown are nominal



positive logic

$2 = \overline{1 \cdot 3}$ $6 = \overline{5 \cdot 7}$ $8 = \overline{9 \cdot 10}$ $14 = \overline{12 \cdot 13}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 3$ v to 4 v)

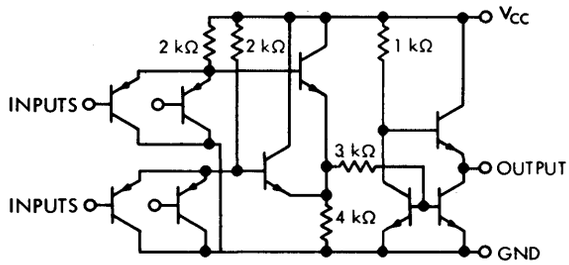
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC}=3$ v	1.7		3	v
			$V_{CC}=4$ v	2.4		4	v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	6	$V_{CC}=3$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-5$ ma)	1.7			v
			$V_{CC}=4$ v, $V_{in}=0.4$ v, N+ = 10 ($I_{load}=-8$ ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	5	$V_{CC}=3$ v, $V_{in}=1.7$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
			$V_{CC}=4$ v, $V_{in}=2.4$ v, N– = 10 ($I_{sink}=2$ ma)			0.3	v
I_{in}	Input current (each input)	6	$V_{in}=0.3$ v, N+ = N– = 0			–0.2	ma
$I_{CC(on)}$	On level supply current (each gate)	9	$V_{CC}=V_{in}=3$ v, N+ = N– = 0, $T_A=25°C$		3.3		ma
			$V_{CC}=V_{in}=4$ v, N+ = N– = 0, $T_A=25°C$		4.5		ma
$I_{CC(off)}$	Off level supply current (each gate)	9	$V_{CC}=3$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.2		ma
			$V_{CC}=4$ v, $V_{in}=0.3$ v, N+ = N– = 0, $T_A=25°C$		1.6		ma

switching characteristics, $T_A = 25°C$, $V_{CC} = 3.5$ v, N– = 1

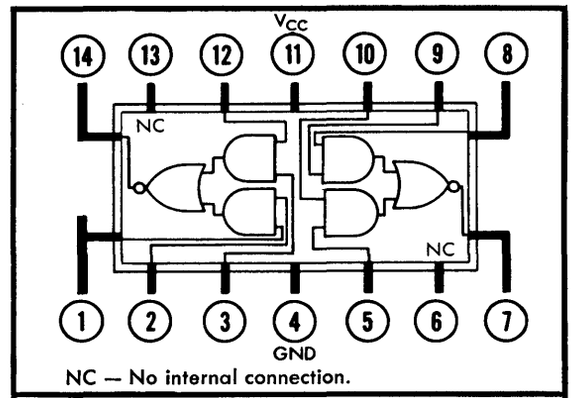
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: $V_{in}=2.5$ v, f = 1 Mc, $t_p=500$ nsec, $t_r=t_f=20$ nsec	20	30	nsec
t_r	Rise Time			25	45	nsec
t_s	Storage Time			25	45	nsec
t_f	Fall Time			25	40	nsec
t_{pd}	Propagation Delay Time	23		25		nsec

TYPE SN7370
DUAL AND-OR-INVERT GATE

schematic (each gate)



Component values shown are nominal



NC — No internal connection.

positive logic

$7 = \overline{(5 \cdot 10)+(8 \cdot 9)}$ $14 = \overline{(1 \cdot 2)+(3 \cdot 12)}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N+ 10
Maximum Fan-out From Each Output Into Negative Loads, N– 10

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(0)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 (on level) at output	14	V_{CC}=3 v	1.7		3	v
			V_{CC}=4 v	2.4		4	v
$V_{in(1)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 (off level) at output	15		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	15	V_{CC}=3 v, V_{in}=0.4 v, N+=10 (I_{load}=–5 ma)	1.7			v
			V_{CC}=4 v, V_{in}=0.4 v, N+=10 (I_{load}=–8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	14	V_{CC}=3 v, V_{in}=1.7 v, N–=10 (I_{sink}=2 ma)			0.3	v
			V_{CC}=4 v, V_{in}=2.4 v, N–=10 (I_{sink}=2 ma)			0.3	v
I_{in}	Input current (each input)	15	V_{in}=0.3 v, N+=N–=0			–0.2	ma
$I_{CC(on)}$	On level supply current (each gate)	14	V_{CC}=V_{in}=3 v, N+=N–=0, T_A=25°C		3.3		ma
			V_{CC}=V_{in}=4 v, N+=N–=0, T_A=25°C		4.5		ma
$I_{CC(off)}$	Off level supply current (each gate)	15	V_{CC}=3 v, V_{in}=0.3 v, N+=N–=0, T_A=25°C		1.2		ma
			V_{CC}=4 v, V_{in}=0.3 v, N+=N–=0, T_A=25°C		1.6		ma

switching characteristics, T_A = 25°C, V_{CC} = 3.5 v, N– = 1

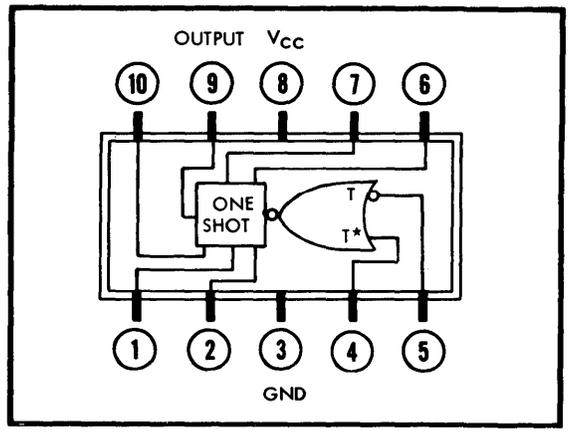
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_d	Delay Time	22	*Input*: V_{in}=2.5 v, f=1 Mc, t_p=500 nsec, t_r=t_f=20 nsec	30	60	nsec
t_r	Rise Time			30	60	nsec
t_s	Storage Time			100	200	nsec
t_f	Fall Time			100	200	nsec
t_{pd}	Propagation Delay Time	23		65		nsec

logic

TRUTH TABLE

positive logic				
T		T★		OUTPUT
t_n	t_{n+1}	t_n	t_{n+1}	
1	1	--	--	INHIBITED (logical 1)
--	--	0	0	INHIBITED (logical 1)
0	0	1	0	ONE-SHOT (logical 0 for t_p nsec)
0	1	1	1	ONE-SHOT (logical 0 for t_p nsec)

t_n = bit time before change in input levels
t_{n+1} = bit time after change in input levels



recommended operating conditions

Supply Voltage, V_{CC} . . . . . 3 v to 4 v
Maximum Fan-out Into Positive Loads, N+ 10
Maximum Fan-out Into Negative Loads, N– 10
Minimum Set-Up Time, $t_{set\text{-}up}$† . . . . . 400 nsec

electrical characteristics (unless otherwise noted T_A = 0°C to 70°C, V_{CC} = 3 v to 4 v)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at T or T★ input	16	V_{CC}=3 v	1.7		3	v
			V_{CC}=4 v	2.4		4	v
$V_{in(0)}$	Input voltage required to ensure logical 0 at T or T★ input	16		0		0.4	v
$V_{out(1)}$	Logical 1 output voltage (off level)	17	V_{CC}=3 v, N+=10 (I_{load}=–5 ma)	1.7			v
			V_{CC}=4 v, N+=10 (I_{load}=–8 ma)	2.6			v
$V_{out(0)}$	Logical 0 output voltage (on level)	17	V_{CC}=3 v, $V_{②}$=0.3 v, pin ⑩ open, N–=10 (I_{sink}=2 ma)			0.3	v
			V_{CC}=4 v, $V_{②}$=0.3 v, pin ⑩ open, N–=10 (I_{sink}=2 ma)			0.3	v
I_{in}	Input current (each input)	16	V_{CC}=3 v, V_{in}=1.7 v, N+=N–=0			0.5	ma
			V_{CC}=4 v, V_{in}=2.6 v, N+=N–=0			0.8	ma
$I_{CC(av)}$	Average supply current	18	V_{CC}=3 v, N+=N–=0, Duty Cycle=50%, T_A=25°C		4.8		ma
			V_{CC}=4 v, N+=N–=0, Duty Cycle=50%, T_A=25°C		6.3		ma

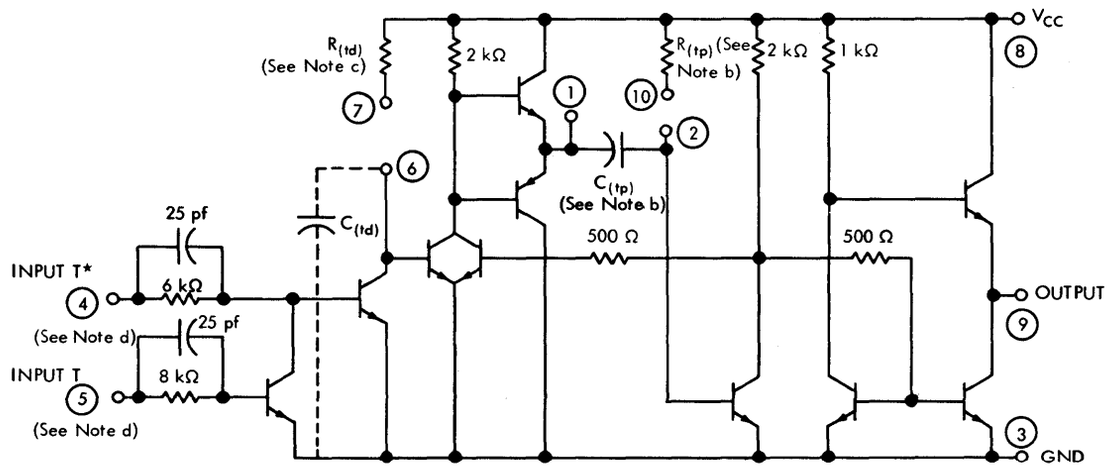
†This is the minimum time necessary for the input signal to dwell before the triggering transition begins and applies when pin ⑥ is shorted to pin ⑦ and pin ② is shorted to pin ⑩. Set-up time begins only after the occurrence of the 10% point of the output fall time.
‡Pin ⑥ shorted to pin ⑦ and pin ② shorted to pin ⑩ unless otherwise noted.

switching times, $T_A = 25°C$, $V_{CC} = 3.5$ v, fan-out N– = 1

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_{d1}	Delay Time after Positive-going Transition at T (pin ⑤)	24	*Input:* $V_{in}=2.5$ v, f = 1 Mc, $t_p=400$ nsec, $t_r=t_f=20$ nsec		90	130	nsec
t_{d2}	Delay Time after Negative-going Transition at T★ (pin ④)				90	130	nsec
t_r	Rise Time				35	60	nsec
t_f	Fall Time				35	60	nsec
t_p	Output Pulse Width	24	*Input:* $V_{in}=2.5$ v, f = 1 Mc, $t_p=400$ nsec, $t_r=t_f=20$ nsec	100	250	400	nsec

‡Pin ⑥ shorted to pin ⑦ and pin ② shorted to pin ⑩ unless otherwise noted.

schematic



NOTES: a. Component values shown are nominal.

b. Output pulse width t_p is proportional to $R_{(tp)}C_{(tp)}$. Output pulse width may be modified using pins ①, ②, ⑧, and ⑩ to change effective values of $R_{(tp)}$ and $C_{(tp)}$. Nominal value of internal $R_{(tp)}$ is 8 k Ω and $C_{(tp)}$ is 25 pf. Value of modified $R_{(tp)}$ should be maintained between 6 k Ω and 15 k Ω.

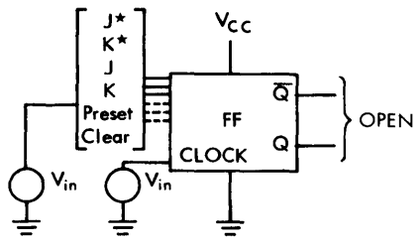
CAUTION:
When the effective valve of $C_{(tp)} \geq 0.1\ \mu f$, a 560-Ω resistor must be connected in series with the external portion of $C_{(tp)}$ (between pins ① and ②).

c. Delay time (t_d) may be modified using pins ③, ⑥, ⑦, and ⑧ to change effective values of $R_{(td)}$ and $C_{(td)}$. Nominal value of internal $R_{(td)}$ is 2 k Ω. Value of modified $R_{(td)}$ should be maintained between 2 k Ω and 10 k Ω.

d. T triggers on a positive transition to logical 1 level, and T★ triggers on a negative transition to logical 0 level. When triggering with T input, hold T★ at logical 1. When triggering with T★ input, hold T at logical 0.

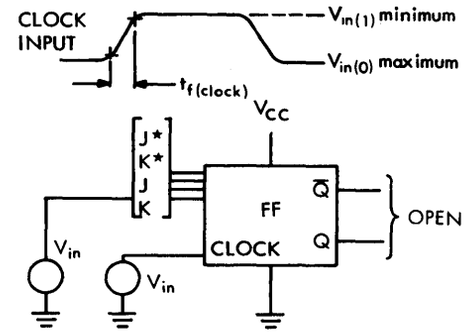
PARAMETER MEASUREMENT INFORMATION§

d-c test circuits



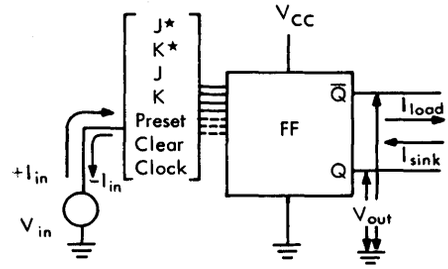
1. Each input is tested separately with unused inputs at worst-case levels.
2. The flip-flop is tested for performance in accordance with truth table.
3. Preset and clear tested with $V_{in(clock)} = 0$.

FIGURE 1



1. The flip-flop is tested for ripple action with the following conditions:
   Clock input: $V_{in(1)}$ minimum, $V_{in(0)}$ maximum, $t_f = 150$ nsec (maximum).
   All other inputs: $V_{in(1)}$ minimum.

FIGURE 2



1. Each input is tested individually for input current.
2. Each output is tested individually for $V_{out(1)}$ and $V_{out(0)}$.

FIGURE 3

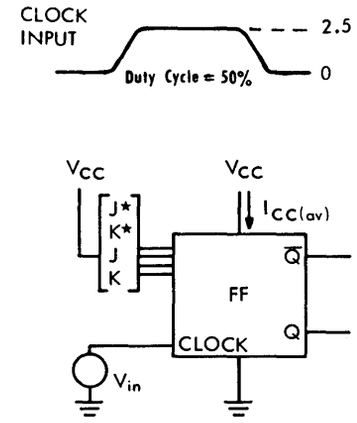
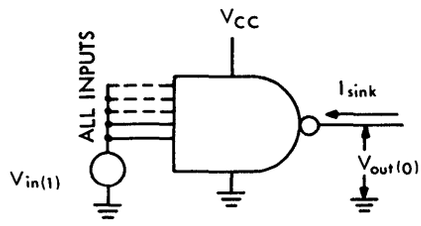
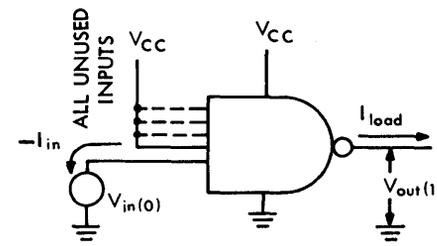


FIGURE 4



1. All inputs tested simultaneously.

FIGURE 5



1. Each input is tested separately.

FIGURE 6

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION§

d-c test circuits (continued)

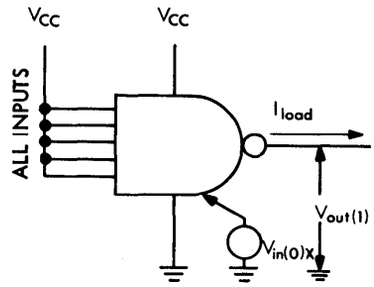


FIGURE 7

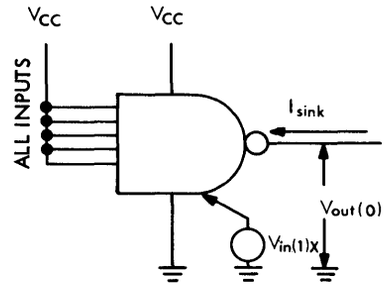
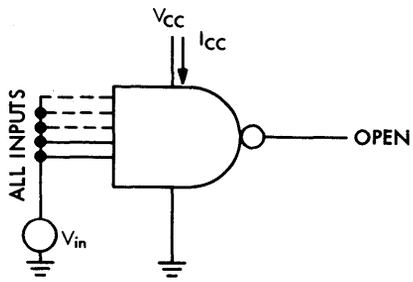
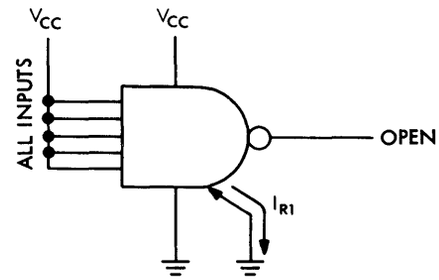


FIGURE 8



1. Test on-level and off-level current.

FIGURE 9



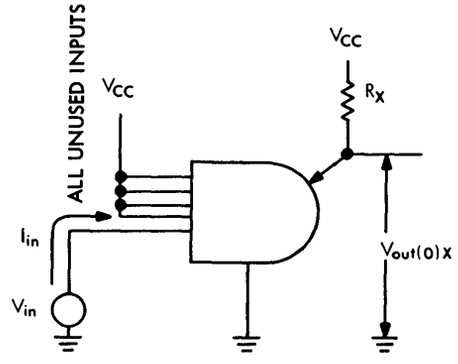
1. $R_{1(eff)} = \frac{V_{CC}}{I_{R1}}$

FIGURE 10

§ Arrows indicate actual direction of current flow.

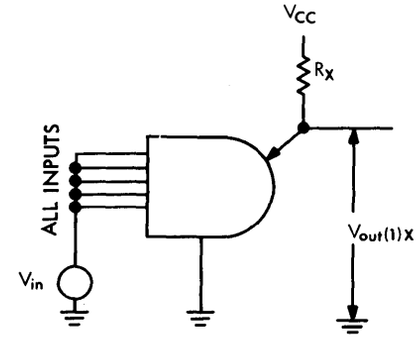
PARAMETER MEASUREMENT INFORMATION§

d-c test circuits (continued)



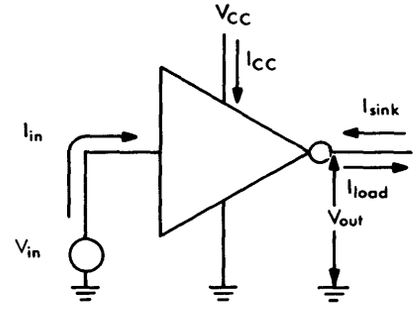
1. $R_X = 1.35\ k\Omega$ at 0°C.
2. $R_X = 1.5\ k\Omega$ at 70°C.
3. Each input is tested separately.
4. R_X is worst case equivalent of R_1 in the SN7310 or the SN7315.

FIGURE 11



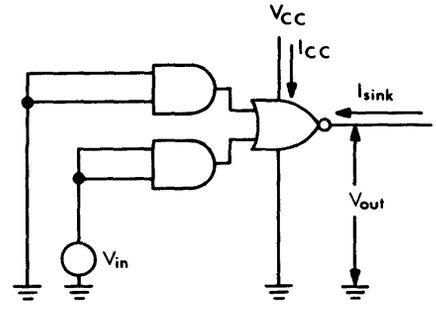
1. $R_X = 2.6\ k\Omega$ at 0°C.
2. $R_X = 2.8\ k\Omega$ at 70°C.
3. All inputs tested simultaneously.
4. R_X is the worst case equivalent of R_1 in the SN7310 or the SN7315.

FIGURE 12



1. Each inverter is tested separately.

FIGURE 13



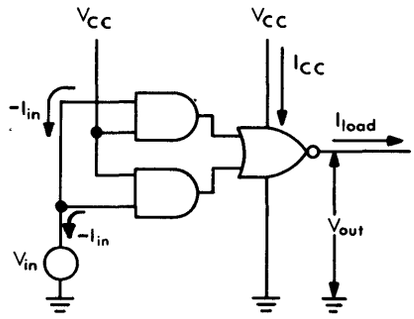
1. Each AND section is tested separately.

FIGURE 14

§ Arrows indicate actual direction of current flow.

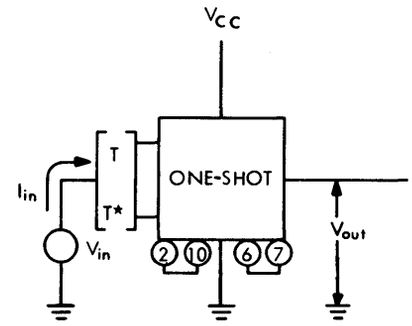
PARAMETER MEASUREMENT INFORMATION§

d-c test circuits (continued)



1. Each input pair is tested separately for $V_{out(1)}$.
2. Each input tested separately for I_{in}.

FIGURE 15



1. Each input is tested separately.
2. With the unused input at the worst-case level and using minimum $V_{in(1)}$ and maximum $V_{in(0)}$ input voltage levels, the one-shot output is verified.

FIGURE 16

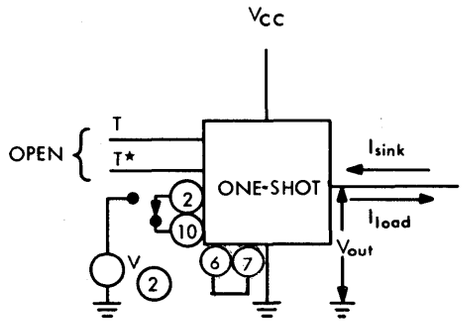
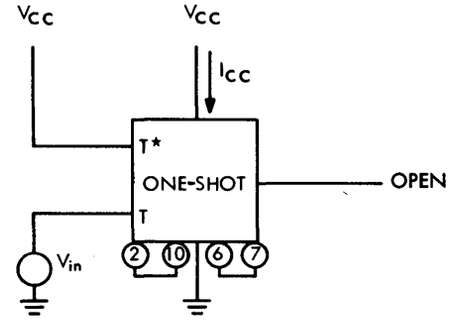


FIGURE 17



1. I_{CC} is measured with a 50% duty cycle.

FIGURE 18

§ Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics

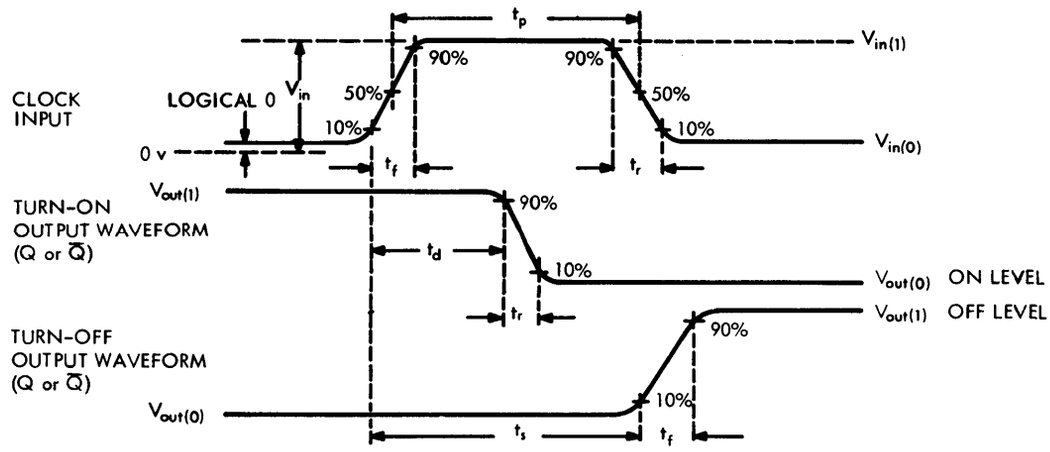


FIGURE 19. CLOCK PULSE AND OUTPUT VOLTAGE WAVEFORMS

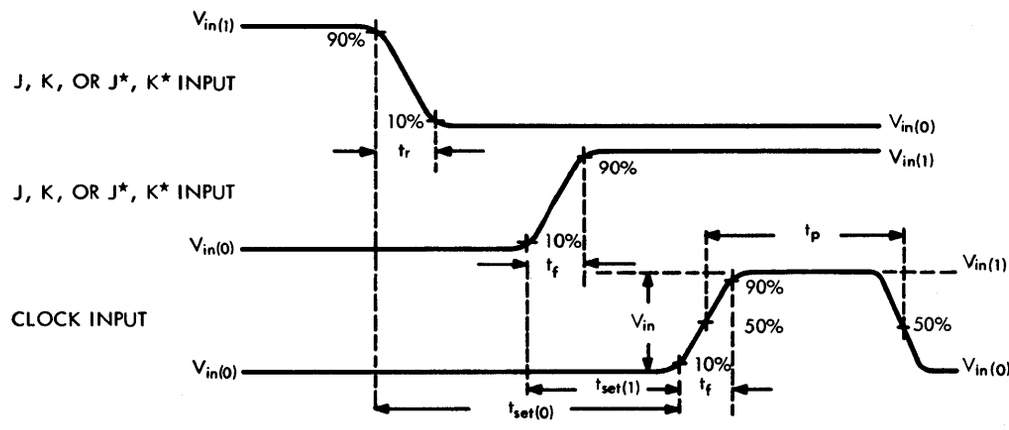
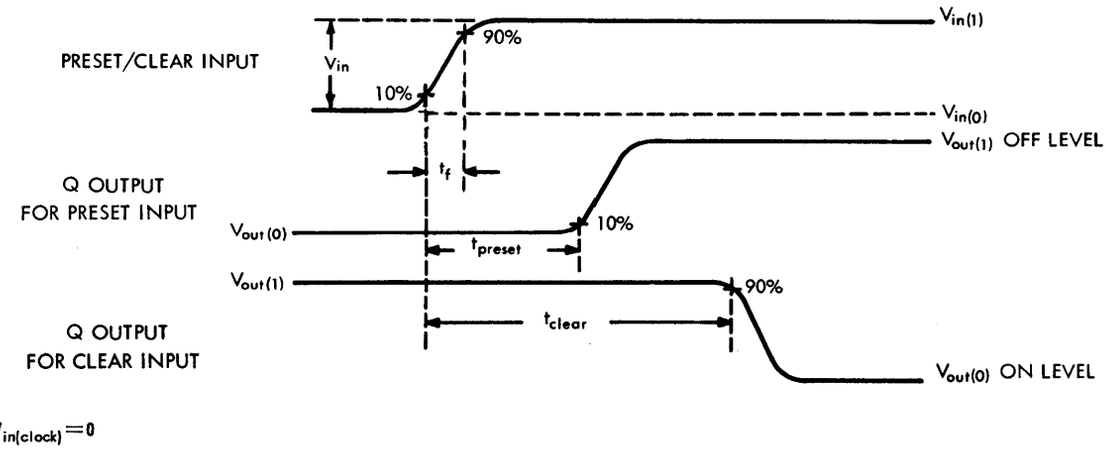


FIGURE 20. TIME TO SET A LOGICAL LEVEL VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



1. $V_{in(clock)} = 0$

FIGURE 21. PRESET/CLEAR TIME VOLTAGE WAVEFORMS

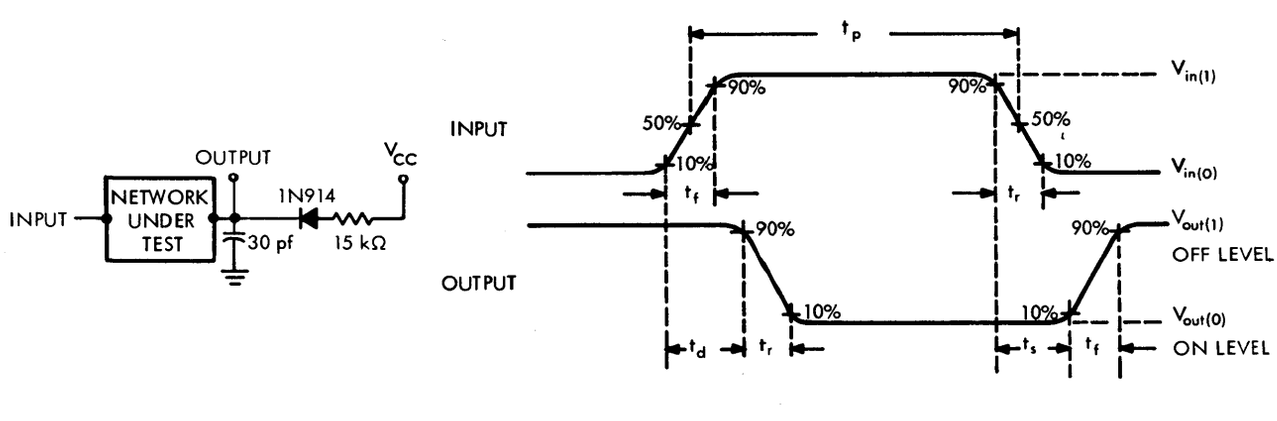
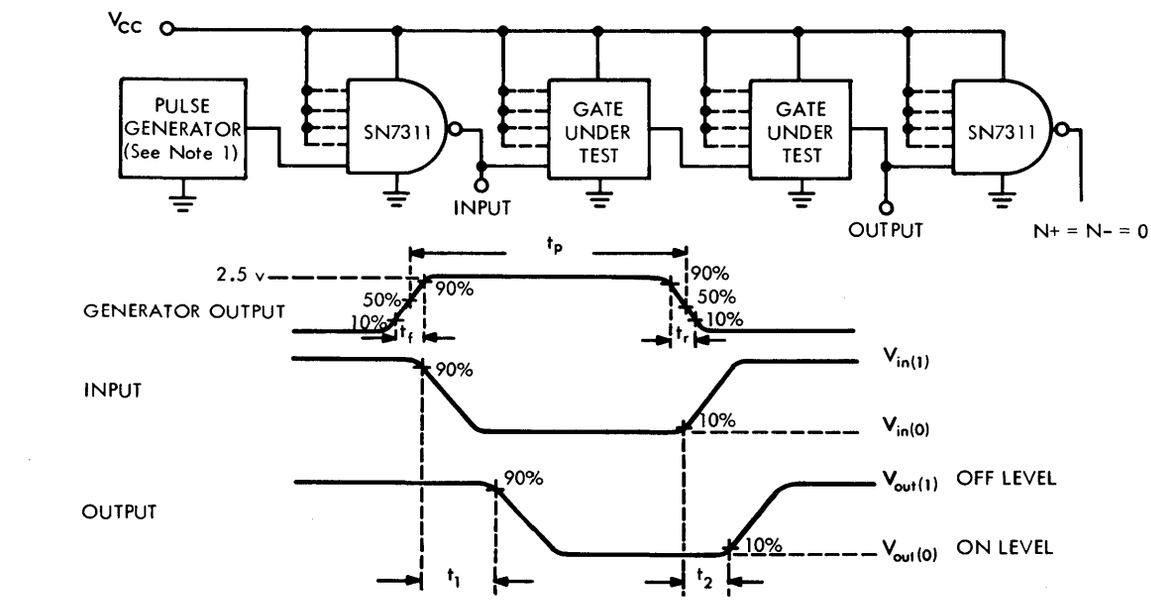


FIGURE 22. GATE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: 1. The generator has the following characteristics: $t_r = t_f = 20$ nsec, $t_p = 500$ nsec, PRR = 1 Mc, $Z_{out} \simeq 50\ \Omega$.

2. Propagation delay: $t_{pd} = \frac{t_1 + t_2}{4}$

FIGURE 23. GATE PROPAGATION DELAY TEST CIRCUIT AND VOLTAGE WAVEFORMS

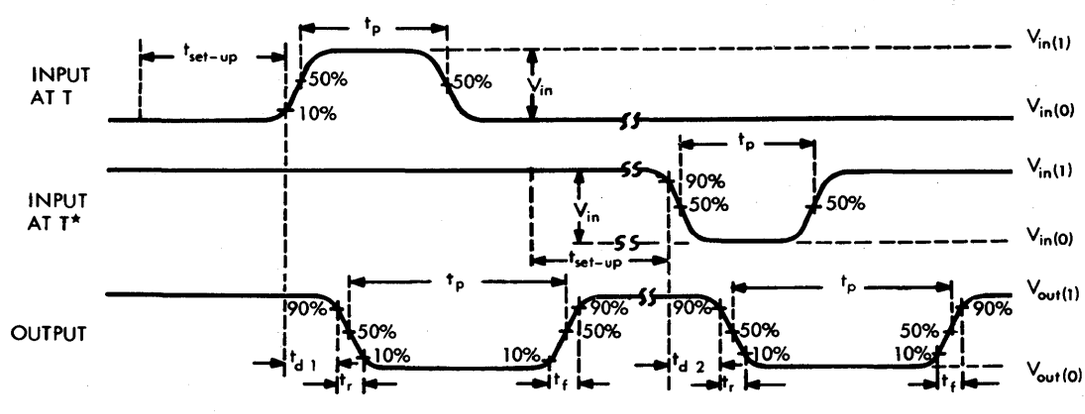


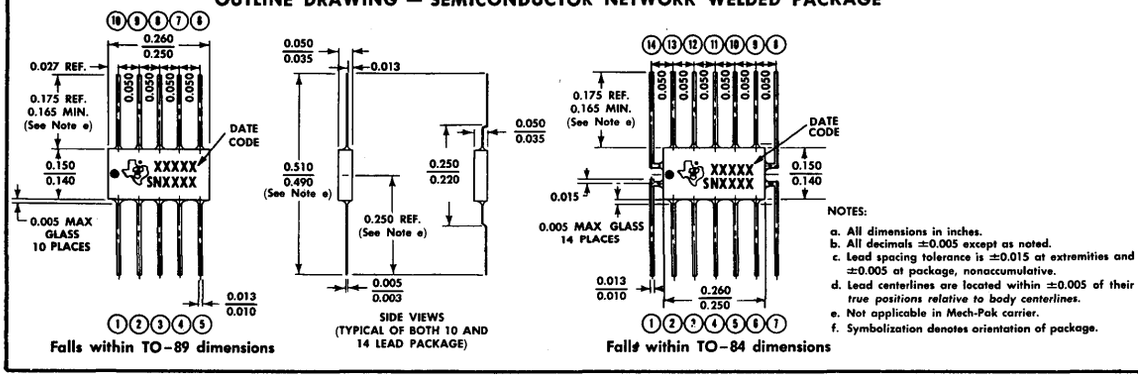
FIGURE 24. ONE-SHOT VOLTAGE WAVEFORMS

MECHANICAL DATA

general

Series 73 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 73 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE

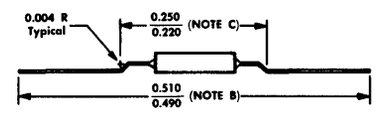


NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their *true positions relative to body centerlines.*
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

FORMED LEADS



NOTES: A. All dimensions in inches
B. Not applicable in Mech-Pak Carrier
C. Measured from centerline of outside bends

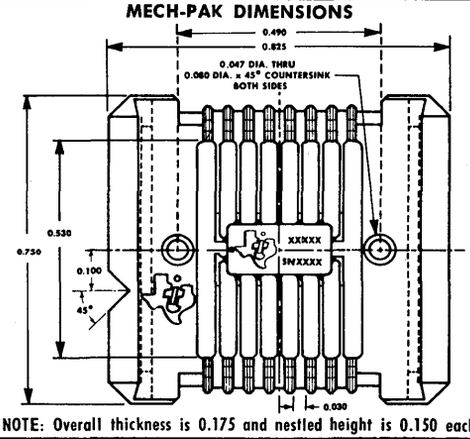
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTE: Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

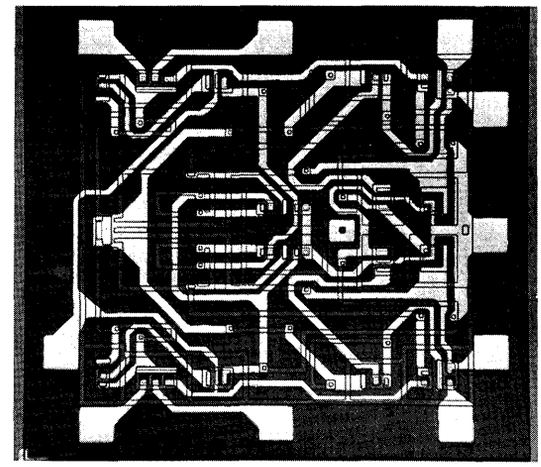
‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

SERIES 15 830
BULLETIN NO. DL-S 668867, NOVEMBER 1966

DIODE-TRANSISTOR LOGIC (DTL) NETWORKS FOR DIGITAL SYSTEMS

application

The series 15 830 networks are designed for use in medium to high-speed digital applications, including data handling, computer and control systems. Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 75°C.



TYPE SN15 850 PULSE-TRIGGERED BINARY BAR

features

LOW SYSTEM COST

- multifunction gates offering low cost per logic function
- electrically designed specifically for monolithic integrated-circuit technology

PERFORMANCE

- high speed
- high d-c noise margins
- low power dissipation
- good fan-out capability

EASE OF DESIGN

- familiar logic configuration (DTL)
- single-ended output — dot-OR logic
- complete family for design flexibility
- single power supply

description

Series 15 830 is a complete family of diode-transistor logic (DTL) which is most attractive when high performance and low cost per function are necessities to system design.

The basic family consists of NAND gates, an expander, a buffer, a power gate, master-slave flip-flops, a pulse-triggered binary and a monostable multivibrator. Dual, triple, and quadruple multifunction gates are available to minimize system package count.

This line features a unique combination of high speed, high d-c noise margin, and low power dissipation. The single-ended output lends itself readily to performing dot-OR logic thus reducing the number of different type functional blocks in a system.

CONTENTS

†Patented by Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

typical operating characteristics, T_A = 0°C to 75°C, supply voltage V_{CC} = 5 V

Speed:	Gate Propagation Delay	25 ns
	Monostable Multivibrator Propagation Delay	20 ns
	Flip-Flop Clock Rate (SN15 831, SN15 845, SN15 848)	7 MHz
	Pulse-Triggered Binary Clock Rate	20 MHz
Fan-Out Capability:	Standard Gates (SN15 830, SN15 846, SN15 862)	8
	Buffer (SN15 832)	25
	Power Gate (SN15 844)	27
	Monostable Multivibrator (SN15 851)	10
	Flip-Flops: SN15 831	7
	SN15 845	12
	SN15 848	11
	Pulse-Triggered Binary	10
D-C Margin:	At logical 1	500 mV
	At logical 0	500 mV
Average Power Dissipation:	Per Gate	5 mW
	Per Flip-Flop	20 mW

design characteristics

Series 15 830 is a complete line of high-speed, high-noise-margin, low-power-dissipation, saturated DTL logic. The circuitry is a modification of the conventional DTL in that it utilizes only one power supply and provides a nonsaturating offset transistor in place of one of the offset diodes.

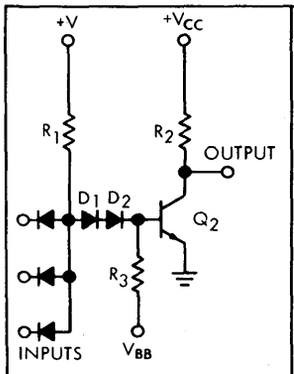


Figure A — Conventional DTL

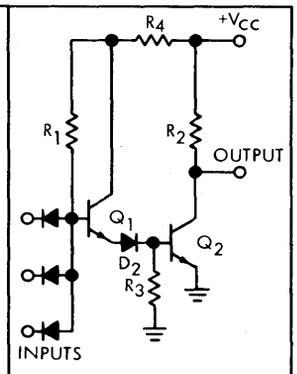


Figure B — Series 15 830

Replacing the offset diode D_1 with transistor Q_1 offers both the manufacturer and the customer a number of advantages:

1. Elimination of the V_{BB} power supply makes one more pin available for multifunction capability, which in turn reduces system package count.
2. Reduction of size of resistor R_3 from 20 kΩ to 5 kΩ produces a substantial reduction in the overall size of the monolithic chip and improves yields. Both of these factors contribute heavily to reducing manufacturing costs.
3. Reduction of turn-off current transients on signal lines is accomplished because the stored charge on the output transistor Q_2 is removed locally by R_3 rather than through diodes D_1 and D_2 onto the input signal lines. These transients are also reduced during switching by the offset transistor Q_1 which operates in the unsaturated mode. This technique eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.
4. The offset transistor Q_1 provides additional drive current to the output transistor Q_2 without requiring high input currents when the input is in the low state. High input currents would limit fan-out of the driving gates. The additional drive to the output transistor permits the use of a smaller base resistor R_3 and relaxes the h_{FE} requirement of the output transistor thus producing higher manufacturing yields.

In order to drive high-fan-out or high-capacity loads, a buffer is available which has a modified double-ended output. This output has a high-sink-current capability when in the ON state and a low-impedance emitter-follower output in the OFF state.

The master-slave flip-flops have AND gate inputs to the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure C):

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

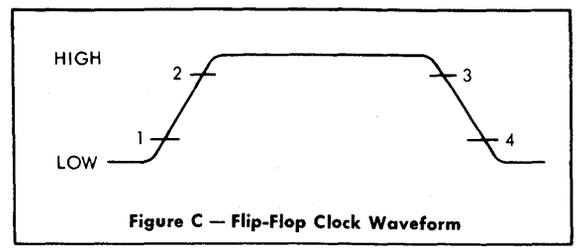


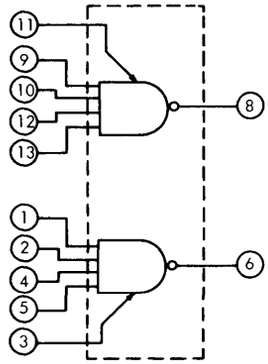
Figure C — Flip-Flop Clock Waveform

The pulse-triggered binary has two 70-pF capacitors in the clock line which provide an input-differentiating network for high-speed clocking applications.

standard line summary

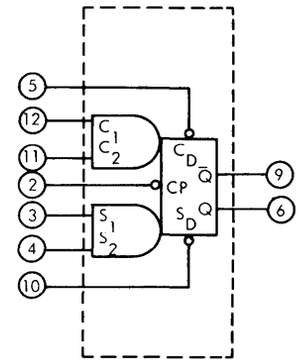
Input and output pin numbers are shown for reference. For all networks shown, V_{CC} is pin (14) (unless otherwise noted) and GND is pin (7). See referenced page for complete pin configuration.

SN15 830 . . . . . See Page 7005
SN15 832 (Buffer) . . . . . See Page 7009
SN15 844 (Power Gate). . . . See Page 7012



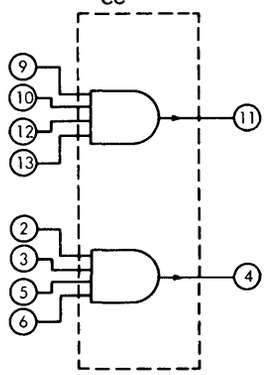
DUAL 4-INPUT NAND/NOR GATES

SN15 831 . . . . . See Page 7007
SN15 845 . . . . . See Page 7014
SN15 848 . . . . . See Page 7019



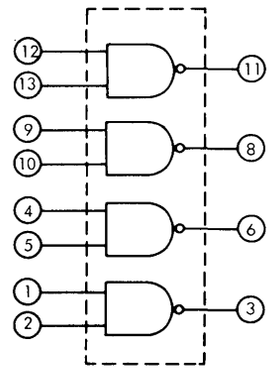
FLIP-FLOPS WITH SET AND CLEAR

SN15 833 . . See Page 7011
(No V_{CC} Terminal)



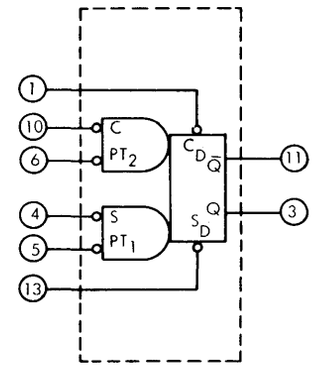
DUAL 4-INPUT EXPANDER

SN15 846 . . See Page 7017



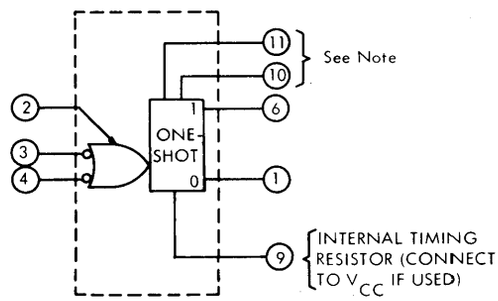
QUADRUPLE 2-INPUT NAND/NOR GATE

SN15 850 . . See Page 7022



PULSE-TRIGGERED BINARY

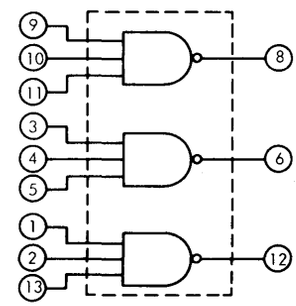
SN15 851 . . . . . See Page 7024



NOTE: External capacitance is added between pins (10) and (11). External resistance bypasses internal timing resistor if connected from (10) to V_{CC}.

MONOSTABLE MULTIVIBRATOR

SN15 862 . . . . See Page 7026



TRIPLE 3-INPUT NAND/NOR GATE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	+8 V
Continuous Output Sink Current (SN15 830, SN15 831, SN15 845, SN15 846, SN15 848, SN15 862)	30 mA
Continuous Output Sink Current (SN15 850, SN15 851)	50 mA
Continuous Output Sink Current (SN15 832, SN15 844)	150 mA
Current Out of Input Terminal	−10 mA
Current Into Input Terminal (except SN15 850 and SN15 851 pin (10))	1 mA
Current Into Input Terminal (SN15 850 and SN15 851 pin (10))	5 mA
Operating Free-Air Temperature Range (See Note 2)	0°C to 75°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies for networks operating at V_{CC} = 5 V, all inputs† at 5 V, and the following output sink current:

SN15 830†, SN15 846, SN15 850, SN15 862	12 mA
SN15 831	10.5 mA
SN15 832†	36 mA
SN15 844†	40 mA
SN15 845	16.8 mA
SN15 848	14.6 mA
SN15 851	15 mA

†Expander nodes open

logic definition

Series 15 830 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input current requirements

Weighted values of input current requirements reflect worst case conditions for T_A = 0°C to 75°C and V_{CC} = 5 V. Each gate input requires that no more than −1.4 mA flow out of the input at a logical 0 input voltage level; therefore, one input load is −1.4 mA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS

NETWORK	TYPE	INPUT	NUMBER OF LOADS
GATES AND EXPANDER	SN15 830, SN15 832, SN15 833, SN15 844, SN15 846, SN15 862	Each Input	1
FLIP-FLOPS	SN15 831	Each Input (Synchronous or Asynchronous)	⅔
		Clock	2
	SN15 845 and SN15 848	Synchronous Inputs	⅔
		Asynchronous and Clock Inputs	2
PULSE-TRIGGERED BINARY	SN15 850	Synchronous or Asynchronous	11½
MONOSTABLE MULTIVIBRATOR	SN15 851	Each Input	2

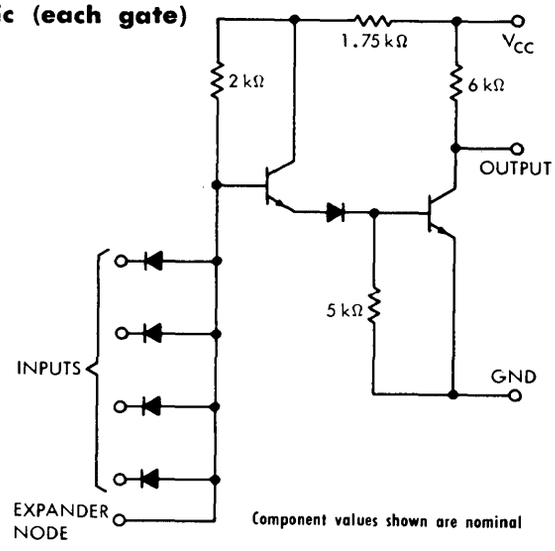
output drive capability

Weighted values of fan-out reflect the ability of an output to sink current (into the output terminal) under recommended operating conditions and are specified as positive values. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

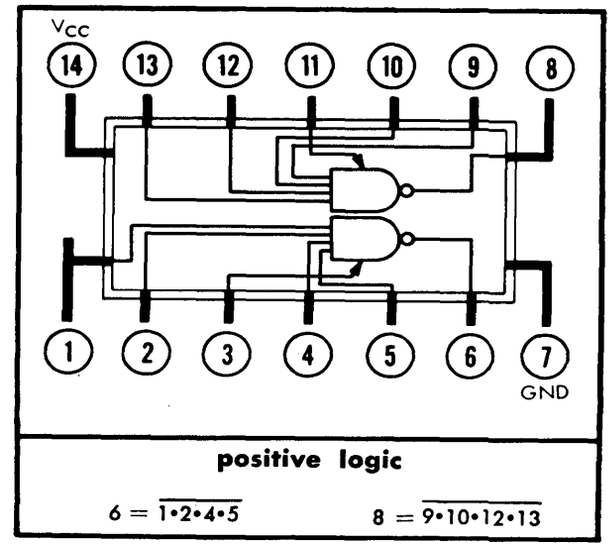
WEIGHTED VALUES OF FAN-OUT

NETWORK	TYPE	OUTPUT	LOADS
GATES	SN15 830, SN15 846, SN15 862	Each Output	8
BUFFER	SN15 832	Each Output	25
POWER GATE	SN15 844	Each Output	27
FLIP-FLOPS	SN15 831	Q or $\overline{Q}$	7
	SN15 845	Q or $\overline{Q}$	12
	SN15 848	Q or $\overline{Q}$	11
PULSE-TRIGGERED BINARY	SN15 850	Q or $\overline{Q}$	8
MONOSTABLE MULTIVIBRATOR	SN15 851	Each Output	10

schematic (each gate)



Component values shown are nominal



positive logic

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V

Maximum Fan-Out From Each Output 8

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 12$ mA, $T_A = 25°C$		0.45	V
			$V_{in} = 2$ V, $I_{sink} = 12$ mA, $T_A = 0°C$		0.45	V
			$V_{in} = 1.8$ V, $I_{sink} = 11.4$ mA, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
			$V_{in} = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0°C$	2.6		V
			$V_{in} = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75°C$	2.5		V

† Expander nodes are open unless otherwise noted:

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage at expander input node, V_{inX}	3	$V_{inX} = 1.8$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
$I_{in(1)}$	Logical 1 level input current	4	$V_{in} = 4$ V, $T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level input current	5	$V_{in} = 0.45$ V, $V_R = 4$ V, $T_A = 25°C$ and 0°C		−1.4	mA
			$V_{in} = 0.5$ V, $V_R = 4$ V, $T_A = 75°C$		−1.33	mA
$I_{out(1)}$	Output reverse current (off level)	6	$V_{out} = 5$ V, $T_A = 25°C$		100	μA
I_{OS}	Short-circuit output current	7	$V_{out} = 0$, $T_A = 25°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 0°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 75°C$		−1.25	mA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	$T_A = 25°C$		8	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	$V_{CC} = 8$ V, $T_A = 25°C$		8	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$, $C_L = 50$ pF	10	30	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 3.9$ kΩ, $C_L = 30$ pF	25	80	ns

† Expander nodes are open unless otherwise noted.

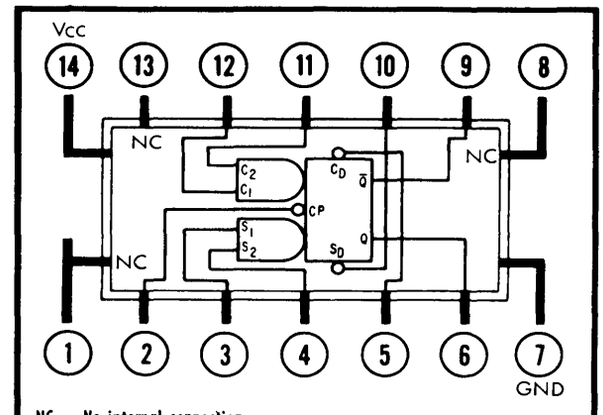
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	*Indeterminate*

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V
Maximum Fan-Out From Each Output 7

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage on level at Q or $\overline{Q}$	10	$V_{CP(S)} = 0.95$ V, $I_{sink} = 10.5$ mA, $T_A = 25°C$		0.45	V
			$V_{CP(S)} = 1$ V, $I_{sink} = 10.5$ mA, $T_A = 0°C$		0.45	V
			$V_{CP(S)} = 0.85$ V, $I_{sink} = 10.2$ V, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage off level at Q or $\overline{Q}$	11	$V_1 = 1.9$ V, $V_2 = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
			$V_1 = 2$ V, $V_2 = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0°C$	2.6		V
			$V_1 = 1.8$ V, $V_2 = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75°C$	2.5		V
$V_{out(1)}$	Logical 1 output voltage off level at Q or $\overline{Q}$	12	$V_1 = 1.9$ V, $V_2 = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
			$V_1 = 2$ V, $V_2 = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0°C$	2.6		V
			$V_1 = 1.8$ V, $V_2 = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75°C$	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	13	$V_{in} = 1.1$ V, $V_{CP(0)} = 0.45$ V, $T_A = 25°C$		−2.8	mA
			$V_{in} = 1.2$ V, $V_{CP(0)} = 0.45$ V, $T_A = 0°C$		−2.8	mA
			$V_{in} = 0.95$ V, $V_{CP(0)} = 0.5$ V, $T_A = 75°C$		−2.67	mA
$I_{CP(1)}$	Logical 1 level clock-input *reverse current*	14	$V_{CP} = 4$ V, $T_A = 25°C$ and $0°C$		30	μA
			$V_{CP} = 4$ V, $T_A = 75°C$		40	μA

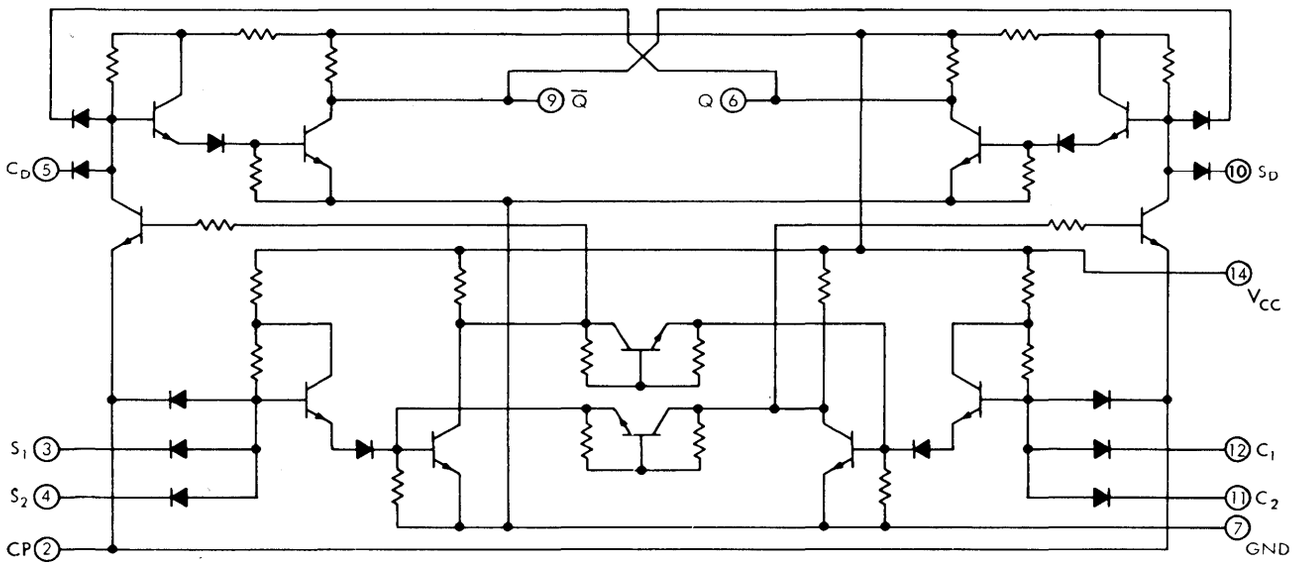
electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	$V_{in} = 4$ V, $T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	16	$V_{in} = 0.45$ V, $T_A = 25°C$ and 0°C		−1.05	mA
			$V_{in} = 0.5$ V, $T_A = 75°C$		−1	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	17	$V_{in} = 4$ V, $T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	18	$V_{in} = 0.45$ V, $T_A = 25°C$ and 0°C		−0.95	mA
			$V_{in} = 0.5$ V, $T_A = 125°C$		−0.9	mA
$I_{CC(0)}$	Logical 0 level supply current	19	$T_A = 25°C$		14	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	$V_{CC} = 8$ V, $T_A = 25°C$		18	mA

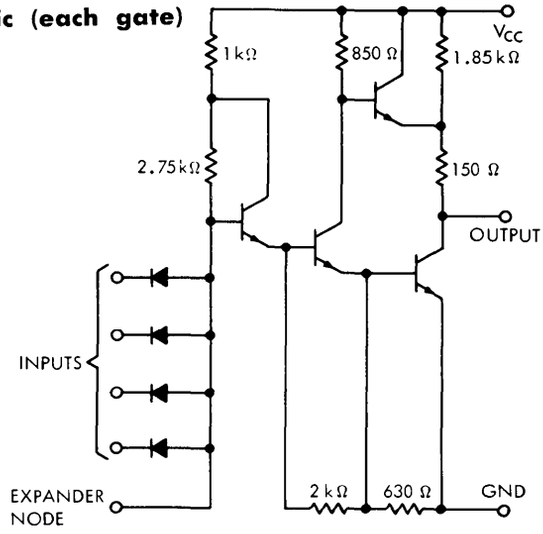
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	$R_l = 400\ \Omega$ $C_L = 50$ pF	5	75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_l = 3.9$ kΩ $C_L = 30$ pF	5	75	ns

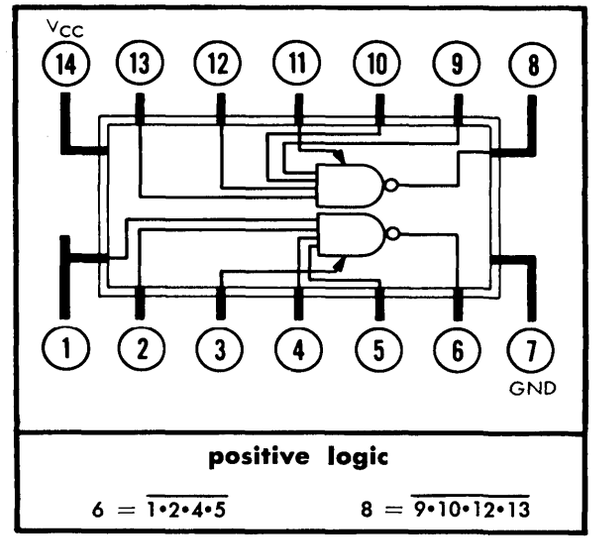
schematic



schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V

Maximum Fan-Out From Each Output 25

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 36$ mA, $T_A = 25°C$		0.45	V
			$V_{in} = 2$ V, $I_{sink} = 36$ mA, $T_A = 0°C$		0.45	V
			$V_{in} = 1.8$ V, $I_{sink} = 34$ mA, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -2.5$ mA, $T_A = 25°C$	2.6		V
			$V_{in} = 1.2$ V, $I_{load} = -2$ mA, $T_A = 0°C$	2.6		V
			$V_{in} = 0.95$ V, $I_{load} = -3$ mA, $T_A = 75°C$	2.5		V

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

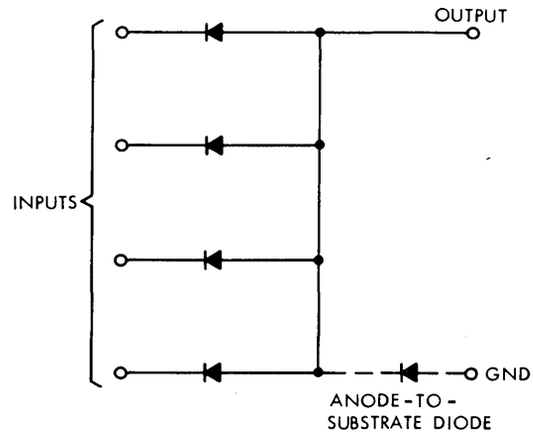
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage input at expander node, V_{inX}	3	$V_{inX} = 1.8$ V, $I_{load} = -2.5$ mA, $T_A = 25°C$	2.6		V
$I_{in(1)}$	Logical 1 level input current	4	$V_{in} = 4$ V, $T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level input current	5	$V_{in} = 0.45$ V, $V_R = 4$ V, $T_A = 25°C$ and 0°C		−1.4	mA
			$V_{in} = 0.5$ V, $V_R = 4$ V, $T_A = 75°C$		−1.33	mA
$I_{out(1)}$	Output reverse current (off level)	6	$V_{out} = 5$ V, $T_A = 25°C$		100	μA
I_{OS}	Short-circuit output current	7	$V_{out} = 0$, $T_A = 25°C$	−16		mA
			$V_{out} = 0$, $T_A = 0°C$	−15		mA
			$V_{out} = 0$, $T_A = 75°C$	−14		mA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	$T_A = 25°C$		30	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	$V_{CC} = 8$ V, $T_A = 25°C$		8	mA

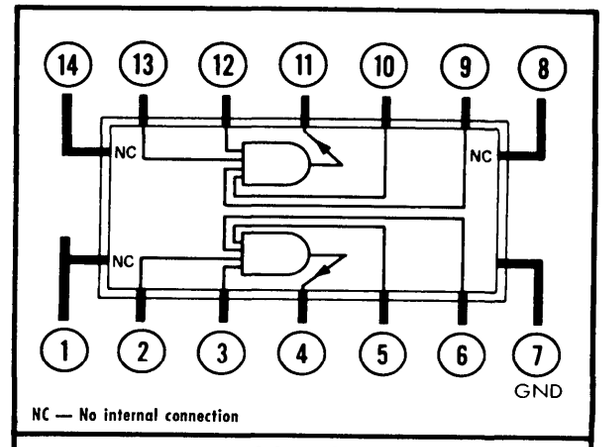
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 150\ \Omega$, $C_L = 500$ pF	15	40	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 510\ \Omega$, $C_L = 500$ pF	25	80	ns

† Expander nodes are open unless otherwise noted.

schematic (each expander)





NC — No internal connection

positive logic

4 = 2•3•5•6 11 = 9•10•12•13

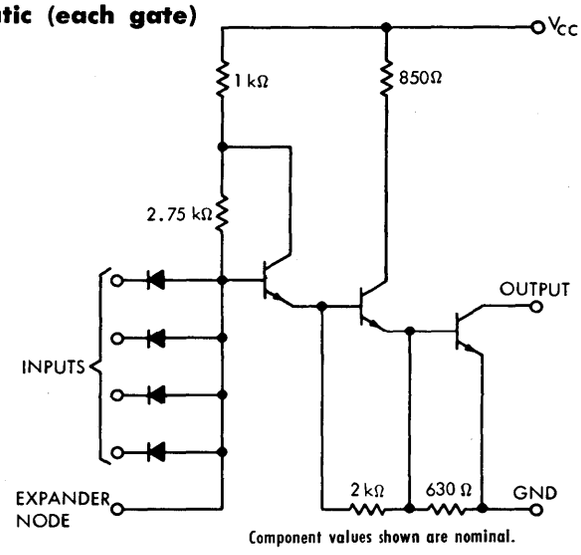
electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_F	Input diode forward voltage	21	I_{out} = 2 mA, T_A = 25°C	0.68	0.82	V
			I_{out} = 2 mA, T_A = 0°C	0.75	0.9	V
			I_{out} = 2 mA, T_A = 75°C	0.6	0.75	V
$I_{in\ R}$	Input diode reverse current	22	V_{in} = 4 V, T_A = 25°C		5	μA
			V_{in} = 4 V, T_A = 0°C		5	μA
			V_{in} = 4 V, T_A = 75°C		10	μA
$I_{out\ R}$	Anode-to-substrate reverse current	23	V_{out} = 4 V, T_A = 25°C		10	μA

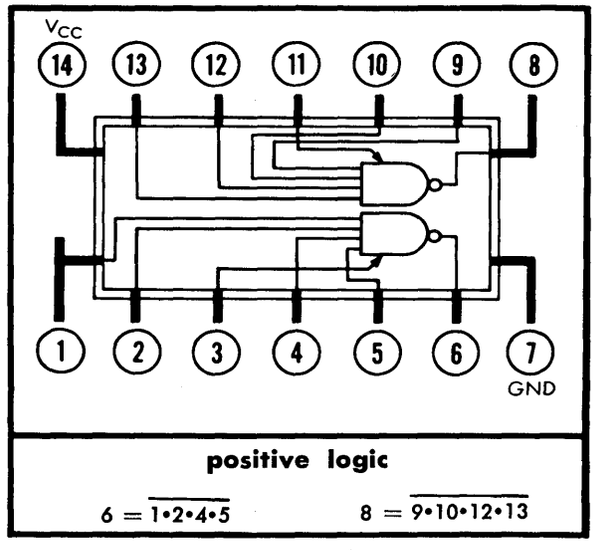
NOTE: A total of four expanders may be connected to an expandable gate to provide a fan-in of 20.

TYPE SN15 844
DUAL 4-INPUT NAND/NOR POWER GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V

Maximum Fan-Out From Each Output 27

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 40$ mA, $T_A = 25°C$		0.45	V
			$V_{in} = 2$ V, $I_{sink} = 40$ mA, $T_A = 0°C$		0.45	V
			$V_{in} = 1.8$ V, $I_{sink} = 36$ mA, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	24	$I_{sink} = 5$ mA, $T_A = 25°C$	6		V
$I_{in(1)}$	Logical 1 level input current	4	$V_{in} = 4$ V, $T_A = 25°C$ and $0°C$		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA

† Expander nodes are open unless otherwise noted.

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{in(0)}$	Logical 0 level input current	5	$V_{in} = 0.45$ V, $V_R = 4$ V, $T_A = 25°C$ and 0°C		−1.4	mA
			$V_{in} = 0.5$ V, $V_R = 4$ V, $T_A = 75°C$		−1.33	mA
$I_{out\ (1)}$	Output reverse current (off level, worst-case voltage at any input)	25	$V_{in} = 1.1$ V, $V_{out} = 4.5$ V, $T_A = 25°C$		100	μA
			$V_{in} = 1.2$ V, $V_{out} = 4.5$ V, $T_A = 0°C$		100	μA
			$V_{in} = 0.95$ V, $V_{out} = 4.5$ V, $T_A = 75°C$		200	μA
$I_{out\ (1)}$	Output reverse current (off level, worst-case voltage at expander input)	26	$V_{inX} = 1.8$ V, $V_{out} = 4.5$ V, $T_A = 25°C$		100	μA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	$T_A = 25°C$		24	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	$V_{CC} = 8$ V $T_A = 25°C$		8	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 150\ \Omega$, $C_L = 100$ pF	10	35	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 510\ \Omega$, $C_L = 20$ pF	15	50	ns

† Expander nodes are open unless otherwise noted.

TYPE SN15845
FLIP-FLOP WITH SET AND CLEAR

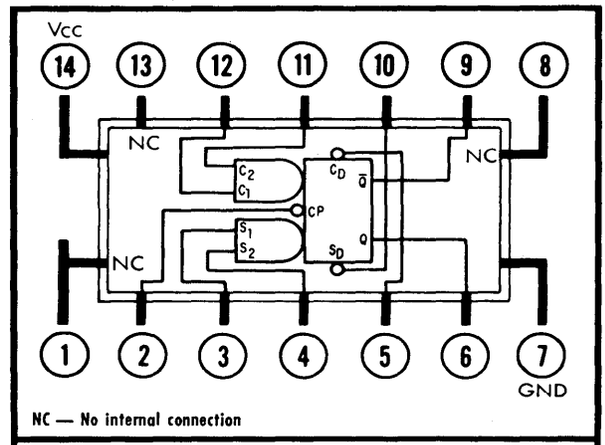
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V
Maximum Fan-Out From Each Output 12

electrical characteristics at V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	27 and 28	V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{sink} = 16.8 mA, T_A = 25°C		0.45	V
			V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{sink} = 16.8 mA, T_A = 0°C		0.45	V
			V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{sink} = 16 mA, T_A = 75°C		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_1 = 5 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_1 = 5 V, V_2 = 1.2 V, I_{load} = –0.12 mA, T_A = 0°C	2.6		V
			V_1 = 5 V, V_2 = 0.95 V, I_{load} = –0.12 mA, T_A = 75°C	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	29	V_{in} = 1.1 V, V_{CP} = 0.45 V, T_A = 25°C		–2.8	mA
			V_{in} = 1.2 V, V_{CP} = 0.45 V, T_A = 0°C		–2.8	mA
			V_{in} = 0.95 V, V_{CP} = 0.5 V, T_A = 75°C		–2.67	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	30	V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25°C and 0°C		20	μA
			V_{CC} = 4 V, V_{CP} = 4 V, T_A = 75°C		30	μA

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

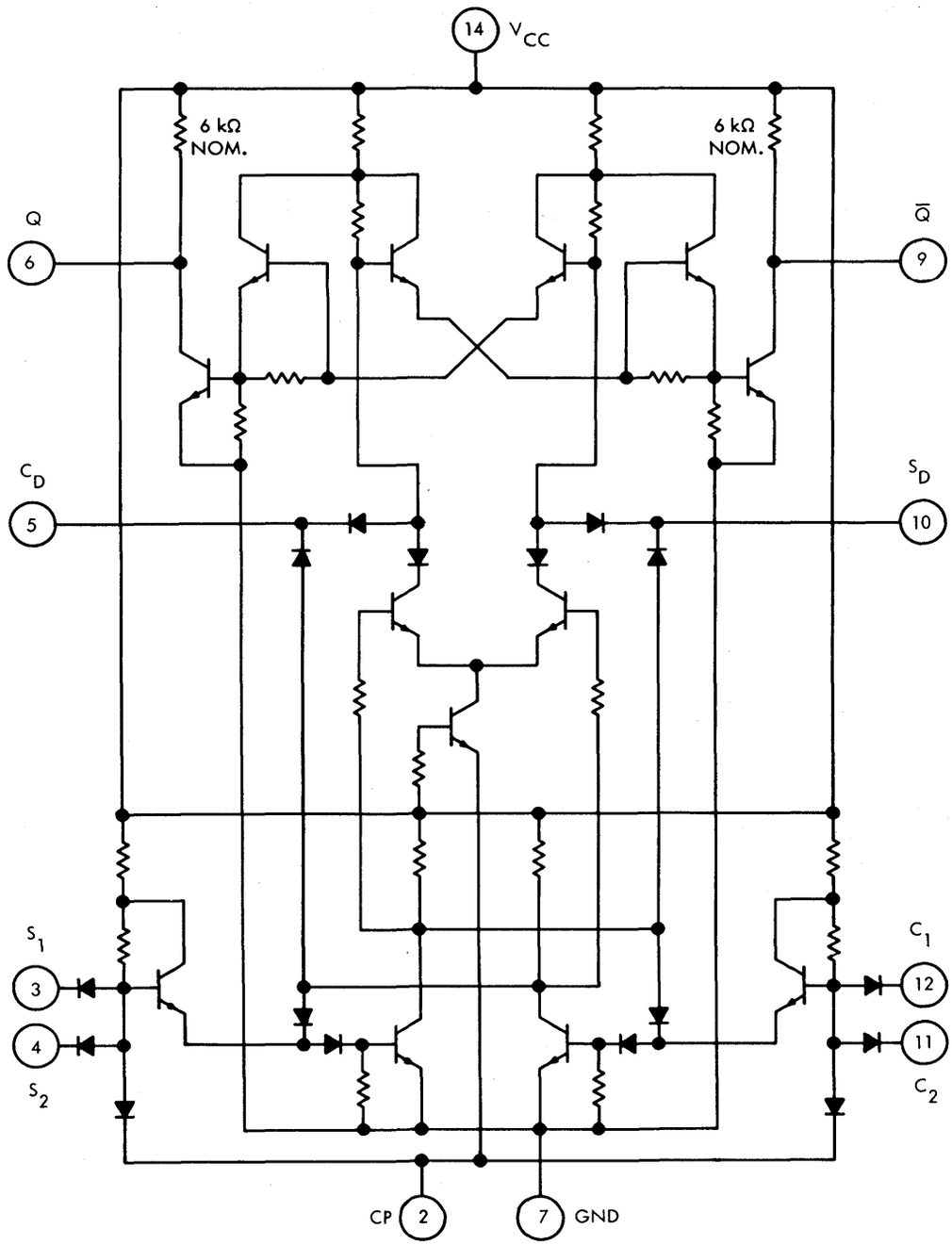
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	$V_{in} = 4$ V, $T_A = 25°C$ and $0°C$		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	31	$V_{in} = 0.45$ V, $V_1 = 4$ V, $V_{CP} = 4$ V, $T_A = 25°C$ and $0°C$		−0.95	mA
			$V_{in} = 0.5$ V, $V_1 = 4$ V, $V_{CP} = 4$ V, $T_A = 75°C$		−0.9	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	$V_{in} = 4$ V, $V_1 = 5$ V, $T_A = 25°C$ and $0°C$		5	μA
			$V_{in} = 4$ V, $V_1 = 5$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	$V_{in} = 0.45$ V, $T_A = 25°C$ and $0°C$		−2.1	mA
			$V_{in} = 0.5$ V, $T_A = 75°C$		−2	mA
I_{OS}	Short-circuit output current	18	$V_{in} = 5$ V, $V_{out} = 0$, $T_A = 25°C$ and $0°C$	−0.59	−1.41	mA
			$V_{in} = 5$ V, $V_{out} = 0$, $T_A = 75°C$	−0.55	−1.38	mA
$I_{CC(0)}$	Logical 0 level supply current	19	$T_A = 25°C$		15	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	$V_{CC} = 8$ V, $T_A = 25°C$		17	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	$R_1 = 330\ \Omega$, $C_L = 50$ pF	5	75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 2\ k\Omega$, $C_L = 30$ pF	5	75	ns

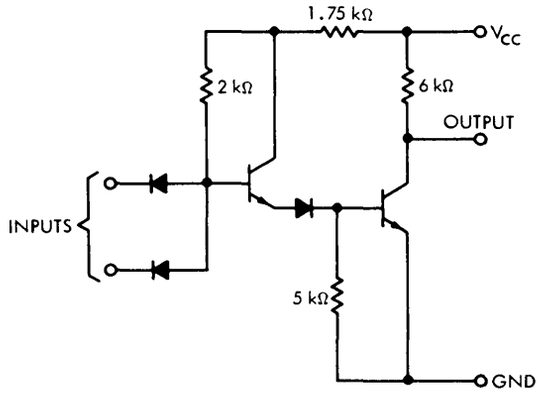
TYPE SN15 845
FLIP-FLOP WITH SET AND CLEAR

schematic

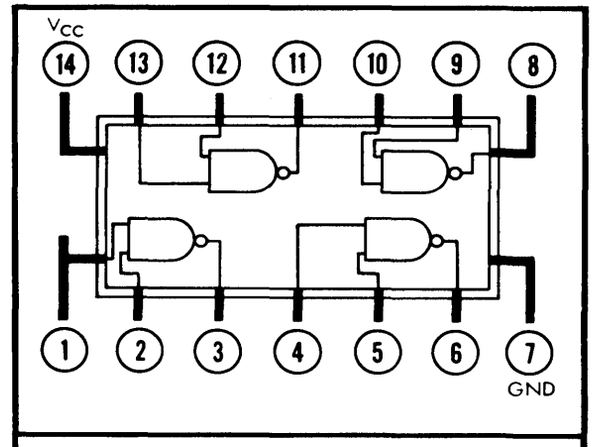


NOTE: Pins (1), (8), and (13) — no internal connection.

schematic (each gate)



Component values shown are nominal.



positive logic

$3 = \overline{1 \cdot 2}$ $6 = \overline{4 \cdot 5}$ $8 = \overline{9 \cdot 10}$ $11 = \overline{12 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V

Maximum Fan-Out From Each Output 8

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 12$ mA, $T_A = 25°C$		0.45	V
			$V_{in} = 2$ V, $I_{sink} = 12$ mA, $T_A = 0°C$		0.45	V
			$V_{in} = 1.8$ V, $I_{sink} = 11.4$ mA, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
			$V_{in} = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0°C$	2.6		V
			$V_{in} = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75°C$	2.5		V

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	$V_{in} = 4$ V, $T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level input current	5	$V_{in} = 0.45$ V, $V_R = 4$ V, $T_A = 25°C$ and 0°C		−1.4	mA
			$V_{in} = 0.5$ V, $V_R = 4$ V, $T_A = 75°C$		−1.33	mA
$I_{out(1)}$	Output reverse current (off level)	6	$V_{out} = 5$ V, $T_A = 25°C$		100	μA
I_{OS}	Short-circuit output current	7	$V_{out} = 0$, $T_A = 25°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 0°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 75°C$		−1.25	mA
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	$T_A = 25°C$		16	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	$V_{CC} = 8$ V, $T_A = 25°C$		16	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$, $C_L = 50$ pF	10	30	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 3.9$ kΩ, $C_L = 30$ pF	25	80	ns

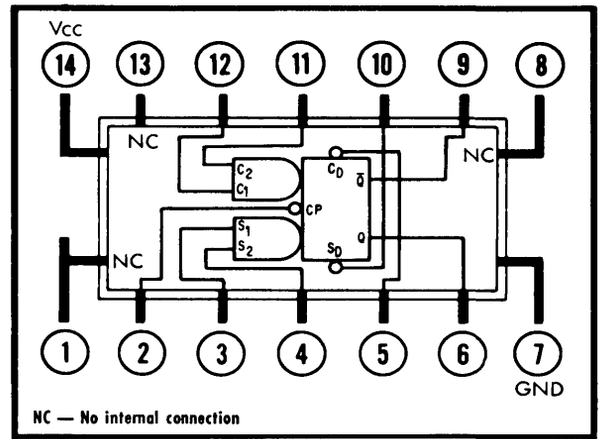
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



NC — No internal connection

positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V
Maximum Fan-Out From Each Output 11

electrical characteristics at V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	27 and 28	V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{sink} = 15.4 mA, T_A = 25°C		0.45	V
			V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{sink} = 15.4 mA, T_A = 0°C		0.45	V
			V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{sink} = 14.6 mA, T_A = 75°C		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_1 = 5 V, V_2 = 1.1 V, I_{load} = –0.12 mA, T_A = 25°C	2.6		V
			V_1 = 5 V, V_2 = 1.2 V, I_{load} = –0.12 mA, T_A = 0°C	2.6		V
			V_1 = 5 V, V_2 = 0.95 V, I_{load} = –0.12 mA, T_A = 75°C	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	29	V_{in} = 1.1 V, V_{CP} = 0.45 V, T_A = 25°C		–2.8	mA
			V_{in} = 1.2 V, V_{CP} = 0.45 V, T_A = 0°C		–2.8	mA
			V_{in} = 0.95 V, V_{CP} = 0.5 V, T_A = 75°C		–2.67	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	30	V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25°C and 0°C		20	μA
			V_{CC} = 4 V, V_{CP} = 4 V, T_A = 75°C		30	μA

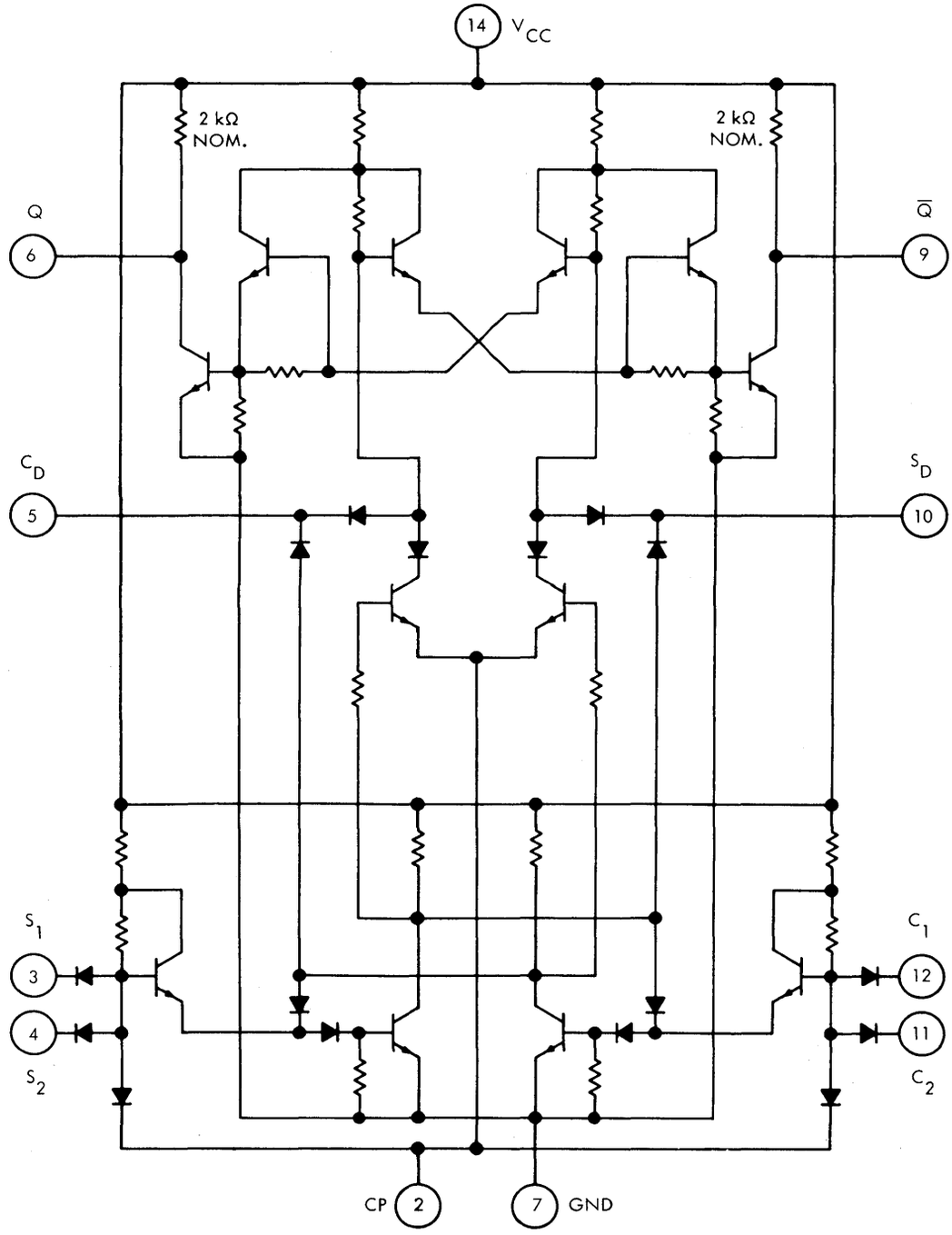
electrical characteristics (continued) at V_{CC} = 5 V (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{in} = 4 V, T_A = 25°C and 0°C		5	μA
			V_{in} = 4 V, T_A = 75°C		10	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	31	V_{in} = 0.45 V, V_1 = 4 V, V_{CP} = 4 V, T_A = 25°C and 0°C		−0.95	mA
			V_{in} = 0.5 V, V_1 = 4 V, V_{CP} = 4 V, T_A = 75°C		−0.9	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	V_{in} = 4 V, V_1 = 5 V, T_A = 25°C and 0°C		5	μA
			V_{in} = 4 V, V_1 = 5 V, T_A = 75°C		10	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	V_{in} = 0.45 V, T_A = 25°C and 0°C		−2.1	mA
			V_{in} = 0.5 V, T_A = 75°C		−2	mA
I_{OS}	Short-circuit output current	18	V_{in} = 5 V, V_{out} = 0, T_A = 25°C and 0°C	−0.59	−1.41	mA
			V_{in} = 5 V, V_{out} = 0, T_A = 75°C	−0.55	−1.38	mA
$I_{CC(0)}$	Logical 0 level supply current	19	T_A = 25°C		15	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 V, T_A = 25°C		17	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	R_1 = 330 Ω, C_L = 50 pF	5	65	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 2 kΩ, C_L = 30 pF	5	75	ns

schematic



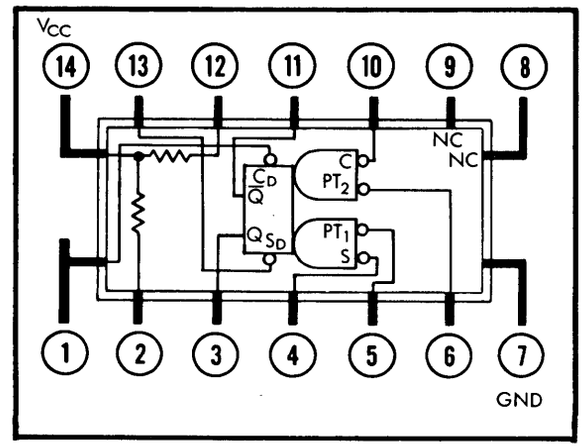
NOTE: Pins (1), (8) and (13) – no internal connection.

logic

TRUTH TABLES

SYNCHRONOUS					
t_n PULSE INPUT				t_{n+1} OUTPUT	
S	C	PT_1	PT_2	Q	$\overline{Q}$
1	X	X	1	Qn	$\overline{Q}$n
X	1	1	X	Qn	$\overline{Q}$n
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S_D	C_D	Q	$\overline{Q}$
1	1	Qn	$\overline{Q}$n
0	1	0	1
1	0	1	0
0	0	1	1



NOTES:
1. *X indicates that either a logical 1 or a logical 0 may be present.*
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT_1 and PT_2 indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V
Maximum Fan-Out From Each Output 8

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	34	V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.45	V
			V_{in} = 2 V, I_{sink} = 12 mA, T_A = 0°C		0.45	V
			V_{in} = 1.8 V, I_{sink} = 11.4 mA, T_A = 75°C		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	35	V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{load} = −1.5 mA, T_A = 25°C	2.6		V
			V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{load} = −1.5 mA, T_A = 0°C	2.6		V
			V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{load} = −1.5 mA, T_A = 75°C	2.5		V
I_{inPT}	Pulse-triggered-input current	36	V_{in} = 8 V, T_A = 25°C and 0°C		5	μA
			V_{in} = 8 V, T_A = 75°C		10	μA
$I_{in(0)}$	Logical 0 level-input current at C or S	37	V_{in} = 0.45 V, T_A = 25°C and 0°C		−2.1	mA
			V_{in} = 0.5 V, T_A = 75°C		−2	mA
$I_{in(0)}$	Logical 0 level at C_D or S_D input current	37	V_{in} = 0.45 V, T_A = 25°C and 0°C		−1.6	mA
			V_{in} = 0.5 V, T_A = 75°C		−1.52	mA

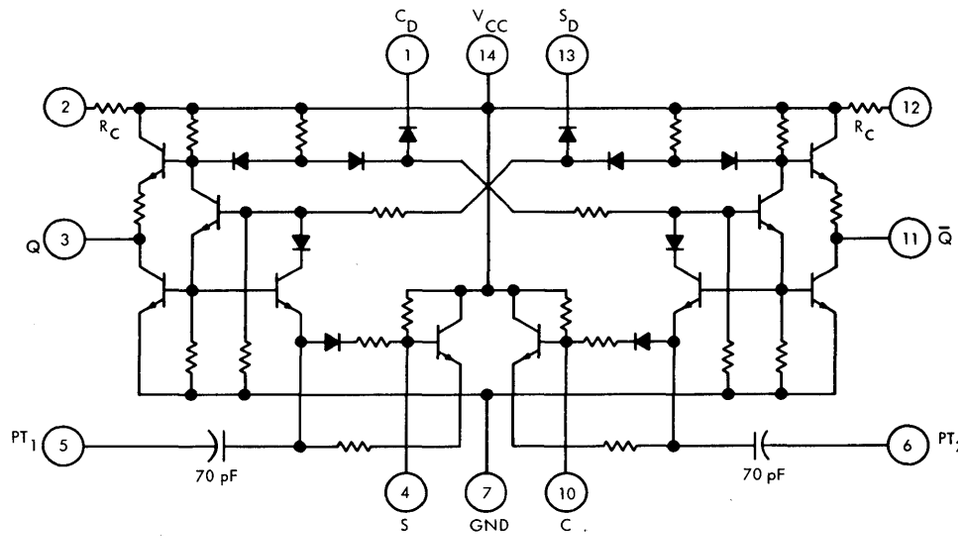
electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current at C_D or S_D	38	$V_{in} = 4$ V,	$T_A = 25°C$ and 0°C		5	μA
			$V_{in} = 4$ V,	$T_A = 75°C$		10	μA
I_{RC}	Current through resistor R_C	39	$V_{in} = 0$,	$T_A = 25°C$	–3.3	–7.9	mA
I_{OS}	Short-circuit output current	40	$V_{out} = 0$,	$T_A = 25°C$ and 0°C	–13.7	–29	mA
			$V_{out} = 0$,	$T_A = 75°C$	–12.6	–28	mA
$I_{out(1)}$	Output reverse current (off level)	40	$V_{out} = 4.5$ V,	$T_A = 25°C$ and 0°C		150	μA
$I_{CC(0)}$	Logical 0 level supply current	41	$T_A = 25°C$			9.3	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	42	$V_{CC} = 8$ V,	$T_A = 25°C$		19.6	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	53	$R_1 = 400\ \Omega$,	$C_L = 100$ pF	5	32	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 3.9\ k\Omega$,	$C_L = 100$ pF	5	25	ns

schematic



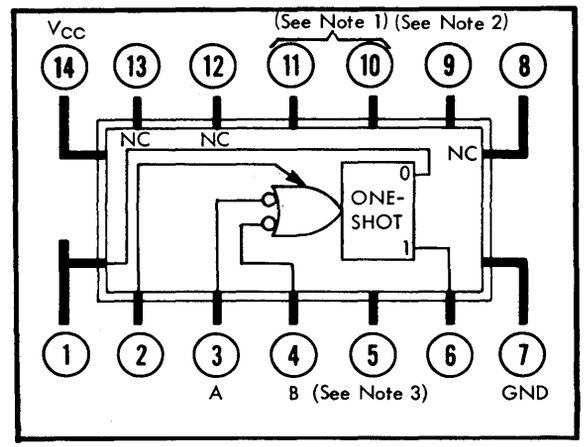
TYPE SN15 851
MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE

t_n INPUT		t_{n+1} INPUT		OUTPUT
A	B	A	B	
1	1	1	1	INHIBIT
1	1	1	0	ONE-SHOT
1	1	0	1	ONE-SHOT
1	1	0	0	ONE-SHOT
0	1	X	X	INHIBIT
1	0	X	X	INHIBIT
0	0	X	X	INHIBIT

NOTES: a. t_n = time before input transition.
b. t_{n+1} = time after input transition.
c. X indicates that either a logical 1 or a logical 0 may be present.



NOTES: 1. External resistor and capacitor may be used between pins (10), (11), and (14) to control one-shot pulse width.
2. To use the internal timing resistor, connect pin (9) to pin (14).
3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V
Maximum Fan-Out From Each Output 10
Input Pulse Characteristics:
Minimum Negative-Going Transition . . . . . 1 V
Maximum Input Fall Time Per Volt . . . . . 25 ns/V
Maximum Duty Cycle 40%

electrical characteristics at V_{CC} = 5 V

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	43	I_{sink} = 15 mA, T_A = 25°C and 0°C		0.45	V
			I_{sink} = 14.5 mA, T_A = 75°C		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	44	I_{load} = −0.18 mA, T_A = 25°C and 0°C	2.6		V
			I_{load} = −0.18 mA, T_A = 75°C	2.5		V
$I_{in(1)}$	Logical 1 level input current	45	V_{in} = 4 V, T_A = 25°C and 0°C		5	μA
			V_{in} = 4 V, T_A = 75°C		10	μA
$I_{in(0)}$	Logical 0 level input current	46	V_1 = 4 V, V_2 = 0.45 V, T_A = 25°C and 0°C	−1.35	−2.8	mA
			V_1 = 4 V, V_2 = 0.5 V, T_A = 75°C	−1.25	−2.63	mA

†Expander node is open unless otherwise noted.

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

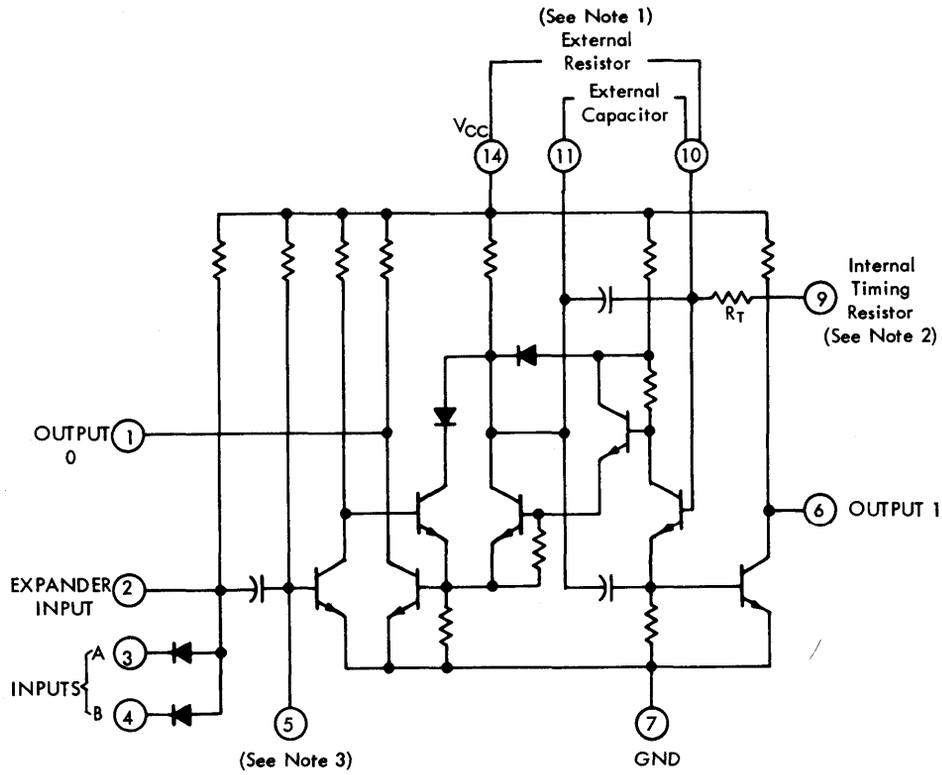
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
I_{RT}	Current through internal timing resistor R_T	47	$V_{in} = 5$ V, $T_A = 25°C$	0.4	0.75	mA
I_{SC}	Short circuit current at expander node or pin (11)	48	$V_{in} = 0$, $T_A = 25°C$ and 0°C	−0.8		mA
			$V_{in} = 0$, $T_A = 75°C$	−0.75		mA
I_{CC}	Supply current	49	$T_A = 25°C$		12	mA
$I_{CC(max)}$	Supply current at maximum V_{CC}	50	$V_{CC} = 8$ V, $T_A = 25°C$		26.7	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	54	$R_1 = 300\ \Omega$, $C_L = 50$ pF		50	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level				50	ns
t_p	Pulse width			50	175	ns

† Expander nodes are open unless otherwise noted.

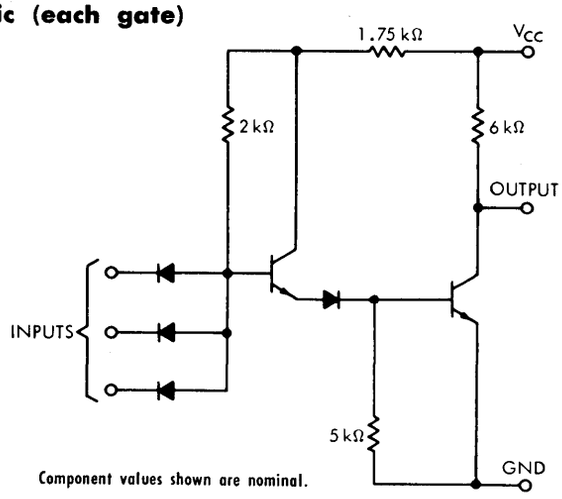
schematic



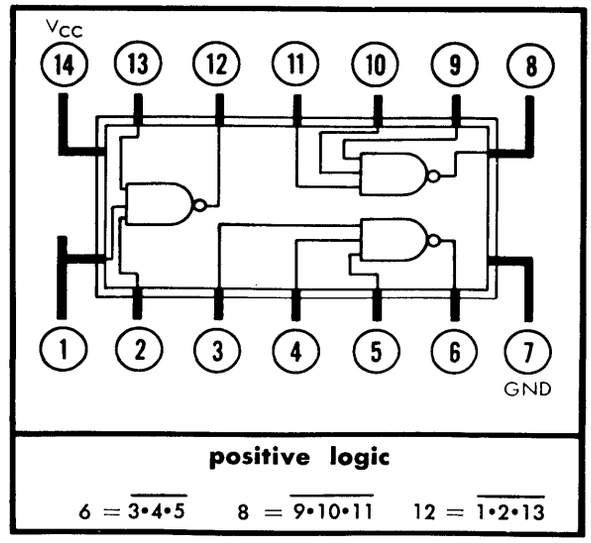
NOTES: 1. External resistor and capacitor may be used (as indicated above) between pins (10), (11), and (14) to control one-shot pulse width.
2. To use the internal timing resistor, connect pin (9) to pin (14).
3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

TYPE SN15 862
TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$6 = \overline{3 \cdot 4 \cdot 5}$ $\quad 8 = \overline{9 \cdot 10 \cdot 11}$ $\quad 12 = \overline{1 \cdot 2 \cdot 13}$

recommended operating conditions

Supply Voltage V_{CC} . . . . . 5 V

Maximum Fan-Out From Each Output 8

electrical characteristics at $V_{CC} = 5$ V

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 12$ mA, $T_A = 25°C$		0.45	V
			$V_{in} = 2$ V, $I_{sink} = 12$ mA, $T_A = 0°C$		0.45	V
			$V_{in} = 1.8$ V, $I_{sink} = 11.4$ mA, $T_A = 75°C$		0.5	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25°C$	2.6		V
			$V_{in} = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0°C$	2.6		V
			$V_{in} = 0.95$ V, $I_{(load)} = -0.12$ mA, $T_A = 75°C$	2.5		V

electrical characteristics (continued) at $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level input current	4	$V_{in} = 4$ V, $T_A = 25°C$ and $0°C$		5	μA
			$V_{in} = 4$ V, $T_A = 75°C$		10	μA
$I_{in(0)}$	Logical 0 level input current	5	$V_{in} = 0.45$ V, $V_R = 4$ V, $T_A = 25°C$ and $0°C$		−1.4	mA
			$V_{in} = 0.5$ V, $V_R = 4$ V, $T_A = 75°C$		−1.33	mA
$I_{out(1)}$	Output reverse current (off level)	6	$V_{out} = 5$ V, $T_A = 25°C$		100	μA
I_{OS}	Short-circuit output current	7	$V_{out} = 0$, $T_A = 25°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 0°C$		−1.3	mA
			$V_{out} = 0$, $T_A = 75°C$		−1.25	mA
$I_{CC(0)}$	Logical 0 level supply current (all gates)	8	$T_A = 25°C$		12	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (all gates)	9	$V_{CC} = 8$ V, $T_A = 25°C$		12	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$, $C_L = 50$ pF	10	30	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 3.9$ kΩ, $C_L = 30$ pF	25	80	ns

PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862

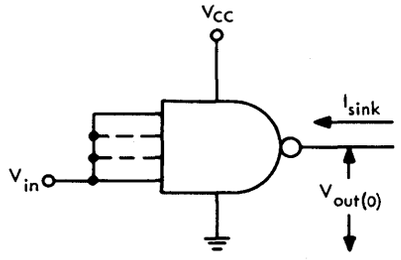
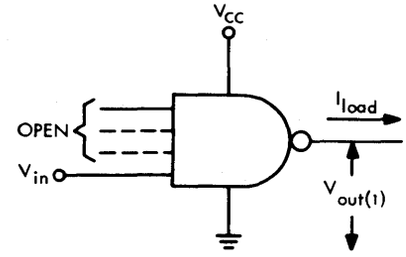


FIGURE 1 — $V_{out(0)}$

SN15 830, SN15 832, SN15 846, and SN15 862



1. Each input is tested separately.

FIGURE 2 — $V_{out(1)}$

SN15 830 and SN15 832

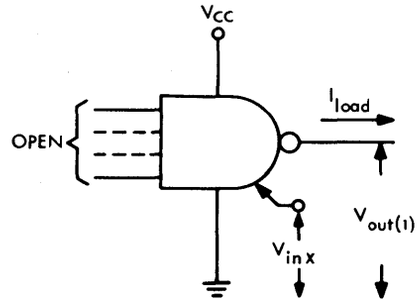
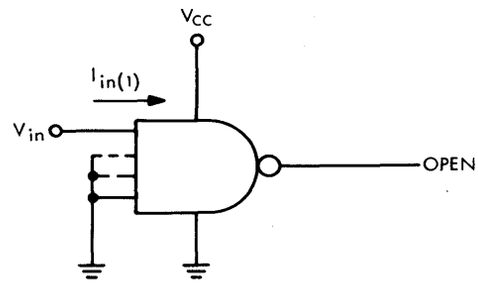


FIGURE 3 — $V_{out(1)}$

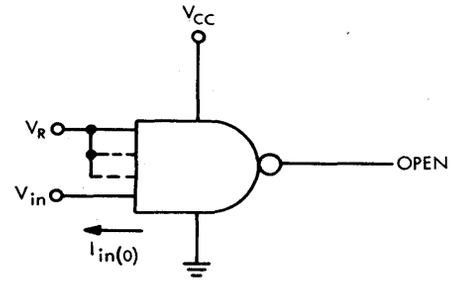
SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862



1. Each input is tested separately.

FIGURE 4 — $I_{in(1)}$

SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862



1. Each input is tested separately.

FIGURE 5 — $I_{in(0)}$

SN15 830, SN15 832, SN15 846, and SN15 862

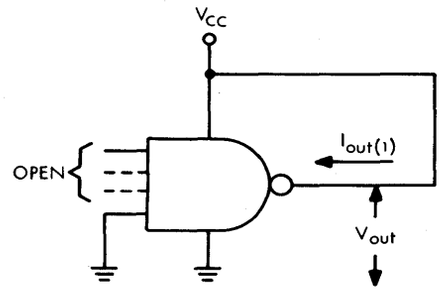


FIGURE 6 — $I_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 830, SN15 832, SN15 846, and SN15 862

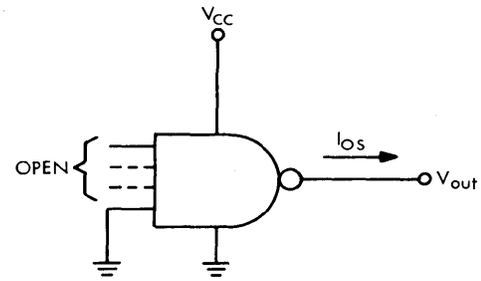


FIGURE 7 — I_{OS}

SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862

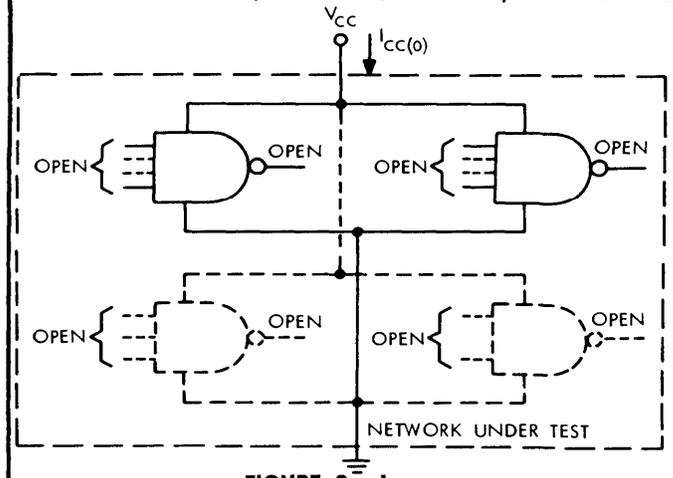


FIGURE 8 — $I_{CC(0)}$

SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862

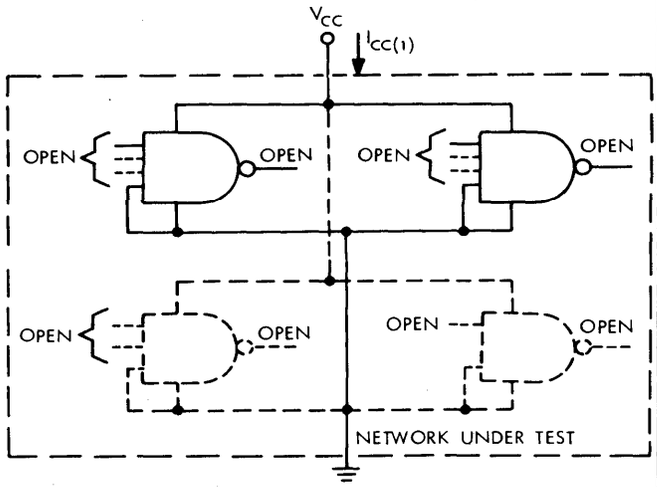
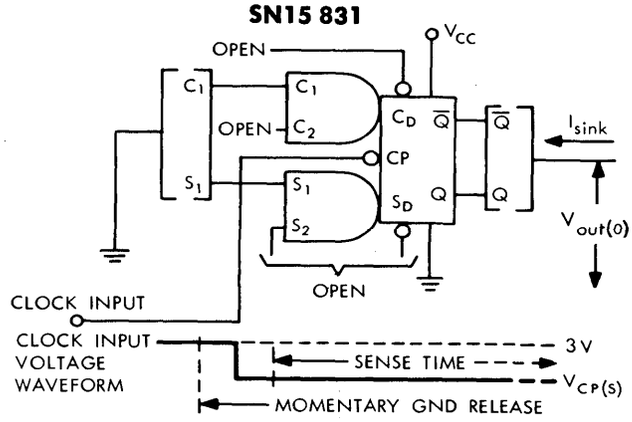


FIGURE 9 — $I_{CC(1)}$

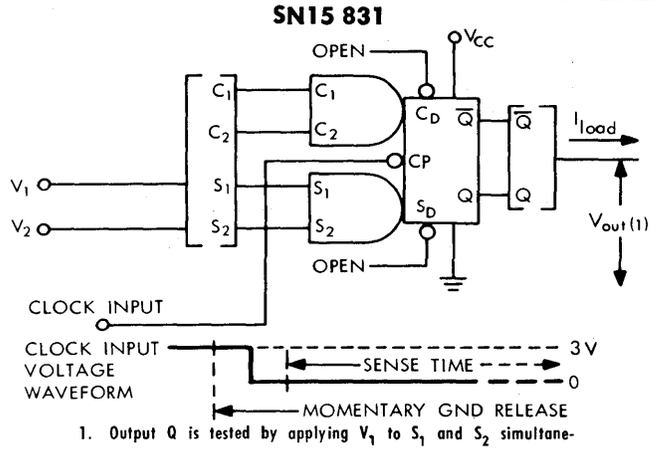
SN15 831



1. Output Q is tested by grounding S_1 and applying a momentary ground to $\overline{Q}$. I_{sink} is driven into Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and applying a momentary ground to Q. I_{sink} is driven into $\overline{Q}$.

FIGURE 10 — $V_{out(0)}$

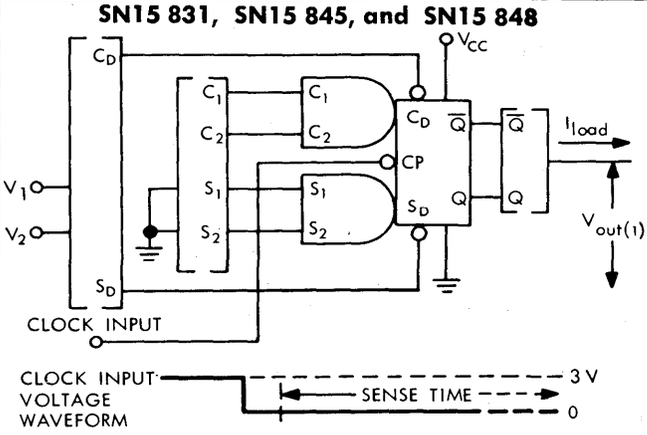
SN15 831



1. Output Q is tested by applying V_1 to S_1 and S_2 simultaneously, applying V_2 to C_1 and C_2 individually, and loading Q.
2. Output $\overline{Q}$ is tested by applying V_1 to C_1 and C_2 simultaneously, applying V_2 to S_1 and S_2 individually, and loading $\overline{Q}$.
3. Momentary ground is applied to output being tested.

FIGURE 11 — $V_{out(1)}$

SN15 831, SN15 845, and SN15 848



1. Output Q is tested by grounding S_1 and S_2, applying V_1 to C_D and V_2 to S_D, and loading Q.
2. Output $\overline{Q}$ is tested by grounding C_1 and C_2, applying V_1 to S_D and V_2 to C_D, and loading $\overline{Q}$.

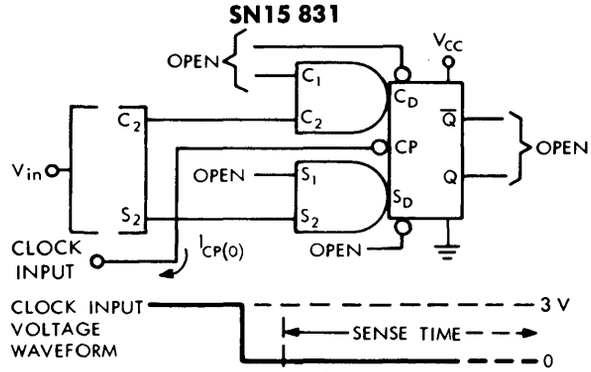
FIGURE 12 — $V_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 831



1. V_{in} is applied to each input separately.

FIGURE 13 — $I_{CP(0)}$

SN15 831

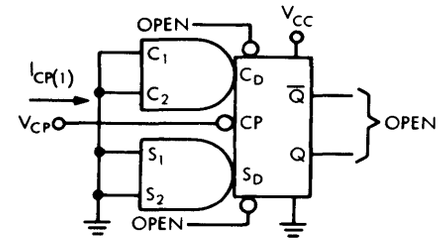
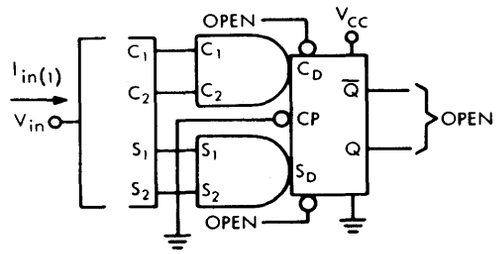


FIGURE 14 — $I_{CP(1)}$

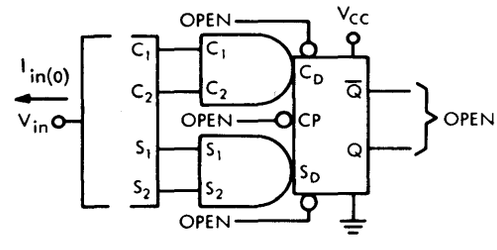
SN15 831, SN15 845 and SN15 848



1. V_{in} is applied to each input separately.

FIGURE 15 — $I_{in(1)}$

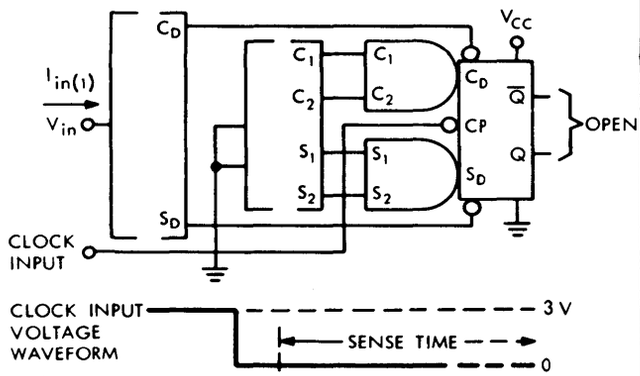
SN15 831



1. V_{in} is applied to each input separately.

FIGURE 16 — $I_{in(0)}$

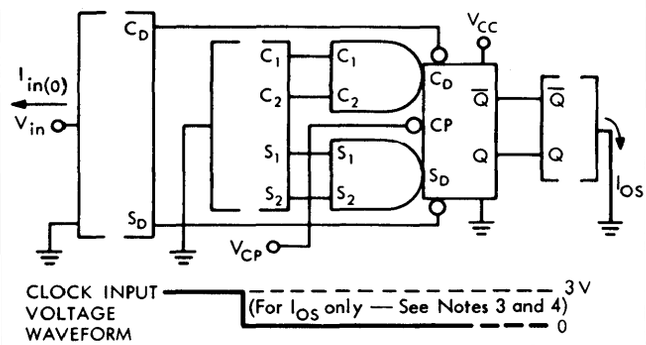
SN15 831



1. C_D input diode is tested by grounding S_1 and S_2 and applying V_{in} to C_D.
2. S_D input diode is tested by grounding C_1 and C_2 and applying V_{in} to S_D.

FIGURE 17 — $I_{in(1)}$

SN15 831 ($I_{in(0)}$) SN15 845 and SN15 848 (I_{OS})



1. Logical 0 level input current at C_D is tested with S_D, S_2, and $\overline{Q}$ grounded and CP open.
2. Logical 0 level input current at S_D is tested with C_D, C_2, and Q grounded and CP open.
3. Short-circuit output current at Q is tested by applying V_{in} to C_D and S_D, grounding C_1 and C_2, and applying clock input.
4. Short-circuit output current at $\overline{Q}$ is tested by applying V_{in} to C_D and S_D, grounding S_1 and S_2, and applying clock input.

FIGURE 18 — $I_{in(0)}$ and I_{OS}

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 831, SN15 845, and SN15 848

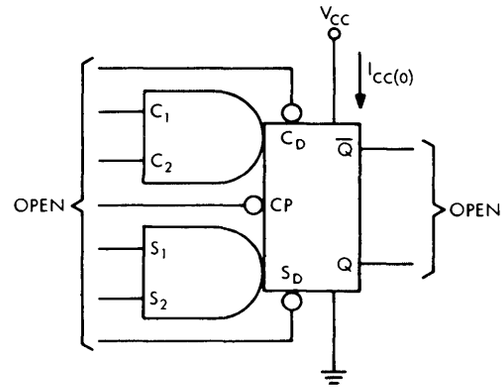


FIGURE 19 — $I_{CC(0)}$

SN15 831, SN15 845, and SN15 848

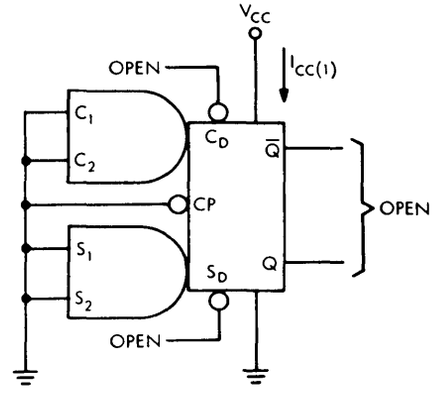
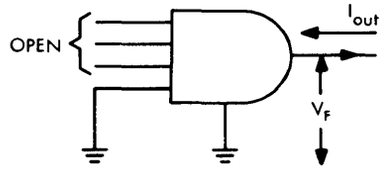


FIGURE 20 — $I_{CC(1)}$

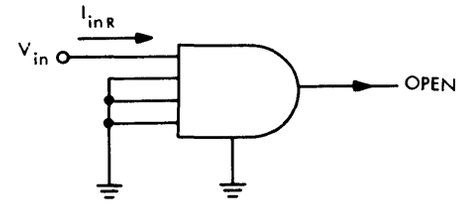
SN15 833



1. Each input is tested separately.

FIGURE 21 — V_F

SN15 833



1. Each input is tested separately.

FIGURE 22 — $I_{in\,R}$

SN15 833

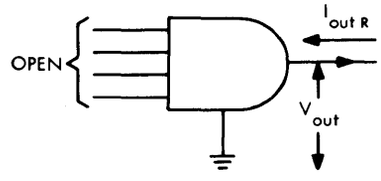


FIGURE 23 — $I_{out\,R}$

SN15 844

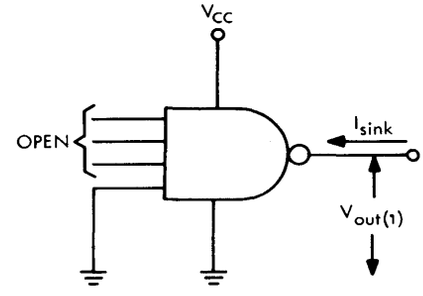


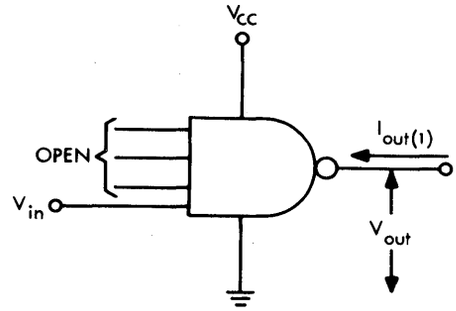
FIGURE 24 — $V_{out(1)}$

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits † (continued)

SN15 844



1. Each input is tested separately.

FIGURE 25 — $I_{out(1)}$

SN15 844

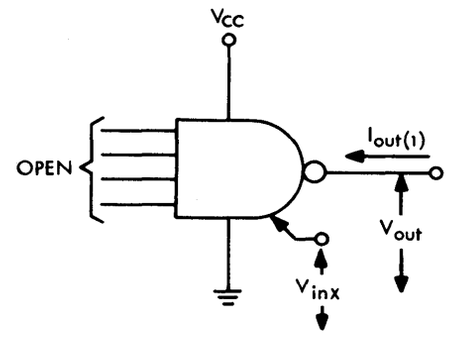
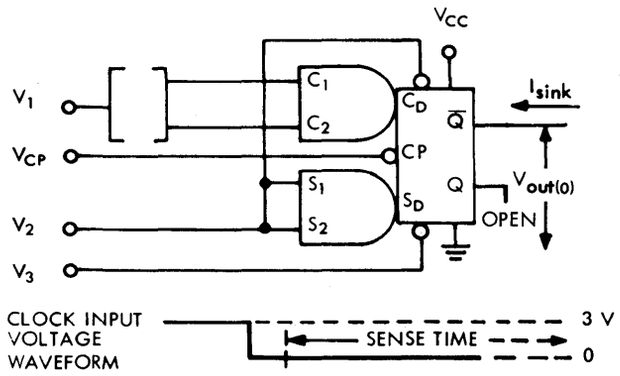


FIGURE 26 — $I_{out(1)}$

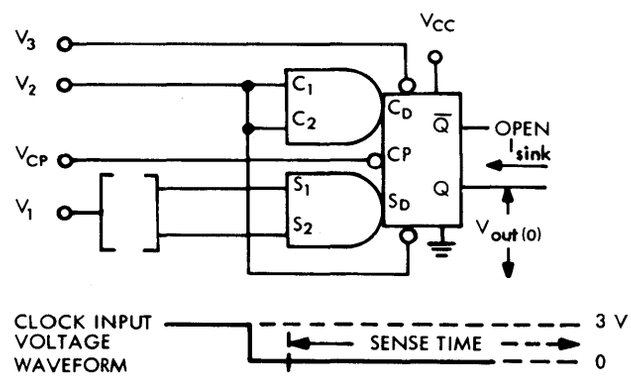
SN15 845 and SN15 848



1. Inputs C_1 and C_2 are tested separately.

FIGURE 27 — $V_{out(0)}$

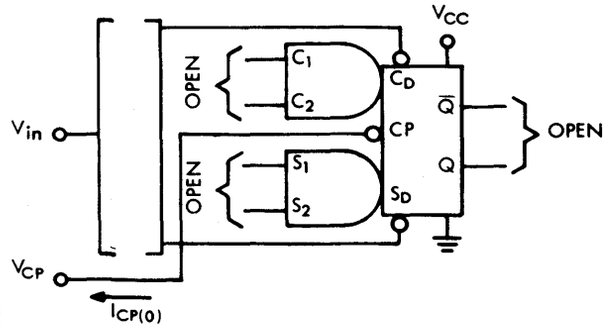
SN15 845 and SN15 848



1. Inputs S_1 and S_2 are tested separately.

FIGURE 28 — $V_{out(0)}$

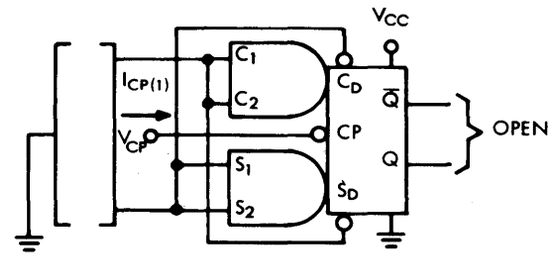
SN15 845 and SN15 848



1. V_{in} is applied to S_D or C_D separately.

FIGURE 29 — $I_{CP(0)}$

SN15 845 and SN15 848



1. Ground is applied separately to C_1,C_2 and S_D or to S_1,S_2 and C_D.

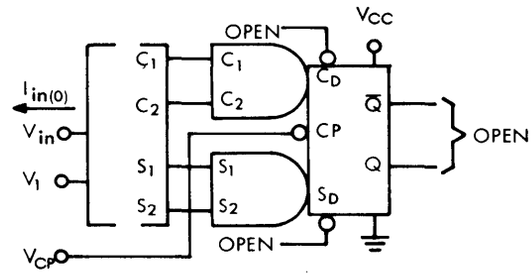
FIGURE 30 — $I_{CP(1)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

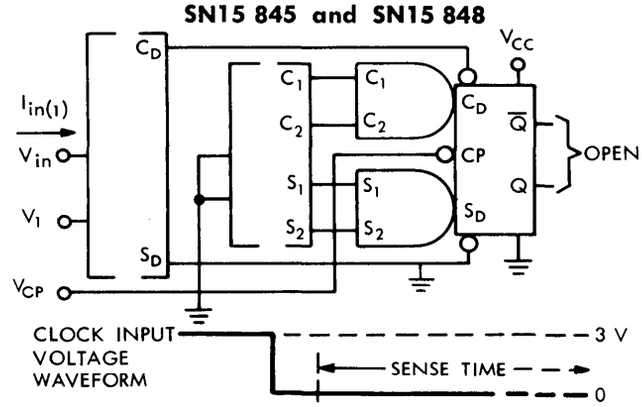
SN15 845 and SN15 848



1. Each synchronous input is tested separately by applying V_{in} to input under test and V_1 to the remaining gate input.

FIGURE 31 — $I_{in(0)}$

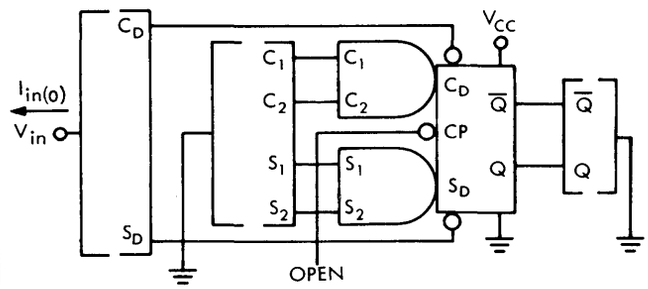
SN15 845 and SN15 848



1. C_D input diode is tested by grounding S_1 and S_2, and by applying V_1 to S_D and V_{in} to C_D.
2. S_D input diode is tested by grounding C_1 and C_2, and by applying V_1 to C_D and V_{in} to S_D.

FIGURE 32 — $I_{in(1)}$

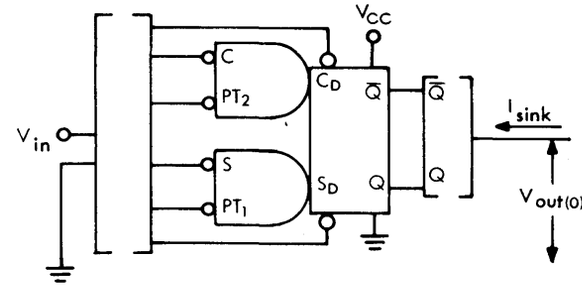
SN15 845 and SN15 848



1. C_D is tested with S_1 and S_2 grounded.
2. S_D is tested with C_1 and C_2 grounded.

FIGURE 33 — $I_{in(0)}$

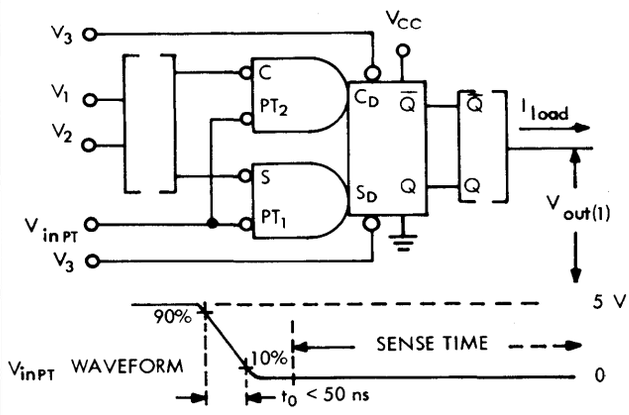
SN15 850



1. Output Q is tested by grounding C and C_D, applying V_{in} to S_D, and loading Q.
2. Output $\overline{Q}$ is tested by grounding S and S_D, applying V_{in} to C_D, and loading $\overline{Q}$.

FIGURE 34 — $V_{out(0)}$

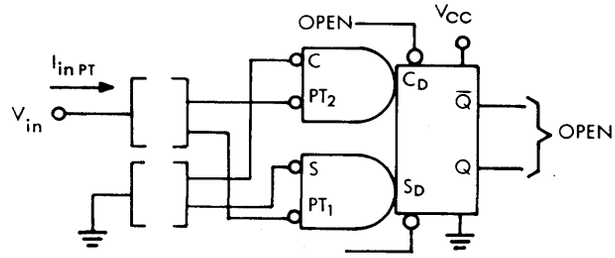
SN15 850



1. Output Q is tested by applying V_1 to C, V_2 to S, V_3 to C_D and S_D, and loading Q.
2. Output $\overline{Q}$ is tested by applying V_1 to S, V_2 to C, V_3 to C_D and S_D, and loading $\overline{Q}$.

FIGURE 35 — $V_{out(1)}$

SN15 850



1. Input PT_1 is tested by grounding S and applying V_{in} to PT_1.
2. Input PT_2 is tested by grounding C and applying V_{in} to PT_2.

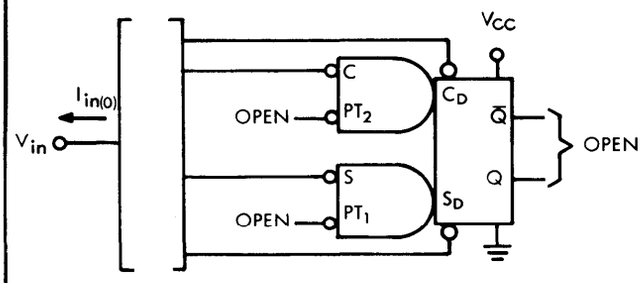
FIGURE 36 — $I_{in\,PT}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

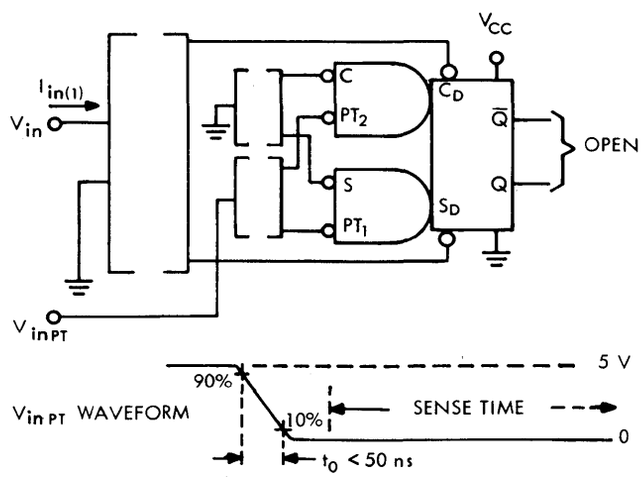
SN15 850



1. Each input is tested separately with all other inputs open-circuited.

FIGURE 37 — $I_{in(0)}$

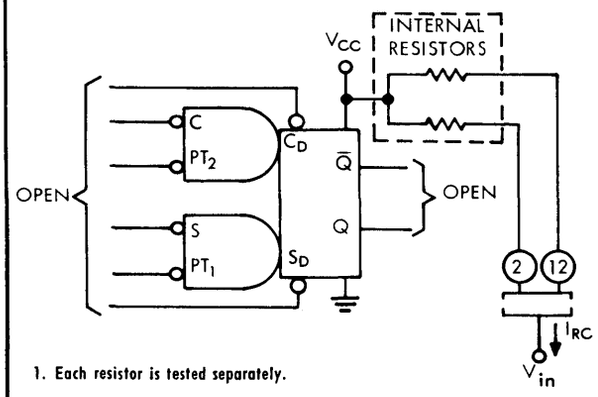
SN15 850



1. Each asynchronous input is tested separately.
2. When testing C_D ground S and apply V_{inPT} to PT_2.
3. When testing S_D ground C and apply V_{inPT} to PT_1.

FIGURE 38 — $I_{in(1)}$

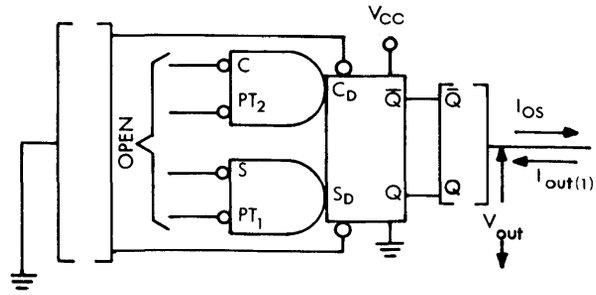
SN15 850



1. Each resistor is tested separately.

FIGURE 39 — I_{RC}

SN15 850



1. When testing output Q ground S_D.
2. When testing output $\overline{Q}$ ground C_D.

FIGURE 40 — I_{OS} and $I_{out(1)}$

SN15 850

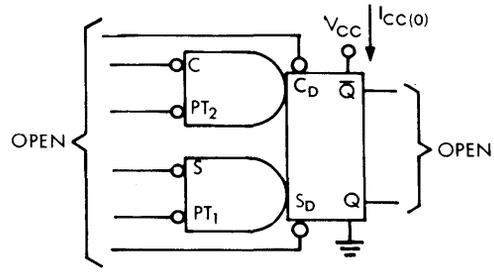


FIGURE 41 — $I_{CC(0)}$

SN15 850

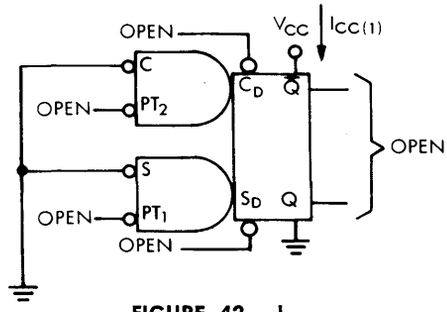


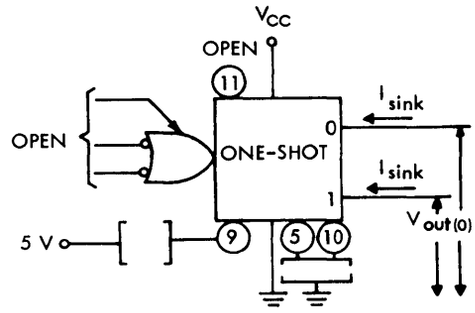
FIGURE 42 — $I_{CC(1)}$

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

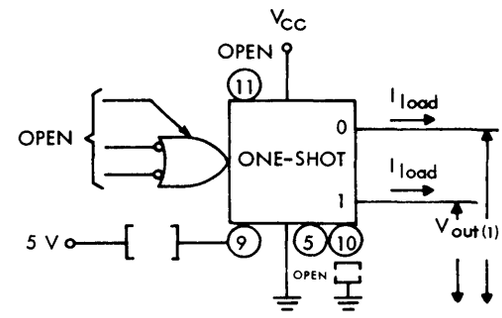
SN15 851



1. Output 0 is tested by applying ground separately to pins (5) and (10) and loading output 0.
2. Output 1 is tested by applying 5 V to pin (9) and loading output 1.

FIGURE 43 — $V_{out(0)}$

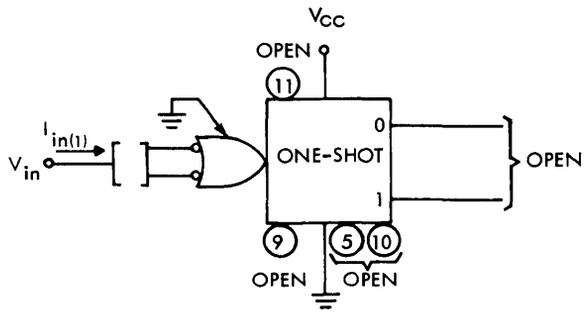
SN15 851



1. Output 0 is tested by applying 5 V to pin (9) and loading output 0.
2. Output 1 is tested by applying ground to pin (10) and loading output 1.

FIGURE 44 — $V_{out(1)}$

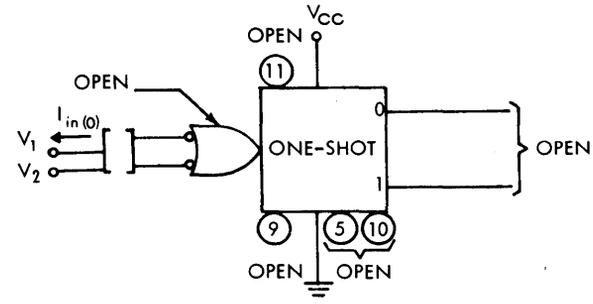
SN15 851



1. Each input is tested separately.

FIGURE 45 — $I_{in(1)}$

SN15 851



1. Each input is tested separately by applying V_2 to input under test and V_1 to the other input.

FIGURE 46 — $I_{in(0)}$

SN15 851

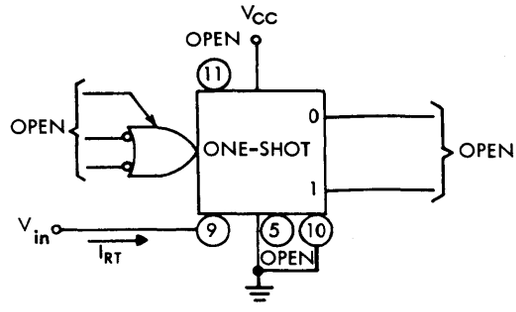


FIGURE 47 — I_{RT}

SN15 851

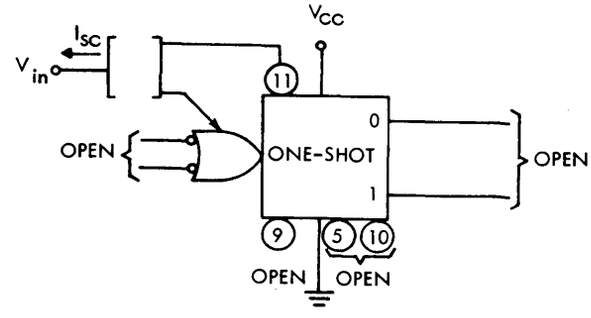


FIGURE 48 — I_{SC}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

SN15 851

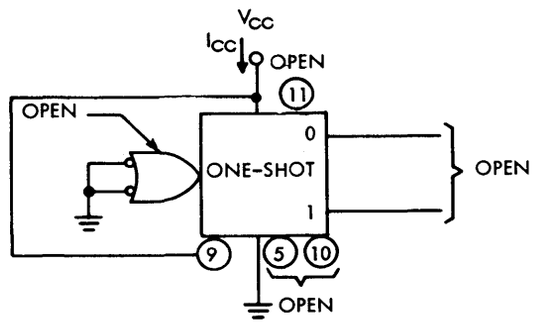


FIGURE 49 — I_{CC}

SN15 851

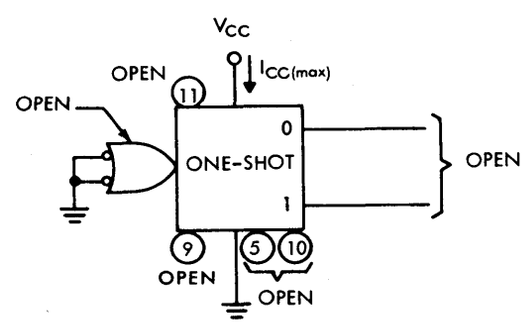
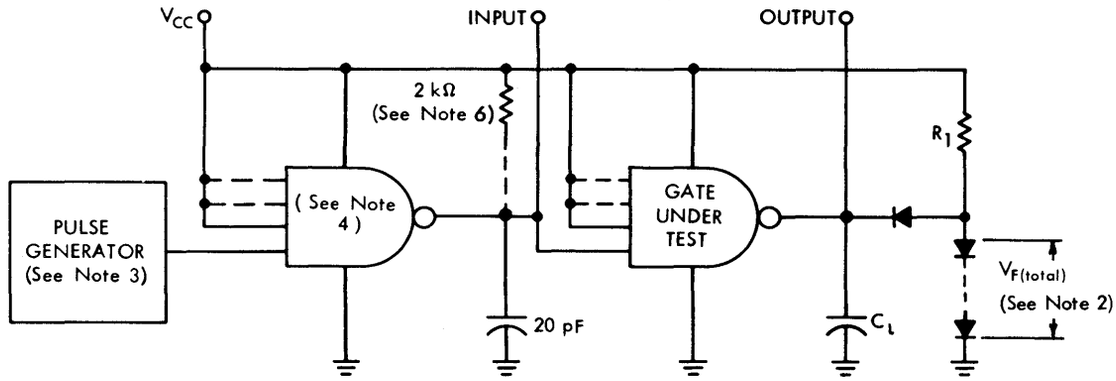


FIGURE 50 — $I_{CC(max)}$

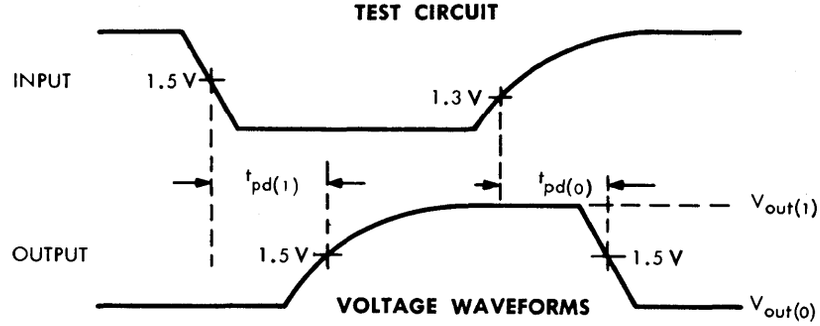
†Arrows indicate actual direction of current flow.

switching characteristics

SN15 830, SN15 832, SN15 844, SN15 846, and SN15 862



TEST CIRCUIT



VOLTAGE WAVEFORMS

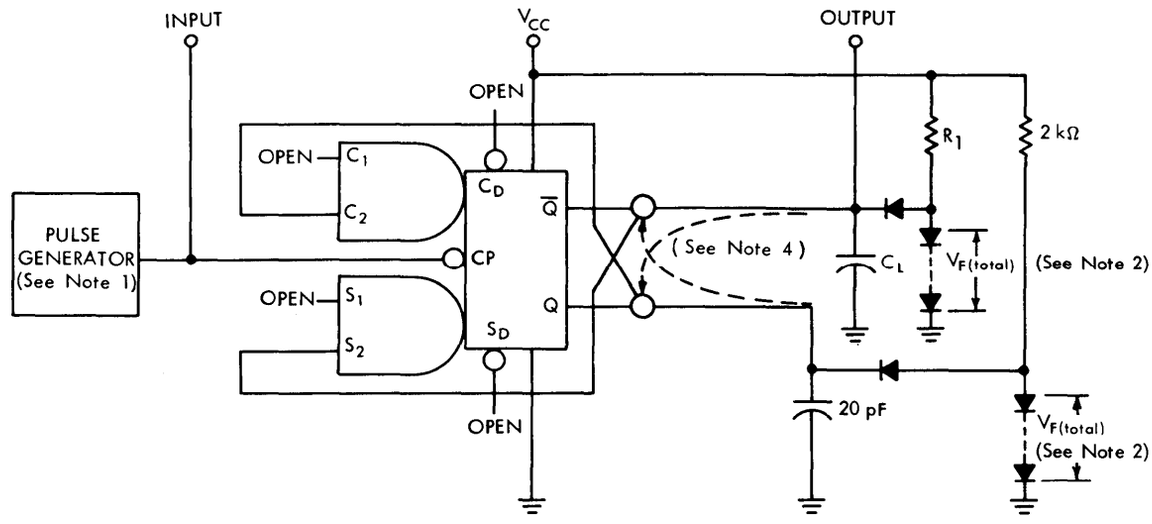
NOTES: 1. Each gate is tested separately.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)} = 1.9$ V to 2.5 V at 2 mA of current.
3. The generator has the following characteristics:
$V_{out} = 3$ V, $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_p = 300$ ns, PRR $= 1$ MHz, $Z_{out} \cong 50\ \Omega$.
4. The driving network is of the same type as the gate under test.
5. Voltage values are with respect to network ground terminal.
6. When testing the SN15 844, connect the 2-kΩ resistor as shown, omit all diodes, and connect resistor R_1 to capacitor C_L and output.

FIGURE 51 — GATE PROPAGATION DELAY

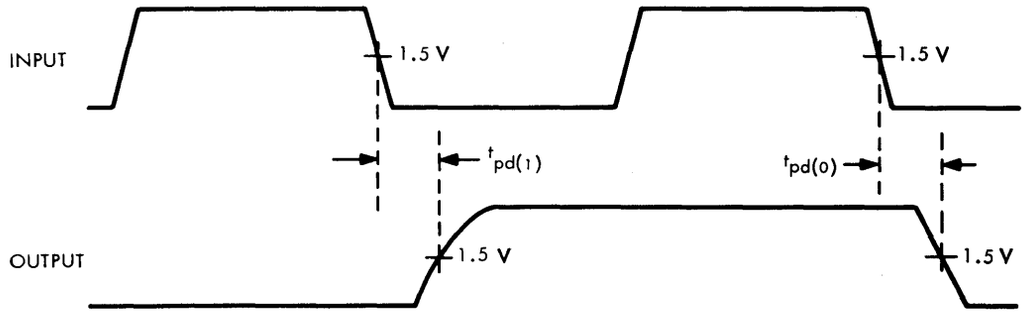
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SN15 831, SN15 845, and SN15 848



TEST CIRCUIT



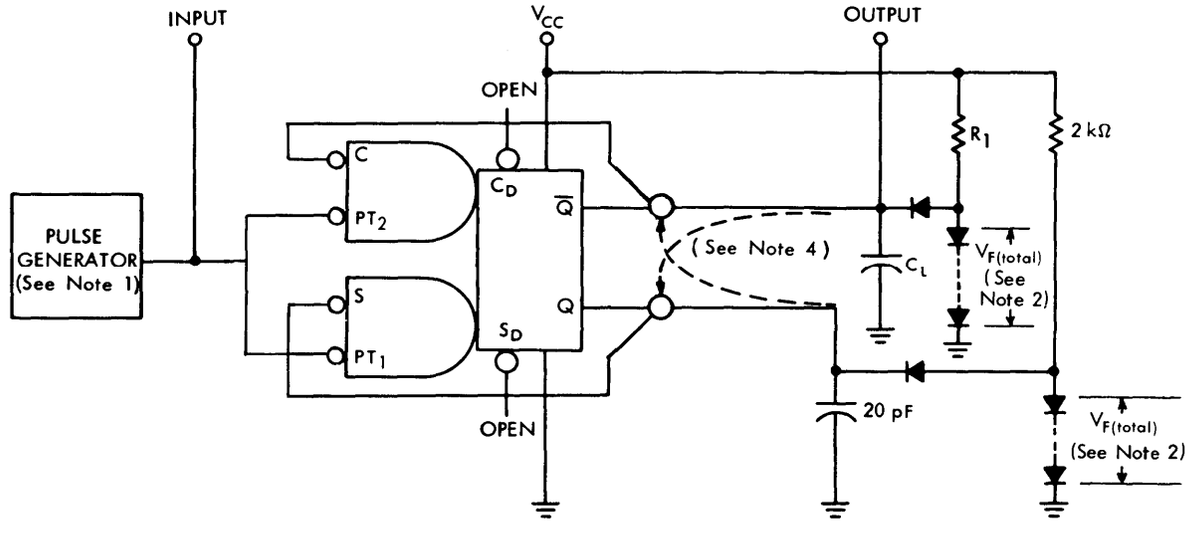
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
$V_{out} = 3$ V, $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_p = 300$ ns, PRR $= 1$ MHz, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)} = 1.9$ V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.
4. Test circuit shows loading when output $\overline{Q}$ is tested. When output Q is tested, loading is interchanged as indicated by the dotted lines.

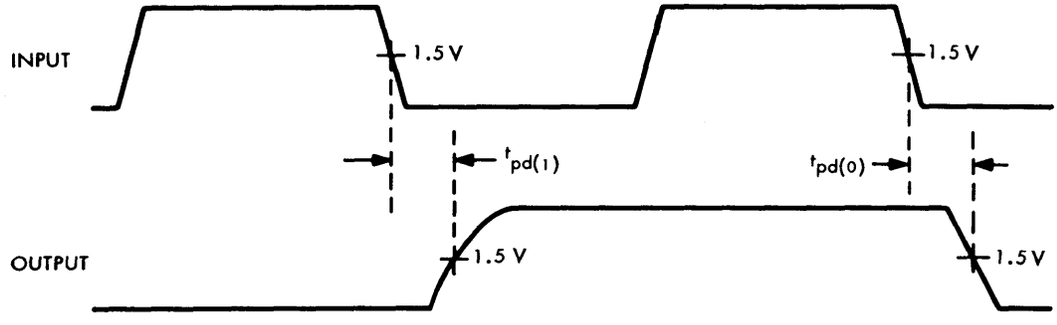
FIGURE 52 — FLIP-FLOP PROPAGATION DELAY

switching characteristics (continued)

SN15 850



TEST CIRCUIT



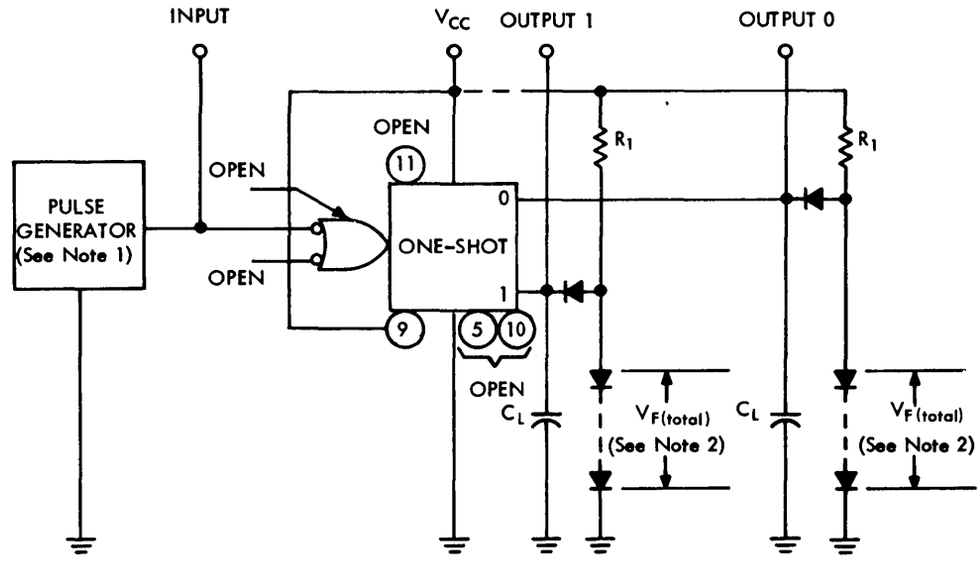
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
$V_{out} = 3$ V, $t_r \leq 15$ ns, $t_f \leq 15$ ns, $t_p = 300$ ns, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)} = 1.9$ V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.
4. Test circuit shows loading when output $\overline{Q}$ is tested. When output Q is tested, loading is interchanged as indicated by the dotted lines.

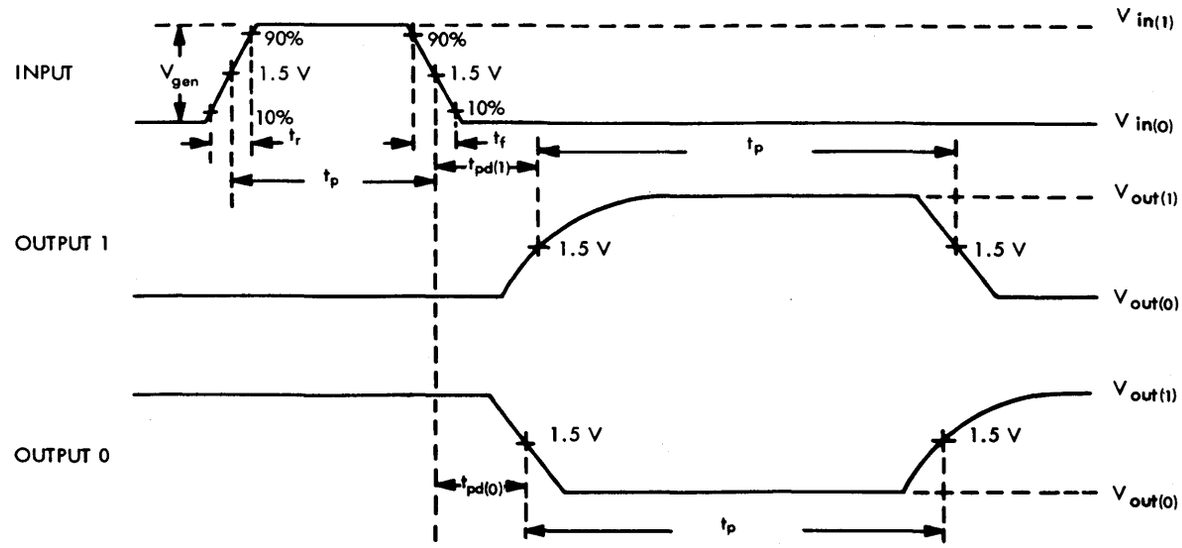
FIGURE 53 — PULSE-TRIGGERED BINARY PROPAGATION DELAY

switching characteristics (continued)

SN15 851



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics:
V_{gen} = 3 V, t_r = 15 ns, t_f = 15 ns, t_p = 300 ns, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.
2. All diodes are 1N916. Use sufficient 1N916 diodes to make $V_{F(total)}$ = 1.9 V to 2.5 V at 2 mA of current.
3. Voltage values are with respect to network ground terminal.

FIGURE 54 — MONOSTABLE MULTIVIBRATOR PROPAGATION DELAY AND PULSE WIDTH

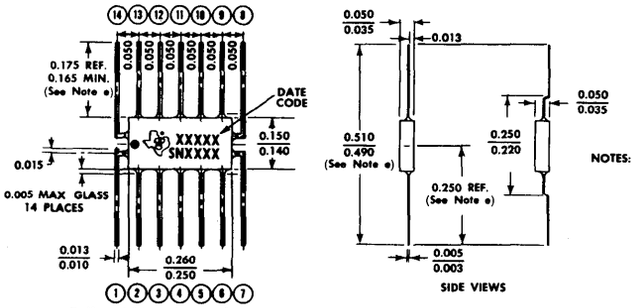
SERIES 15 830
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

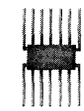
general

SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 15 830 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



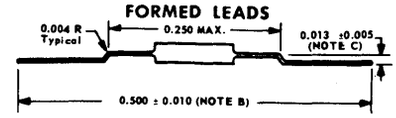
NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. *Symbolization denotes orientation of package.*



leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.

FORMED LEADS



NOTES: a. All dimensions in inches.
b. Not applicable in Mech-Pak Carrier.
c. Measured from center of lead to bottom of package where lead emerges from body.

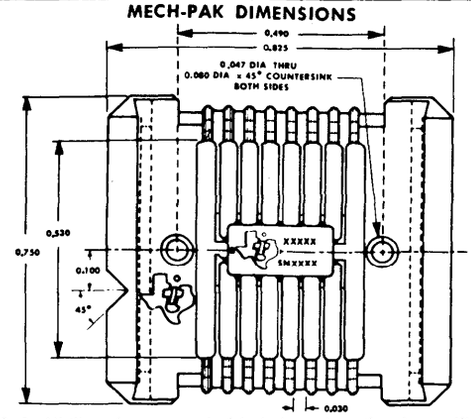
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

SERIES 15 830N
BULLETIN NO. DL-S 668942, NOVEMBER, 1966

DIODE-TRANSISTOR-LOGIC SEMICONDUCTOR NETWORKS IN MOLDED PLUG-IN PACKAGES

description

Series 15 830N consists of the Series 15 830 general-purpose DTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 75°C.

features

LOW SYSTEM COST
- **multifunction gates offering low cost per logic function**
- **electrically designed specifically for monolithic integrated-circuit technology**
- **plug-in configuration ideal for flow-soldering techniques**
- **pins on 100-mil grid spacings for industrial-type circuit-boards**

PERFORMANCE
- **high speed**
- **high d-c noise margins**
- **low power dissipation**
- **good fan-out capability**

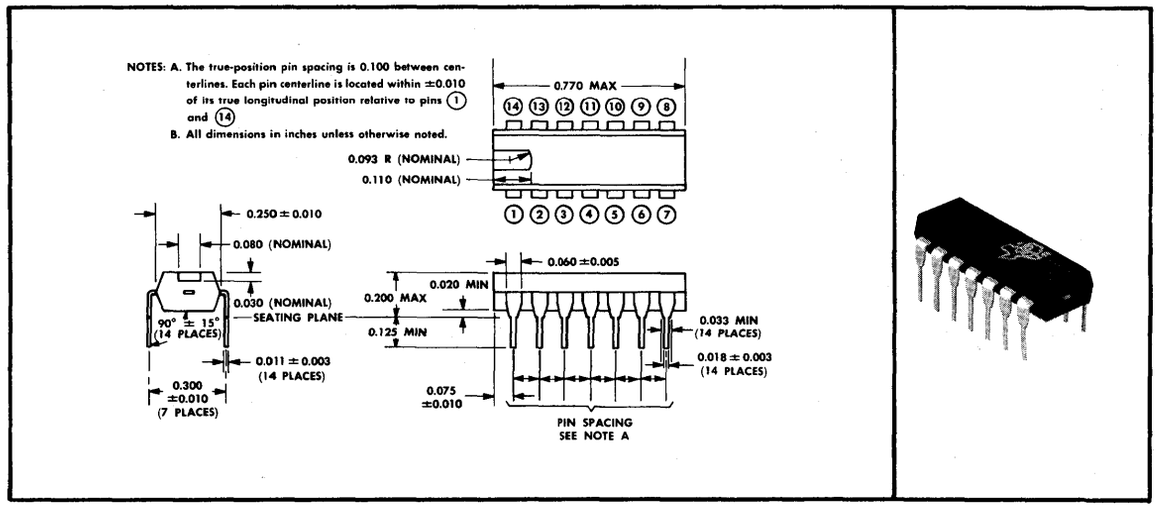
EASE OF DESIGN
- **familiar logic configuration (DTL)**
- **single-ended output — dot-OR logic**
- **complete family for design flexibility**
- **single power supply**

specifications, logic symbols and terminal designations

Schematic diagrams, fan-out rules, maximum ratings, and electrical characteristics for Series 15 830N networks are identical to those of the corresponding Series 15 830 type numbers except for maximum propagation delay times‡. Terminal designations for the Series 15 830N networks are shown in this data sheet.

mechanical data

Series 15 830N networks are mounted on a 14-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions.

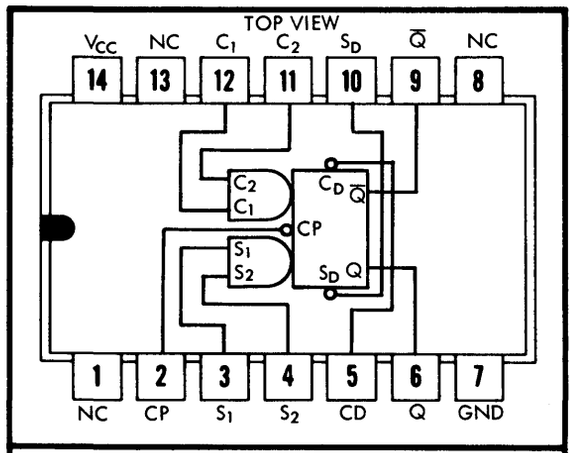


†Patented by Texas Instruments

‡Maximum t_{pd1} and t_{pd0} for Series 15 830N are 5 ns higher than for Series 15 830. The increase in the typical or median value is negligible.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN15 831N, SN15 845N, SN15 848N
MASTER-SLAVE FLIP-FLOPS



positive logic

Low input to S_D sets Q to logical 1

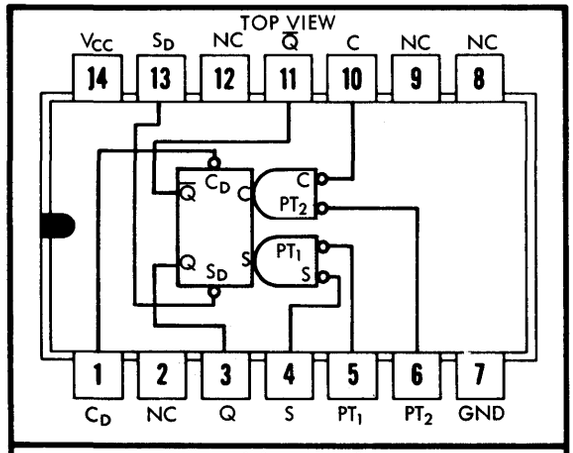
TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$, and C_2 to Q.

SN15 850N
PULSE-TRIGGERED BINARY



positive logic

See asynchronous truth table

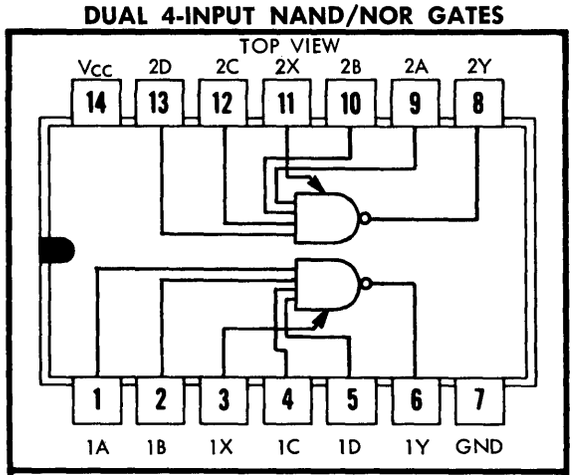
TRUTH TABLES

SYNCHRONOUS					
t_n PULSE INPUT				t_{n+1} OUTPUT	
S	C	PT_1	PT_2	Q	$\overline{Q}$
1	X	X	1	Qn	$\overline{Qn}$
X	1	1	X	Qn	$\overline{Qn}$
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S_D	C_D	Q	$\overline{Q}$
1	1	Qn	$\overline{Qn}$
0	1	0	1
1	0	1	0
0	0	1	1

NOTES:
1. X indicates that either a logical 1 or a logical 0 may be present.
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT_1 and PT_2 indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.

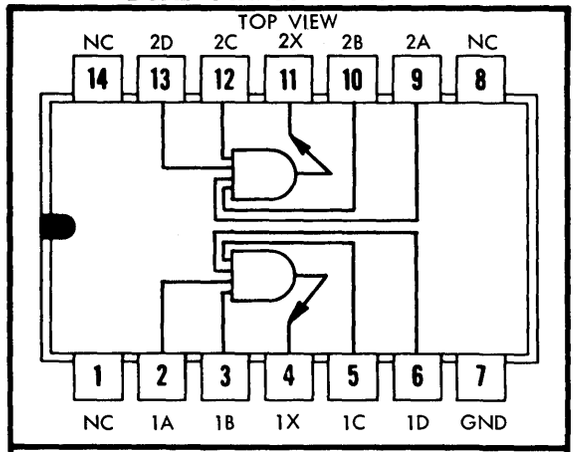
SN15 830N, SN15 832N (BUFFER), SN15 844N (POWER)
DUAL 4-INPUT NAND/NOR GATES



positive logic

$Y = \overline{ABCD}$

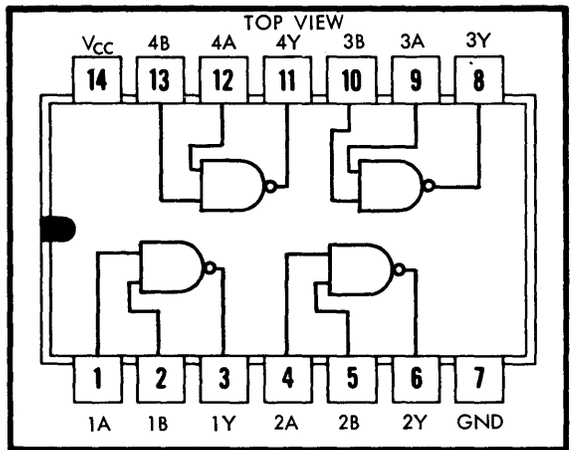
SN15 833N
DUAL 4-INPUT EXPANDER



positive logic

$X = ABCD$

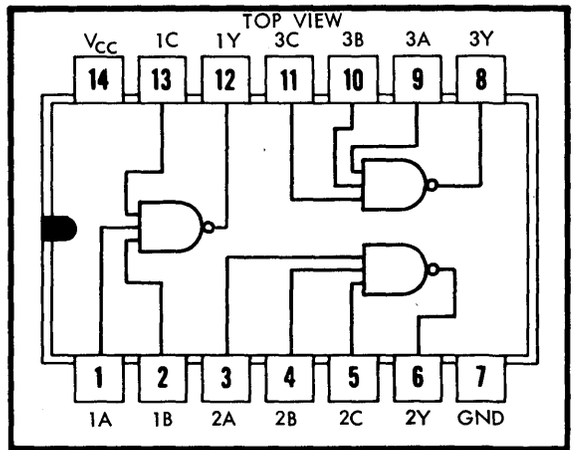
SN15 846N
QUADRUPLE 2-INPUT NAND/NOR GATE



positive logic

$Y = \overline{AB}$

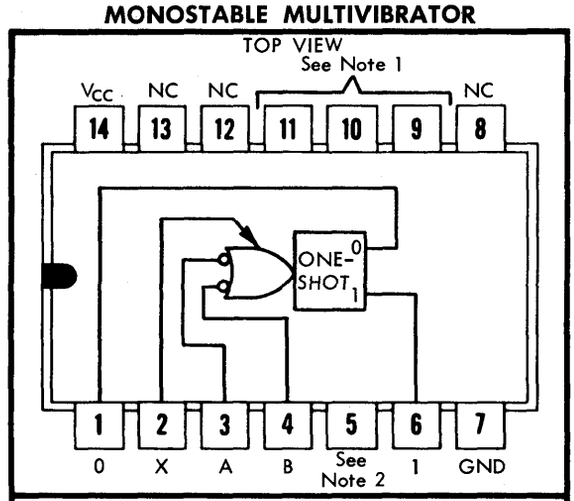
SN15 862N
TRIPLE 3-INPUT NAND/NOR GATE



positive logic

$Y = \overline{ABC}$

SN15 85IN
MONOSTABLE MULTIVIBRATOR



NOTES: 1. Refer to the schematic diagram for using pins ⑨, ⑩, and ⑪ to control one-shot pulse width.
2. Input sensitivity can be decreased by adding a capacitor from pin ⑤ to ground.

PRINTED IN U.S.A.

TYPE SN723 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN723
BULLETIN NO. DL-S 668493, MARCH 1966

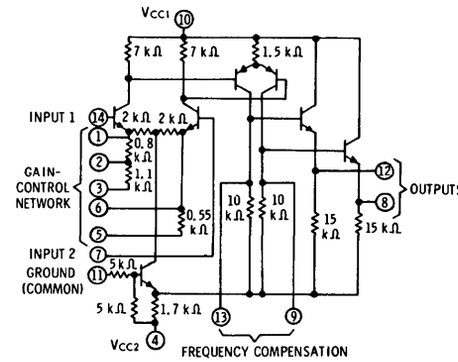
SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

description

The SN723, offering differential inputs and differential emitter-follower outputs, incorporates a resistance network in the emitters of the input stage to facilitate gain adjustment. From the wide range of total resistance available, a particular value may be selected by connecting the resistor-network pins in a configuration which produces the desired gain. Maximum-gain configuration is with pin ① shorted to pin ⑥.

The SN723, one of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

SCHEMATIC DIAGRAM

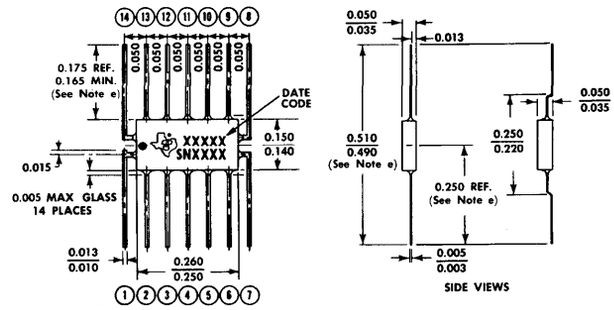
mechanical data

The SN723 is mounted in a glass-to-metal hermetically sealed welded package meeting TO-84. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN723 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

ORDERING INSTRUCTIONS

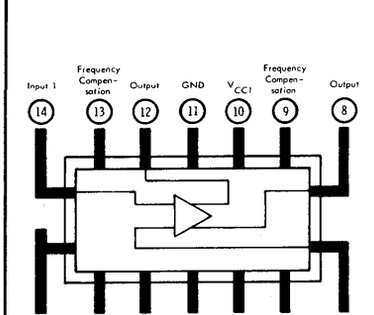
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

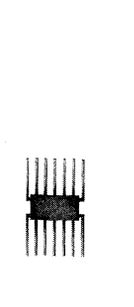
OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



Falls within TO-84 dimensions

NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.





†Patented by Texas Instruments.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 24% nickel, and 17% cobalt.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE SN723
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . ±6 V
Input Voltage (Either Input, See Note 1) . . . . . ±10 V
Duration of Short-Circuit Output Current . . . . . 5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . . 300 mW
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. Derate linearly to 220 mW at 70°C free-air temperature at the rate of 1.8 mW/deg.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			4	15	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = 0°C to 70°C		10		μV/deg
V_{CMO}	Common-mode output offset voltage			600		mV
I_{in}	Input current			6.5		μA
I_{DI}	Differential-input offset current			1	4	μA
V_{OM}	Maximum peak-to-peak output voltage	Differential output, f = 1 kc/s		20		V
		Differential output, f = 1 kc/s, T_A = 0°C to 70°C	15			V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_{VD}	Differential voltage gain	f = 1 kc/s		3000		
		f = 1 kc/s, T_A = 0°C to 70°C	1250			
		f = 1 kc/s, pins ① and ⑧ open		120		
		f = 1 kc/s, pin ① shorted to pin ⑤, pin ⑧ open		800		
		f = 1 kc/s, pin ② shorted to pin ⑤, pins ① and ⑧ open		440		
		f = 1 kc/s, pin ③ shorted to pin ⑤, pins ① and ⑥ open		300		
		f = 1 kc/s, pin ② shorted to pin ⑥, pin ① open		620		
CMRR	Common-mode rejection ratio	f = 1 kc/s		80		dB
BW	Bandwidth (−3 dB)		60	150		kc/s
Z_{in}	Input impedance	f = 1 kc/s	4	10		kΩ
Z_{out}	Output impedance	f = 1 kc/s		250		Ω
P_T	Total power dissipation			100		mW

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading; pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑧ and ⑬ open.

letter symbol and parameter definitions

V_{DI} — That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

V_{CMO} — That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} — The current into either input of the amplifier.

I_{DI} — The difference in the currents into the two input terminals when the output is balanced.

V_{OM} — The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} — The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR — The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW — The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

Z_{in} — The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} — The impedance between the output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS§

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

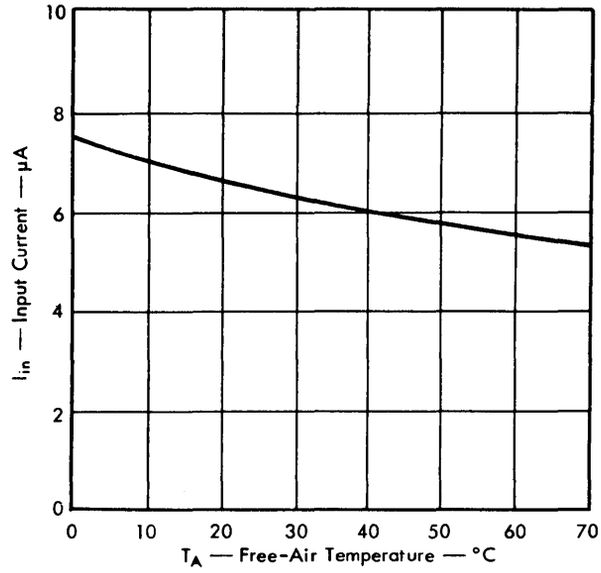


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

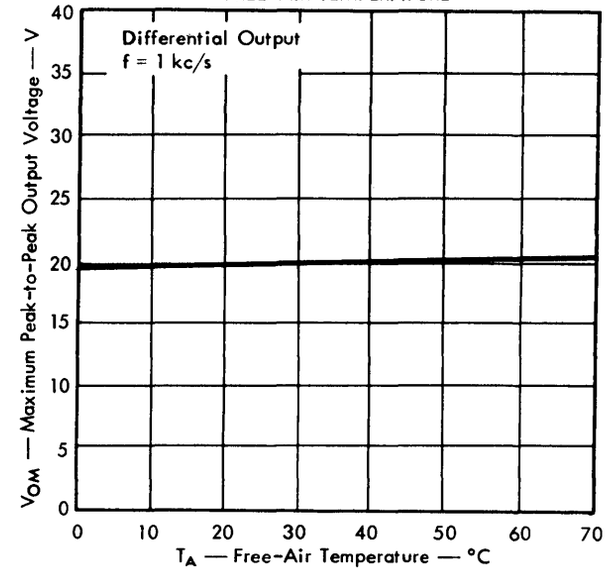


FIGURE 2

SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

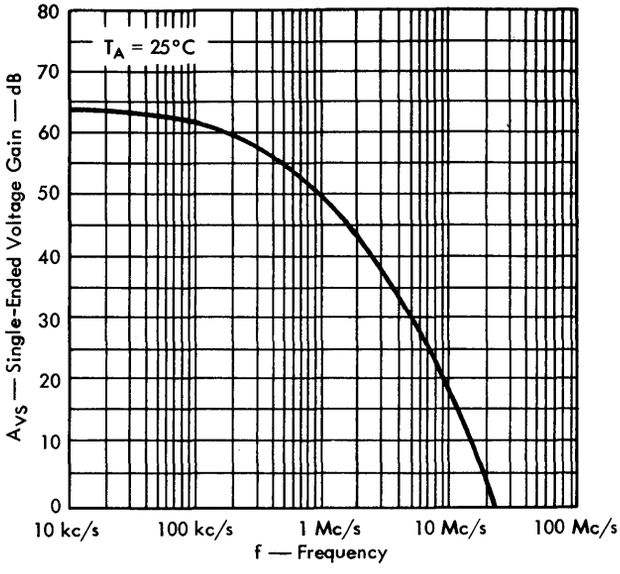


FIGURE 3

DIFFERENTIAL VOLTAGE GAIN
vs
SUPPLY VOLTAGE

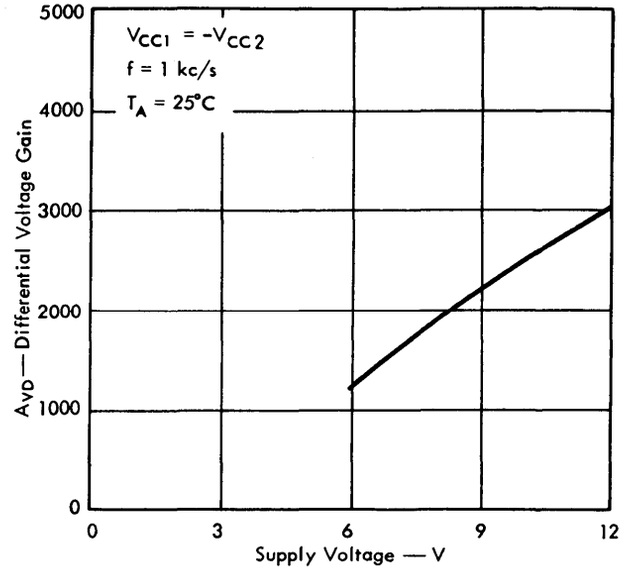


FIGURE 4

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading; pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

TYPICAL CHARACTERISTICS§

DIFFERENTIAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

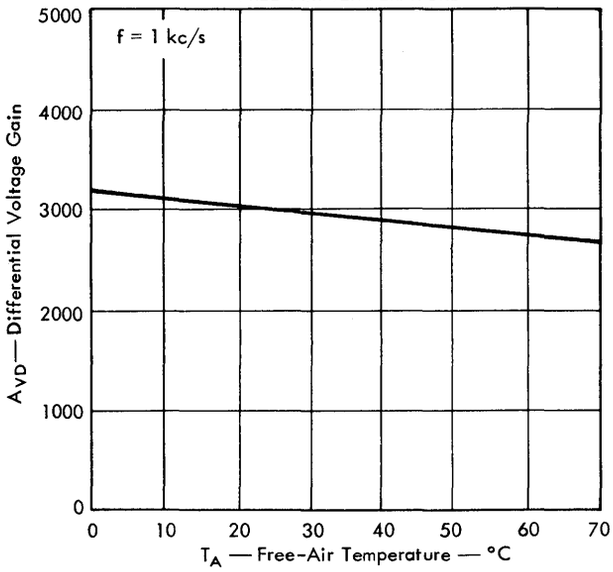


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

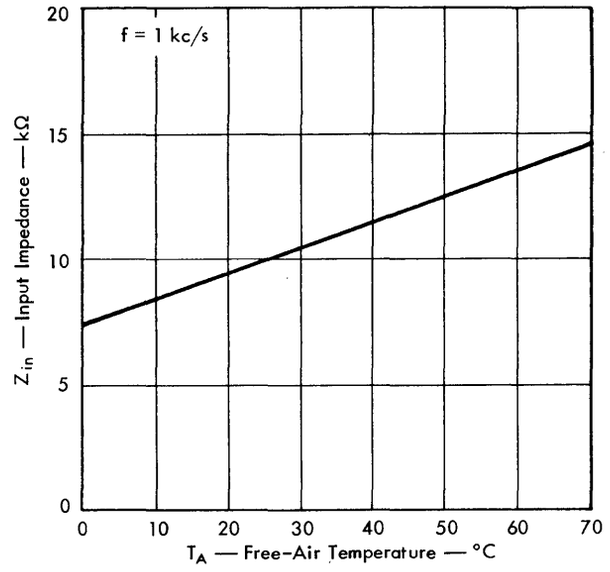


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

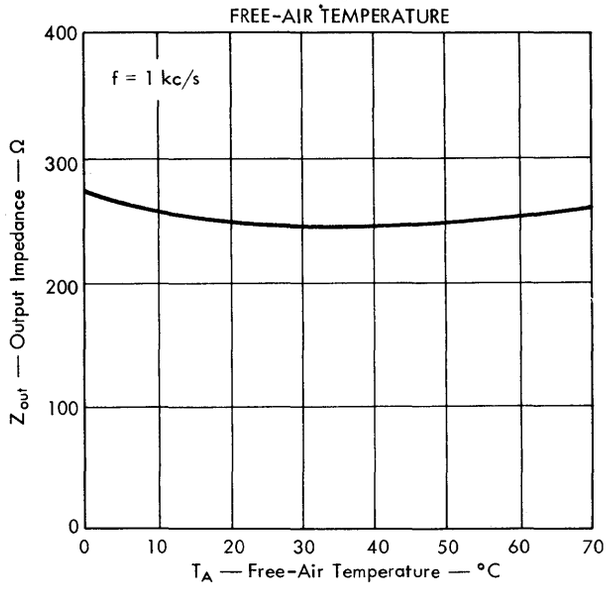


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

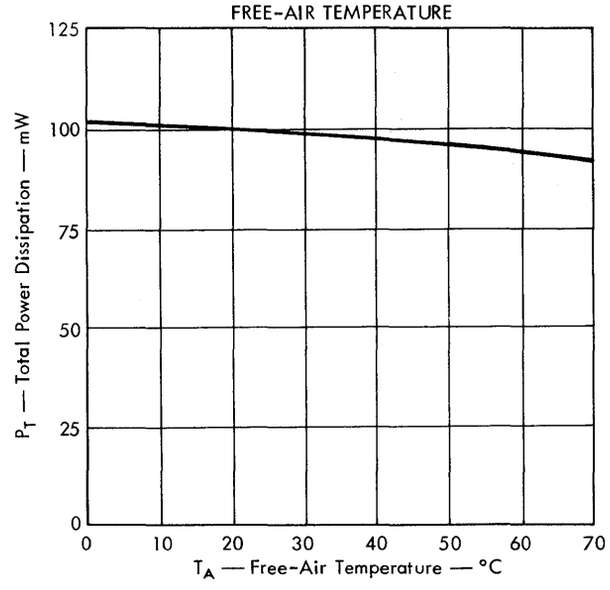


FIGURE 8

§Unless otherwise noted, test conditions are:

V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

PRINTED IN U.S.A.

TYPE SN7231L
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN7231L
BULLETIN NO. DL-S 668829, AUGUST 1966

SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER
for application as

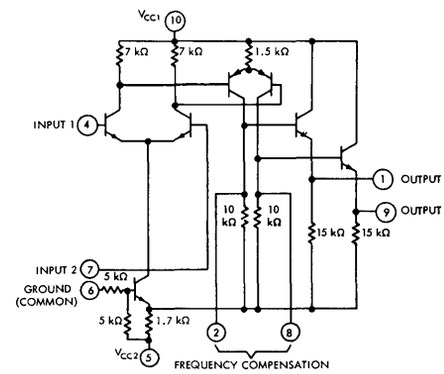
- **Comparator**
- **Level Detector**
- **Differential Amplifier**
- **Voltage Regulator**

- **Military & Industrial Control Systems**
- **Analog-to-Digital Converters**
- **Analog Computers**

description

The SN7231L offers differential inputs and differential emitter-follower outputs. Two stages of differential amplification are used to provide high gain at frequencies up to 1 MHz. A high degree of component matching, which assures stable operation over the temperature range of 0°C to 70°C, is achieved by the monolithic construction.

The SN7231L, one of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.

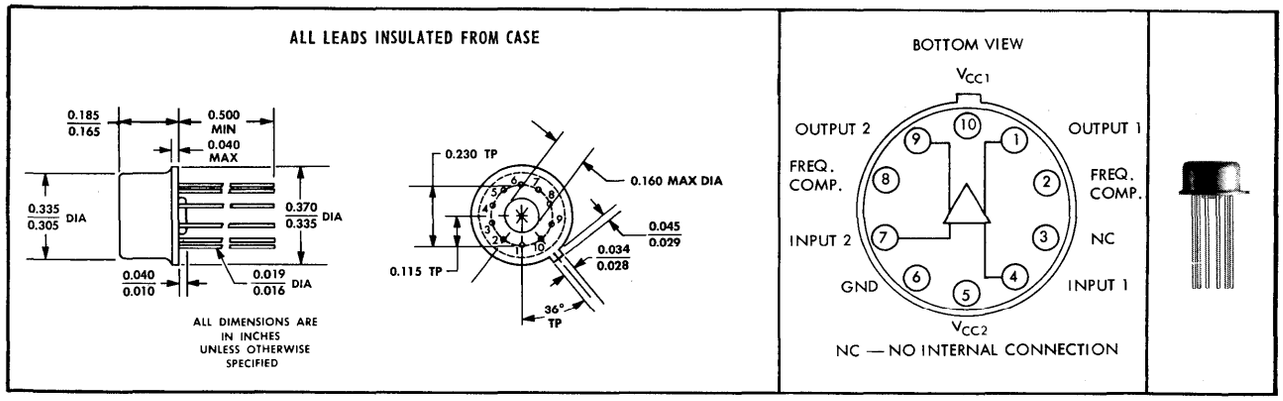


NOTE: Component values shown are nominal.

SCHEMATIC DIAGRAM

mechanical data

The SN7231L package outline is same as JEDEC TO-100 except for diameter of standoff.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1}	+15 V
V_{CC2}	−15 V
Differential Input Voltage	±6 V
Input Voltage (Either Input, See Note 1)	±10 V
Duration of Short-Circuit Output Current	5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	300 mW
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.

2. Derate linearly to 220 mW at 70°C free-air temperature at the rate of 1.8 mW/deg.

†Patented by Texas Instruments

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			4	15	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	$T_{A(1)} = 70°C$, $T_{A(2)} = 0°C$		10		μV/deg
V_{CMO}	Common-mode output offset voltage			600		mV
I_{in}	Input current			6.5		μA
I_{DI}	Differential-input offset current			1	4	μA
V_{OM}	Maximum peak-to-peak output voltage	Differential output, f = 1 kHz		20		V
		Differential output, f = 1 kHz, $T_A = 0°C$ to 70°C	15			V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_{VD}	Differential voltage gain	$R_S = 50\ \Omega$, f = 1 kHz		3000		
		$R_S = 50\ \Omega$, f = 1 kHz, $T_A = 0°C$ to 70°C	1250			
CMRR	Common-mode rejection ratio	$R_S = 50\ \Omega$, f = 1 kHz		80		dB
BW	Bandwidth (–3 dB)		60	150		kHz
Z_{in}	Input impedance	f = 1 kHz	4	1		kΩ
Z_{out}	Output impedance	f = 1 kHz		250		Ω
P_T	Total power dissipation			100		mW

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin (6) grounded.

letter symbol and parameter definitions

V_{DI} That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.

α_{VDI} Temperature coefficient averaged over the specified temperature range and defined by the equation:

$$\alpha_{VDI} = \frac{(V_{DI} @ T_{A(1)}) - (V_{DI} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}$$

V_{CMO} That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.

I_{in} The current into either input of the amplifier.

I_{DI} The difference in the currents into the two input terminals when the output is balanced.

V_{OM} The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR The ratio of the differential-mode voltage gain to the commmon-mode voltage gain.

BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

Z_{in} The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} The impedance between either output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS§

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

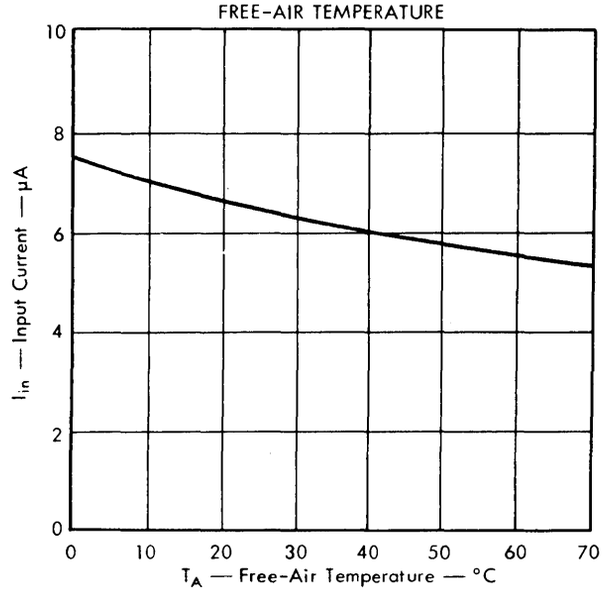


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

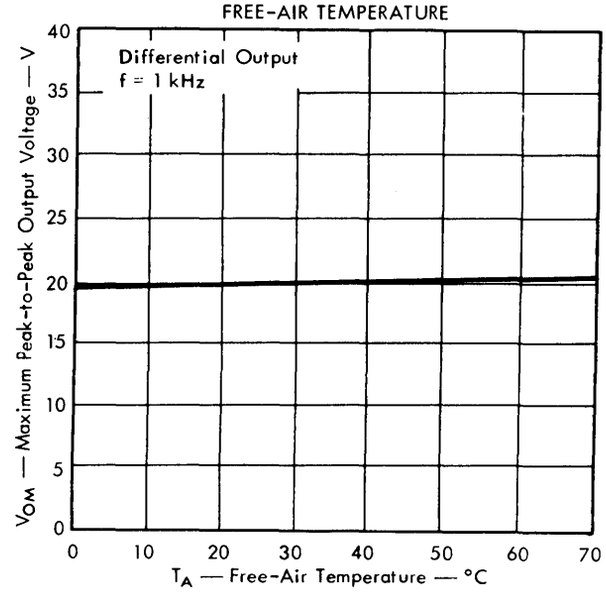


FIGURE 2

SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

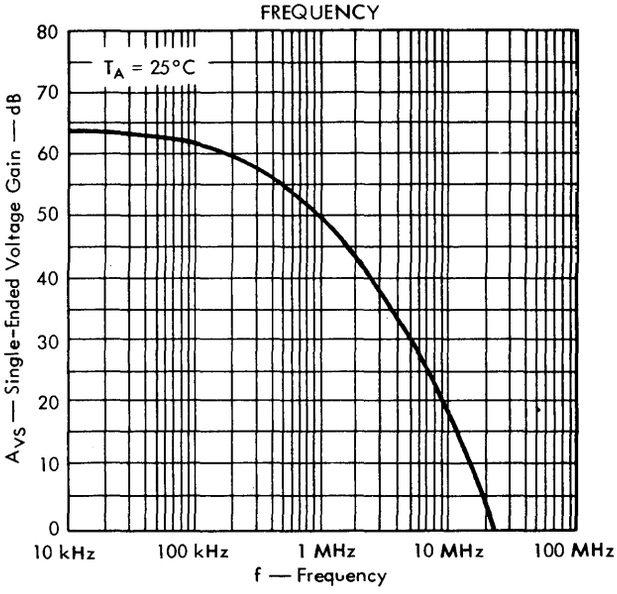


FIGURE 3

DIFFERENTIAL VOLTAGE GAIN
vs
SUPPLY VOLTAGE

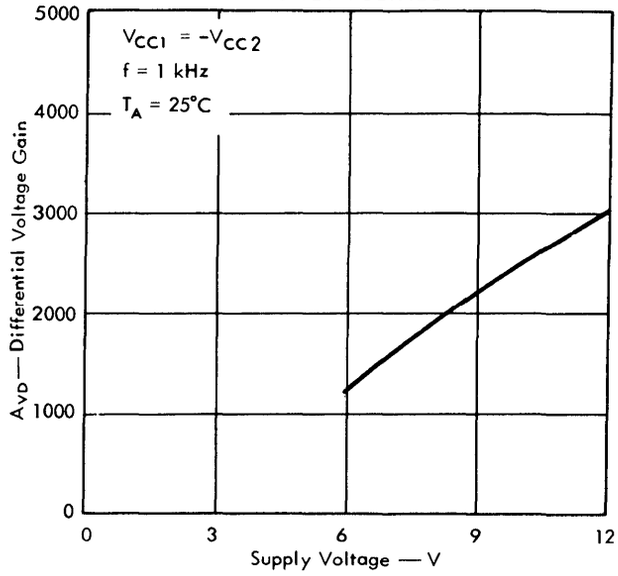


FIGURE 4

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin ⑥ grounded.

TYPICAL CHARACTERISTICS §

DIFFERENTIAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

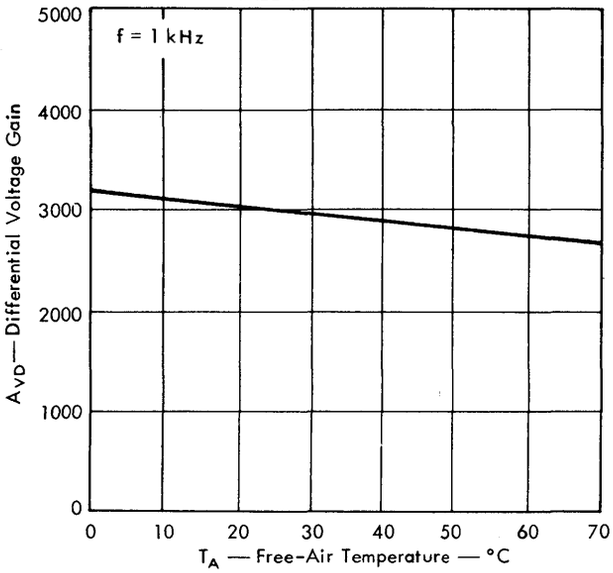


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

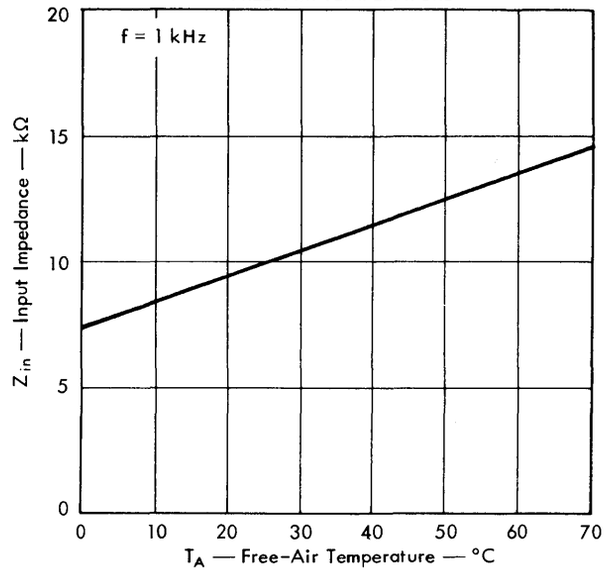


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

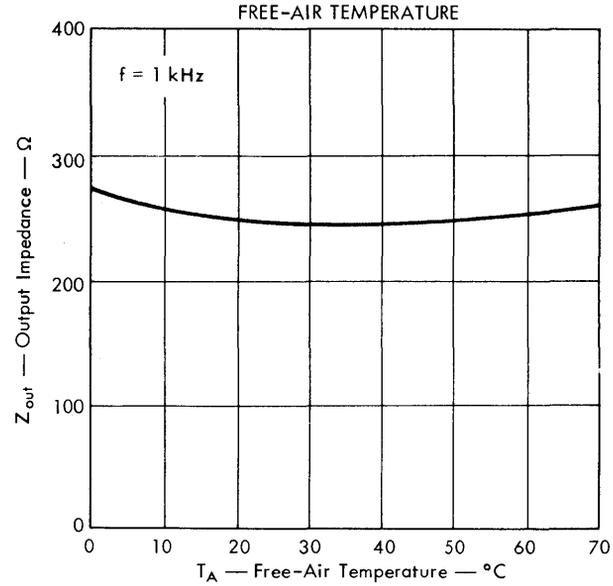


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

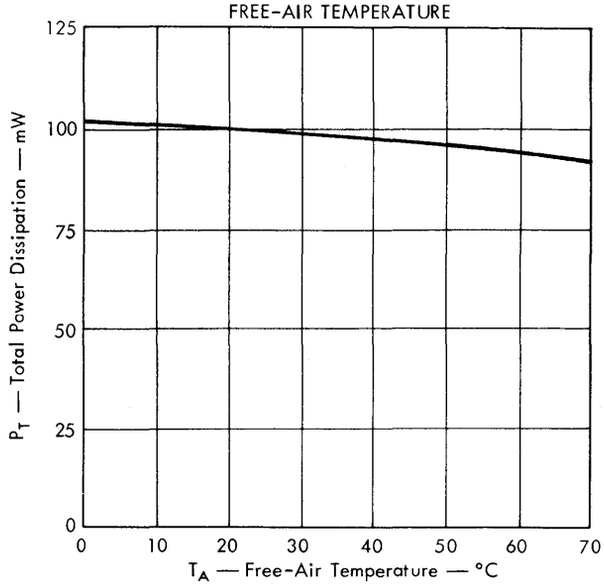


FIGURE 8

§Unless otherwise noted, test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, V_{DI} applied, no external loading and pin ⑥ grounded.

PRINTED IN U.S.A.

TYPES SN724, SN724L
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

TYPES SN724, SN724L
BULLETIN NO. DL-S 668376, MARCH 1966

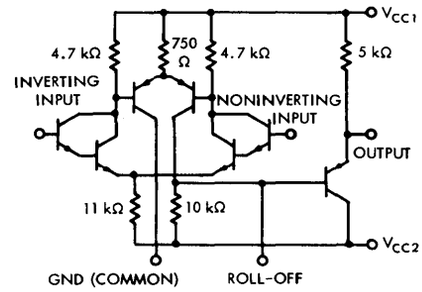
SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIERS
for application as

- **Buffer Amplifier**
- **Differentiator**
- **Integrator**
- **Multivibrator**
- **Level Detector**
- **Summing Amplifier**

description

Each of these networks is a general-purpose operational amplifier consisting of two differential-gain stages and a single-ended emitter-follower output. The input stage utilizes Darlington-connected n-p-n transistors for high input impedance.

The SN724 and SN724L, two of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

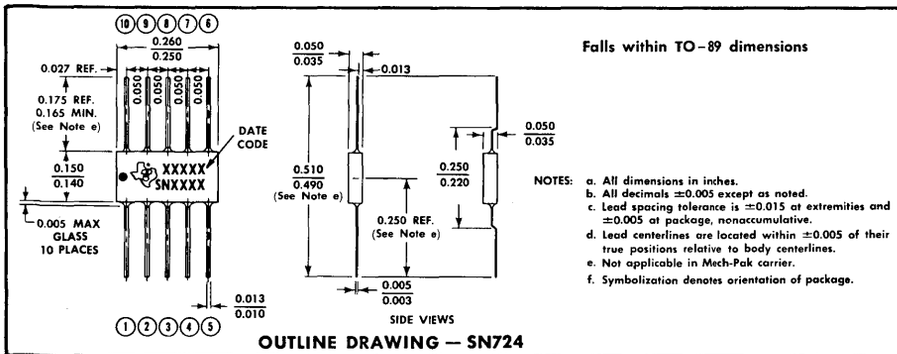
SCHEMATIC DIAGRAM

mechanical data

The SN724 operational amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN724 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

SN724 ORDERING INSTRUCTIONS

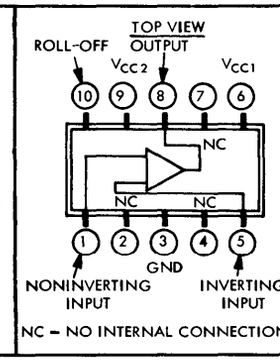
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



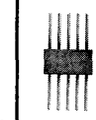
Falls within TO-89 dimensions

NOTES:
a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

OUTLINE DRAWING — SN724

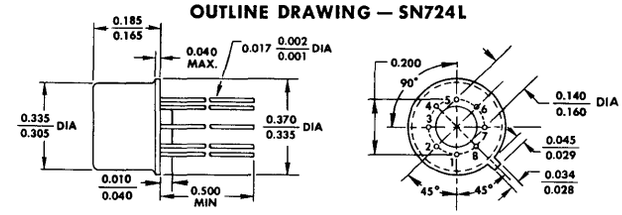


NC – NO INTERNAL CONNECTION

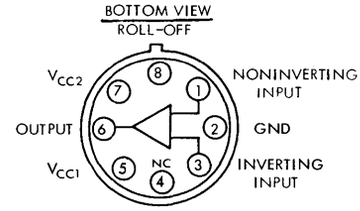


The SN724L package outline is same as JEDEC TO-76 except for case height.

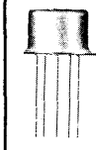
OUTLINE DRAWING — SN724L



DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED



NC — NO INTERNAL CONNECTION



†Patented by Texas Instruments.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . + 15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . 12 V
Common-Mode Input Voltage . . . . . ±10 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			15		mV
		T_A = 0°C to 70°C			40	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = 0°C to 70°C		30		μV/deg
I_{in}	Input Current			110	500	nA
I_{DI}	Differential-input offset current			44		nA
		T_A = 0°C		18		nA
		T_A = 70°C		70		nA
V_{OM}	Maximum peak-to-peak output voltage	f = 1 kc/s, T_A = 0°C to 70°C	8			V
		f = 1 kc/s,		12		V
		10 kΩ load, f = 1 kc/s, T_A = 0°C to 70°C	6			V
		10 kΩ load, f = 1 kc/s		11		V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_V	Voltage gain	f = 1 kc/s, T_A = 0°C to 70°C	400			
		f = 1 kc/s		1200		
CMRR	Common-mode rejection ratio	f = 1 kc/s, T_A = 0°C to 70°C		55		dB
BW	Bandwidth (−3 dB)		60	140		kc/s
Z_{in}	Input impedance	f = 1 kc/s	250	800		kΩ
Z_{out}	Output impedance	f = 1 kc/s		300		Ω
P_T	Total power dissipation	No input signal, no external load		120		mW

§Unless otherwise noted test conditions are: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

letter symbol and parameter definitions

V_{DI} — That d-c voltage which must be applied between the input terminals to obtain zero-output voltage referenced to ground. The application of this voltage balances the amplifier.

I_{in} — The current into either input of the amplifier.

I_{DI} — The difference in the currents into the two input terminals when the output is balanced.

V_{OM} — The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.

V_{CMIM} — The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.

CMRR — The ratio of the differential-mode voltage gain to the common-mode voltage gain.

BW — The range of frequencies within which the voltage gain is within 3 dB of the mid-frequency value.

Z_{in} — The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.

Z_{out} — The impedance between the output terminal and ground when the output is balanced.

TYPICAL CHARACTERISTICS§

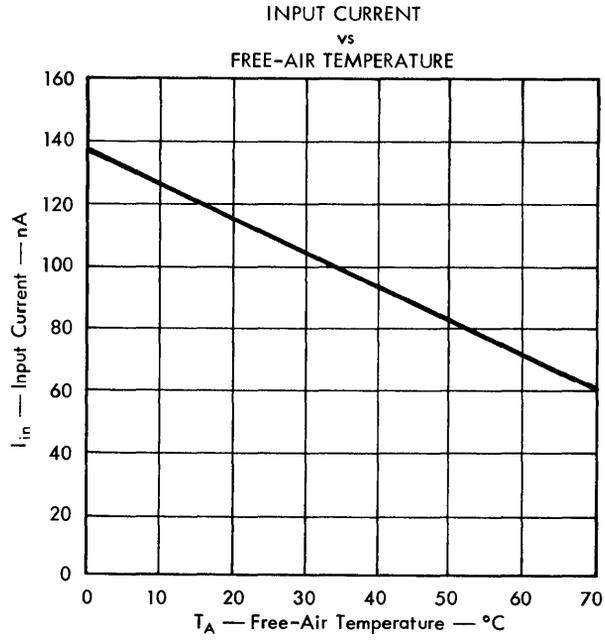


FIGURE 1

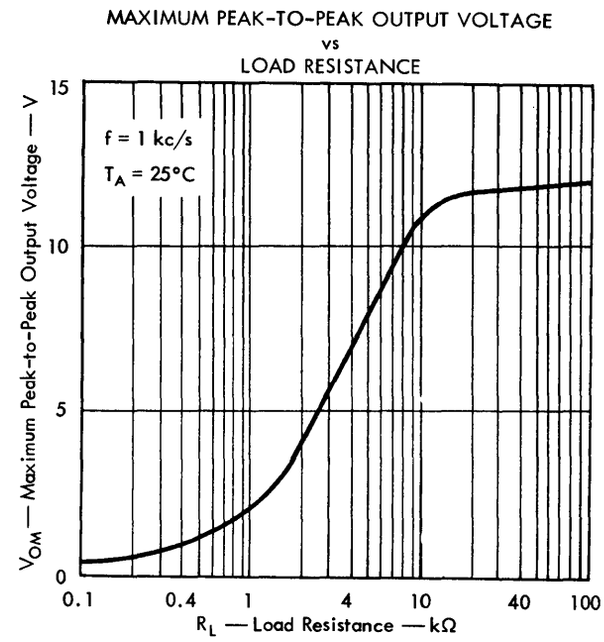


FIGURE 2

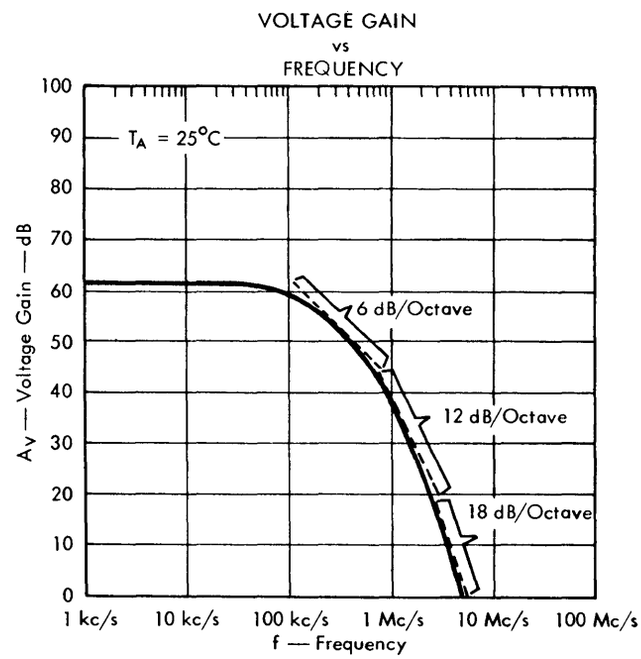


FIGURE 3

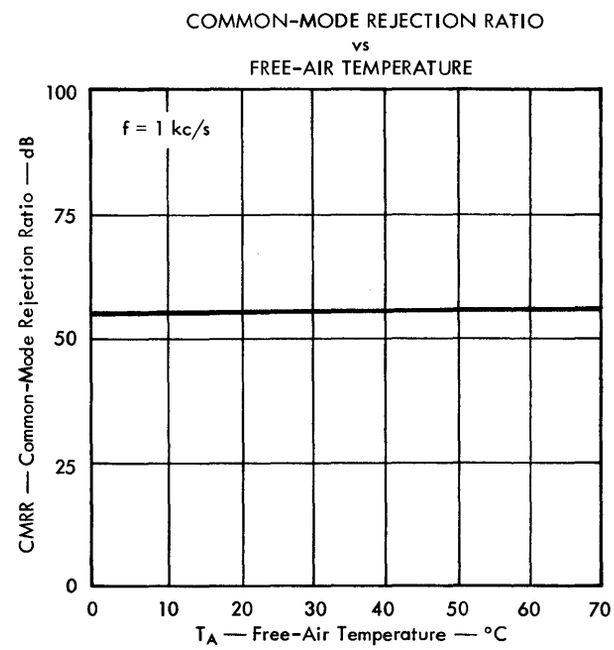


FIGURE 4

§Unless otherwise noted test conditions are: V_{CC1} = +12 V, V_{CC2} = −12 V, ground and V_{DI} applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

TYPICAL CHARACTERISTICS§

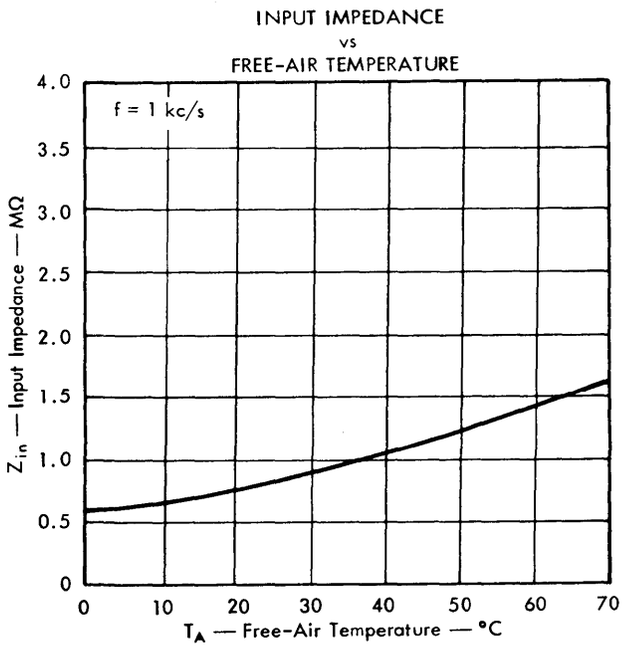


FIGURE 5

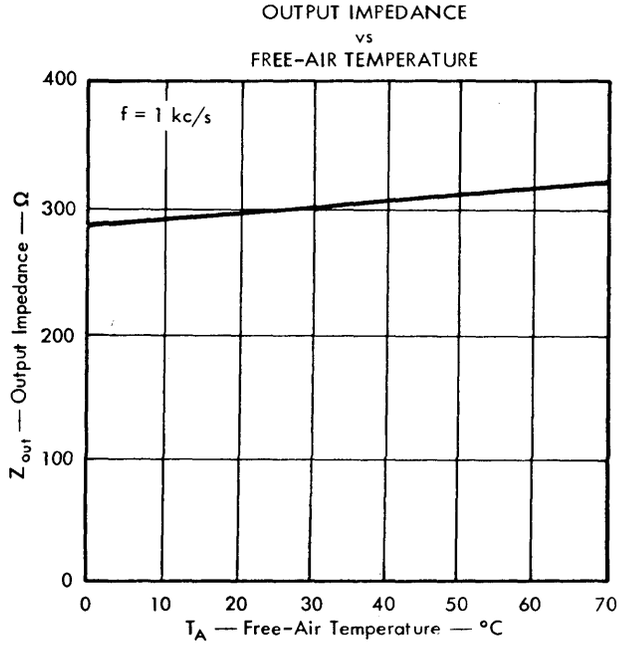


FIGURE 6

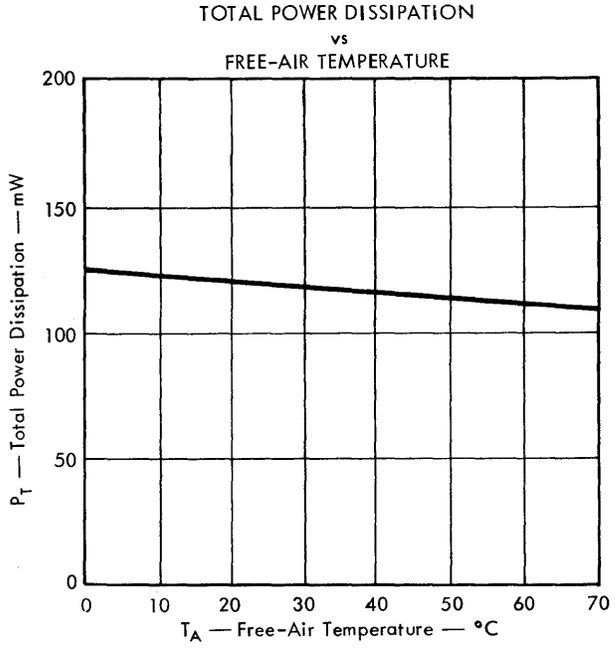


FIGURE 7

§Unless otherwise noted test conditions are: $V_{CC1} = +12$ V, $V_{CC2} = -12$ V, ground and V_{DI} applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

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TYPES SN7500, SN7501, SN7502 SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

TYPES SN7500, SN7501, SN7502
BULLETIN NO. DL-S 668909, OCTOBER 1966

SERIES 75 HIGH-SPEED SENSE AMPLIFIERS FOR CONVERSION OF COINCIDENT-CURRENT MEMORY READ-OUT TO SATURATED-DIGITAL LOGIC LEVELS

application

The SN7500, SN7501, and SN7502 are designed to detect bipolar magnetic-core-memory signals and convert them to logic levels compatible with standard diode-transistor logic (DTL) or transistor-transistor logic (TTL). Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 70°C.

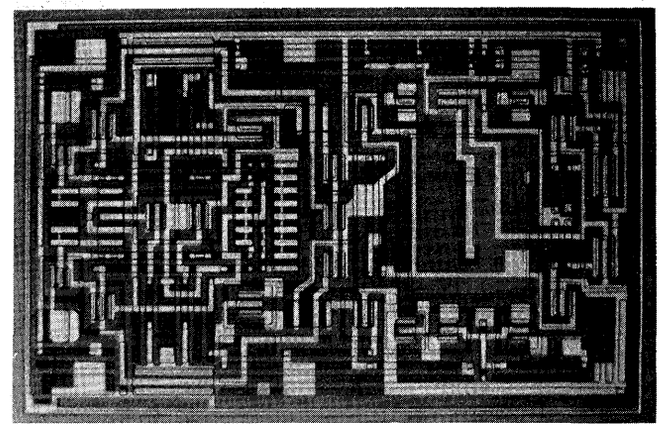
features

PERFORMANCE

- **perform both time and amplitude signal discrimination**
- **adjustable input-threshold voltage level**
- **extremely narrow region of threshold voltage uncertainty**
- **good fan-out capability**
- **typical differential input to logic-output propagation delay time of 50 ns**
- **fast overload recovery time**

EASE OF DESIGN

- **choice of output circuit function**
- **TTL or DTL drive capability**
- **standard logic supply voltages**



TYPE SN7500 CIRCUIT BAR

description

The SN7500 and SN7502 are sense amplifiers with one-shot-output circuits. The SN7500 features a double-ended output with high fan-out capability. The SN7502 features a variable-threshold differential-input circuit, externally controlled output pulse width, and a single-ended output capable of performing dot-OR logic.

The SN7501 is a sense amplifier with flip-flop output circuit. It also features a variable-threshold differential-input circuit. Functions of the internal R-S flip-flop include direct reset and complementary outputs.

All three networks incorporate a strobe input so that threshold detection will occur when the signal-to-noise ratio is at a maximum.

CONTENTS

†Patented by Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

design characteristics

Series 75 sense amplifiers have been designed for use with coincident-current memory systems. The sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. The low-level pulses originating in the memory are transformed into logic levels compatible with the logic section.

A distinct feature of these amplifiers is the extremely narrow region of uncertainty of the threshold circuit. This is accomplished by the high over-all gain coupled with a regenerative output stage. The threshold level of the design is well-defined and any change in this level due to temperature or external reference control can be readily predicted.

A strobe or enable gate is included in the design so the threshold detector can be enabled when the signal-to-noise ratio is a maximum during the system read cycle and inhibited during the write cycle.

The output circuits are designed to be compatible with the available DTL and TTL integrated logic circuits and are characterized for operation with these devices.

circuit operation

The basic Series 75 sense amplifier circuit is shown in figure A.

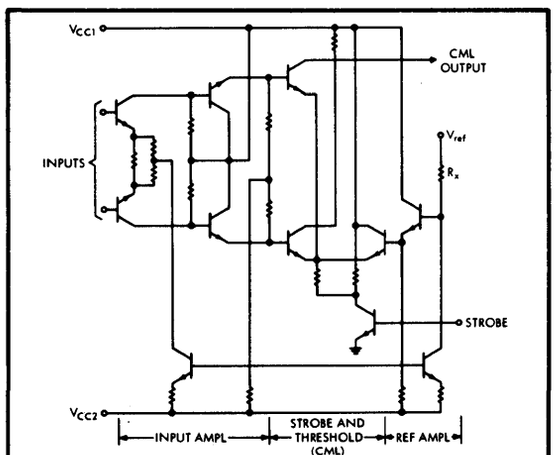


FIGURE A — BASIC SERIES 75 SENSE AMPLIFIER CIRCUIT

The differential-amplifier outputs are used as inputs for a current-mode-logic (CML) circuit. The reference voltage for the CML circuit is determined by the reference amplifier which is common-mode coupled to the input amplifier through the current sources. This common-mode loop stabilizes the reference-amplifier output voltage with respect to the input-amplifier output voltage. The design voltage levels are such that the reference voltage is positive with respect to the amplifier output voltage levels by an amount directly related to the threshold voltage. The result is that the CML output voltage is high if no differential-input voltage is present. A differential-input voltage large enough in amplitude to swing one amplifier output voltage more positive than the reference voltage will switch the CML circuit, thus causing a negative voltage transient at the CML output. The strobe transistor enables or inhibits action of the CML circuit.

input threshold voltage

Since the input threshold voltage is related to the reference-amplifier output voltage, the threshold voltage, developed across resistor R_x (figures A and B) in the SN7500, can be made externally adjustable by providing a method to vary the reference-amplifier input voltage. The reference input terminal (V_{ref}) is provided on the SN7501 and SN7502 to allow external generation of the reference voltage.

SN7500

The SN7500 sense amplifier with one-shot output requires no external components for operation in a conventional 2-μs memory. The circuit is shown in figure B.

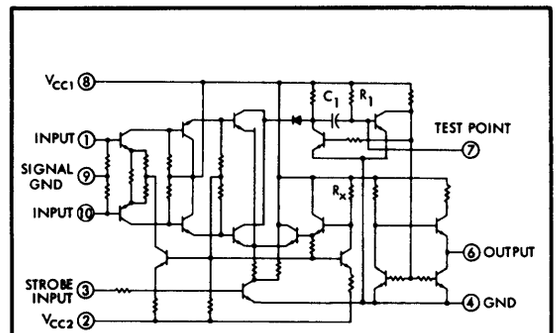


FIGURE B — SN7500 SCHEMATIC DIAGRAM

The SN7500 incorporates a one-shot to provide regeneration and to extend the output pulse width. The pulse width is established internally by the time constant of the R_1C_1 combination. To minimize the external circuitry, sense-line terminations to a signal ground are included in the design. Since these resistors are fabricated using standard diffusion processes, they will exhibit a temperature coefficient of approximately +0.2 percent per centigrade degree. Match of the two termination resistors is nominally 2 percent.

The threshold voltage of the SN7500 is nominally 17 mV, a value chosen to be compatible with most coincident-current memories in the 2-μs range. The threshold reference voltage (V_{ref}) is generated internally to eliminate the need for external components.

The output is an inverting, double-ended (totem-pole) circuit providing capability for sinking load current or supplying source current. This output will drive high-capacitance loads with good rise and fall times with little degradation in output waveform.

SN7502

The SN7502 is very similar to the SN7500 in function and design, except that external components are utilized to increase the flexibility of the circuit. Figure C shows the circuitry for the SN7502.

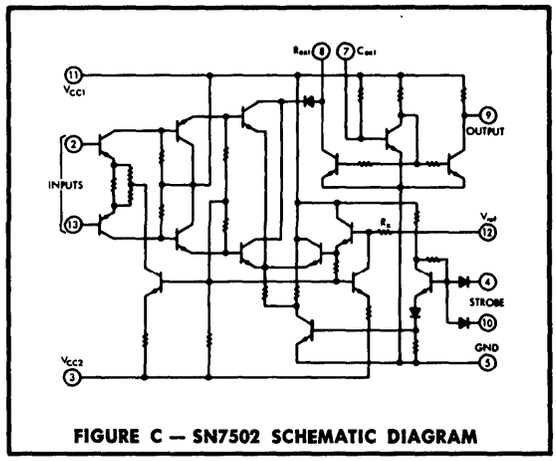


FIGURE C — SN7502 SCHEMATIC DIAGRAM

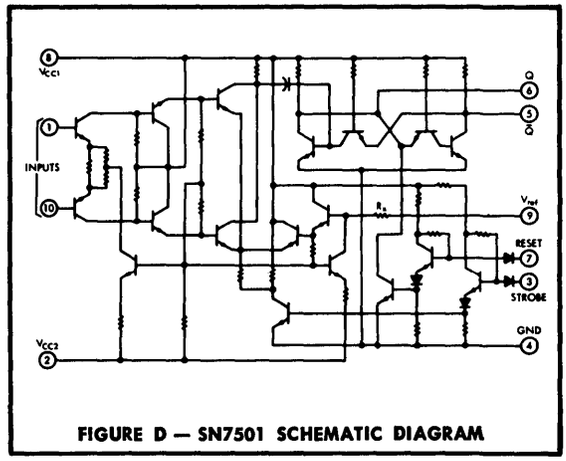


FIGURE D — SN7501 SCHEMATIC DIAGRAM

Unlike the SN7500, the output-pulse width of the SN7502 can be varied by C_{ext} and the input-threshold-voltage level can be adjusted by V_{ref}. Dual DTL strobe inputs increase strobing flexibility and an inverting, single-ended output stage is used to provide a wired-OR output capability. The SN7502, when connected to operate with minimum output pulse width, can be used in the 1-μs memory range.

SN7501

The SN7501 sense amplifier offers maximum flexibility. The device includes a flip-flop with a direct reset capability and complementary outputs. The flip-flop is "set" by a differential input greater than the input-threshold-voltage level which may be adjusted by the external V_{ref} supply. Figure D shows the circuit for the SN7501. The flip-flop output circuit can be used as a temporary data storage element.

Both the stored information and its complement appear in the flip-flop after reading from the memory and are available as inputs to the logic section.

output drive capability

The output circuits for the SN7500, SN7501, and SN7502 feature the ability to both sink or supply load current. This capability permits direct use with both DTL- and TTL-type loads.

input current requirements

Input current requirements reflect worst-case conditions for T_A = 0°C to 70°C and V_{CC1} = +5 V, V_{CC2} = −5 V, and V_{in} as indicated in the table.

INPUT CURRENT REQUIREMENTS

TYPE	INPUT	V_{in}	I_{in} (MAX)
SN7500	Strobe	2.6 V	2.5 mA
SN7501	Strobe or Reset	5 V	5 μA
		0 V	−1.6 mA
SN7502	Strobe	5 V	5 μA
		0 V	−1.6 mA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages:

V_{CC1}	+7 V
V_{CC2}	−7 V
V_{ref}	+7 V
Strobe and Reset Input Voltages	+6 V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTE: Voltage values are with respect to network ground terminal.

logic definition

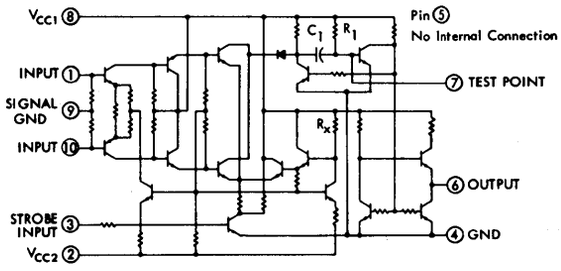
Standard POSITIVE LOGIC with the following definitions is used for specifying digital-level signals:

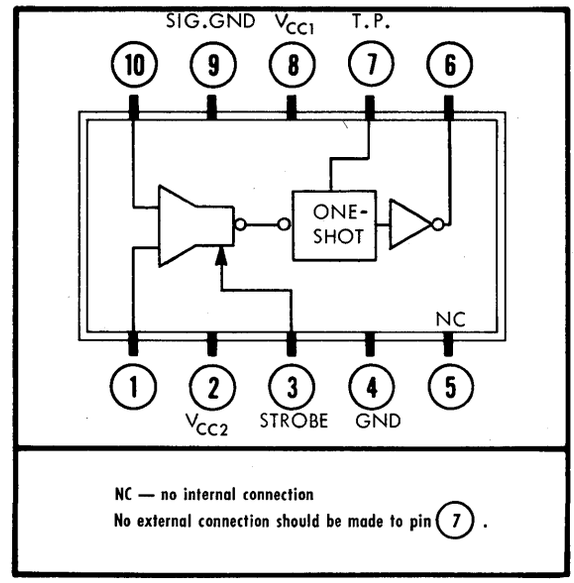
LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

TYPE SN7500
SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

schematic





recommended operating conditions

Supply Voltages:	V_{CC1}	+5 V
	V_{CC2}	−5 V
Strobe Input Voltages:	Logical 0 Level	0 to +0.5 V
	Logical 1 Level	+2 V to +5 V

electrical characteristics (unless otherwise noted, V_{CC1} = + 5 V, V_{CC2} = −5 V, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_T	Differential-input threshold voltage (see note 1)	1		10		30	mV
			T_A = 25°C	10	17	30	mV
V_{CMF}	Common-mode-input firing voltage (see note 2)		T_A = 25°C *Strobe Input:* V_{inS} = 2.6 V *Common-Mode Input Pulse:* $t_r = t_f$ = 50 ns, $t_{p(in)}$ = 150 ns		2		V
$V_{out(1)}$	Logical 1 output voltage	2	I_{load} = −8 mA	2.6			V
$V_{out(0)}$	Logical 0 output voltage	3	I_{sink} = 8 mA			0.4	V
$I_{in(1)S}$	Logical 1 level strobe-input current	4	V_{inS} = 2.6 V		1.2	2.5	mA
r_{inD}	Differential-input d-c resistance	6	Supply voltages are not applied	150	200	300	Ω
I_{CC1}	V_{CC1} supply current	7			15		mA
I_{CC2}	V_{CC2} supply current	7			−10		mA

†Signal-ground terminal is open.

NOTES: 1. The differential-input threshold voltage (V_T) is defined as that pulse or d-c input voltage (V_{in}) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.

2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.

switching characteristics, $V_{CC1} = +5$ V, $V_{CC2} = -5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(0)D}$	Propagation delay time to logical 0 level (differential input-to-output)	8	$V_{inD} = 50$ mV, $C_L = 15$ pF, $I_{sink} = 8$ mA		50	125	ns
$t_{pd(0)S}$	Propagation delay time to logical 0 level (strobe input-to-output)	9	$V_{inD} = 50$ mV, $C_L = 15$ pF, $I_{sink} = 8$ mA		45	100	ns
$t_{p(0)}$	Logical 0 output pulse width	8	$V_{inD} = 50$ mV, $C_L = 15$ pF, $I_{sink} = 8$ mA	200	500	800	ns
t_{orD}	Differential-input overload recovery time (see note 1)		*Differential Input Pulse:* $V_{inD} = 2$ V, $t_r = t_f = 20$ ns		20		ns
t_{orCM}	Common-mode-input overload recovery time (see note 2)		*Common-Mode Input Pulse:* $V_{inCM} = \pm 2$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(min)}$	Minimum cycle time		$t_{pS} = 100$ ns		1.5		μs

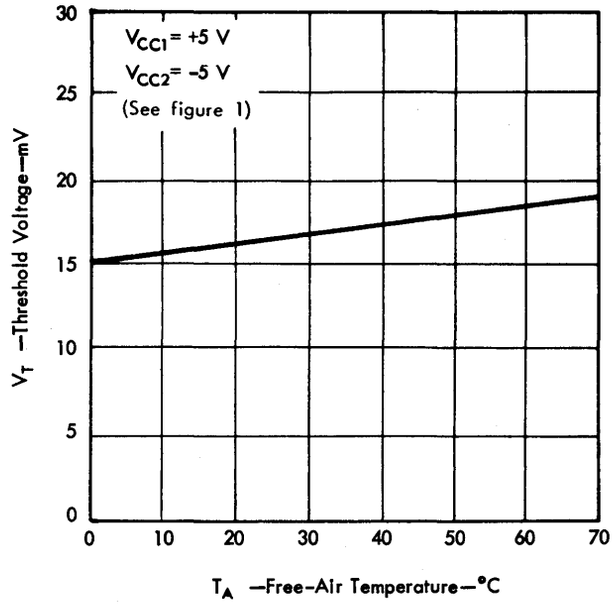
†Signal-ground terminal is open

NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.

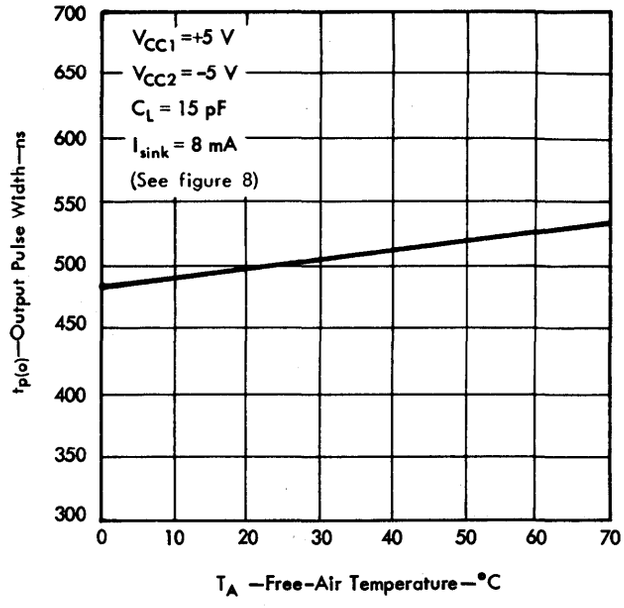
2. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

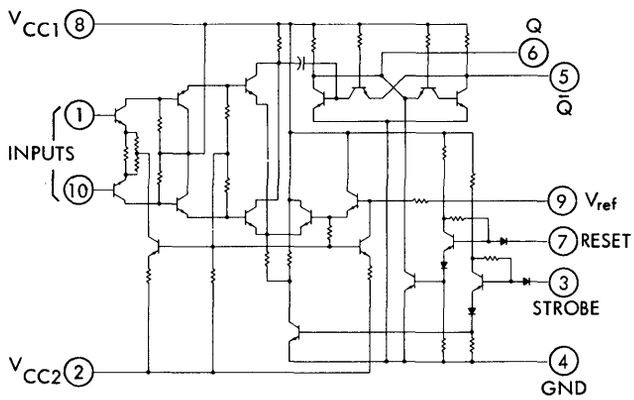


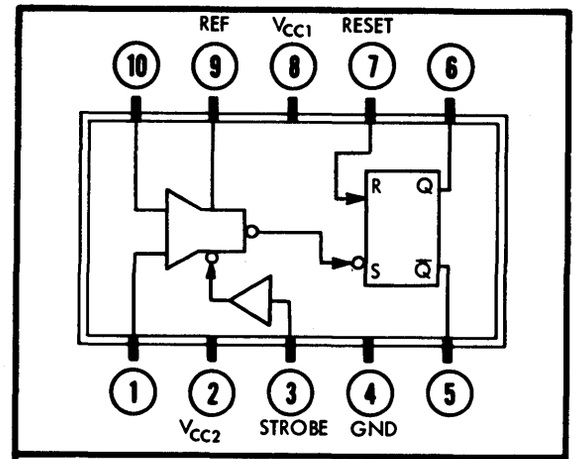
OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE



TYPE SN7501
SENSE AMPLIFIER WITH FLIP-FLOP OUTPUT

schematic





positive logic

High input to reset Q to logical 0.

recommended operating conditions

Supply Voltages:	V_{CC1}	+5 V
	V_{CC2}	−5 V
	V_{ref}	+3.8 V to +5 V
Strobe and Reset Input Voltages:	Logical 0 Level	0 to +0.8 V
	Logical 1 Level	+2 V to +5 V

electrical characteristics, V_{CC1} = + 5 V, V_{CC2} = −5 V (unless otherwise noted, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_T	Differential-input threshold voltage (see note 1)	1	T_A = 0°C	12		20	mV
			T_A = 25°C	14		20	mV
			T_A = 70°C	14		24	mV
V_{CMF}	Common-mode input firing voltage (see note 2)		T_A = 25°C *Strobe Input:* V_{inS} = 2.6 V *Common-Mode-Input Pulse:* $t_r = t_f$ = 50 ns, t_p = 150 ns		2		V
$V_{out(1)}$	Logical 1 output voltage	2	I_{load} = −1 mA	2.6			V
$V_{out(0)}$	Logical 0 output voltage	3	I_{sink} = 4 mA			0.4	V
$I_{in(1)}$	Logical 1 level strobe or reset input current	4	V_{in} = 5 V			5	μA
$I_{in(0)}$	Logical 0 level strobe or reset input current	5	V_{in} = 0			−1.6	mA
z_{inD}	Differential-input impedance (see note 3)		f = 1 kHz		5		kΩ
I_{CC1}	V_{CC1} supply current	7			18		mA
I_{CC2}	V_{CC2} supply current	7			−10		mA
I_{ref}	V_{ref} supply current	7			2.5	3	mA

†V_{ref} = +4 V

NOTES: 1. The differential-input threshold voltage (V_T) is defined as that pulse or d-c input voltage (V_{in}) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.

2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.

3. The differential-input impedance parameter is shown for reference only. This input impedance will not appreciably shunt a low impedance sense-line termination.

switching characteristics, $V_{CC1} = +5$ V, $V_{CC2} = -5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(1)D}$	Propagation delay time to logical 1 level (differential input to output)	8	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{load} \leq -10\ \mu$A		45	75	ns
$t_{pd(0)D}$	Propagation delay time to logical 0 level (differential input to output)	8	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{sink} = 4$ mA		45	75	ns
$t_{pd(1)R}$	Propagation delay time to logical 1 level (reset input to output)	8	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{load} \leq -10\ \mu$A		20	75	ns
$t_{pd(0)R}$	Propagation delay time to logical 0 level (reset input to output)	8	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{sink} = 4$ mA		20	75	ns
$t_{pd(1)S}$	Propagation delay time to logical 1 level (strobe input to output)	9	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{load} \leq -10\ \mu$A		45	75	ns
$t_{pd(0)S}$	Propagation delay time to logical 0 level (strobe input to output)	9	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{sink} = 4$ mA		45	75	ns
t_{orD}	Differential-input overload recovery time (see note 1)		*Differential Input Pulse:* $V_{inD} = 2$ V, $t_r = t_f = 20$ ns	20			ns
t_{orCM}	Common-mode input overload recovery time (see note 2)		*Common-Mode Input Pulse:* $V_{inCM} = \pm 2$ V, $t_r = t_f = 20$ ns	20			ns
$t_{cyc(min)}$	Minimum cycle time		$t_{pS} = 100$ ns, $t_{pR} = 100$ ns	0.7			μs

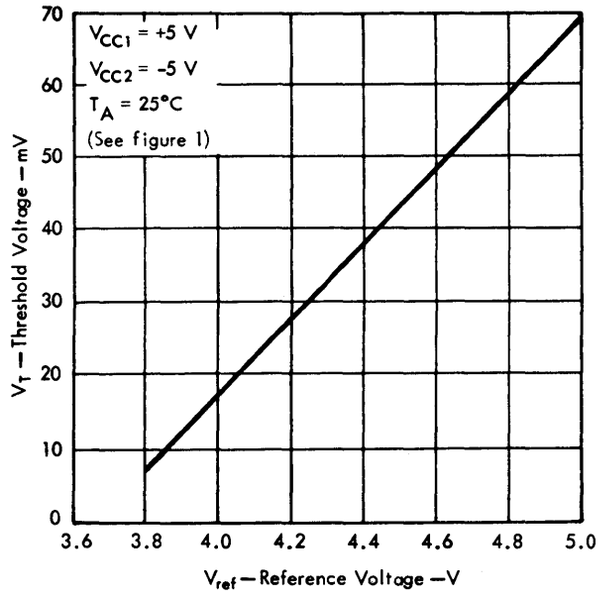
†$V_{ref} = +4$ V

NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

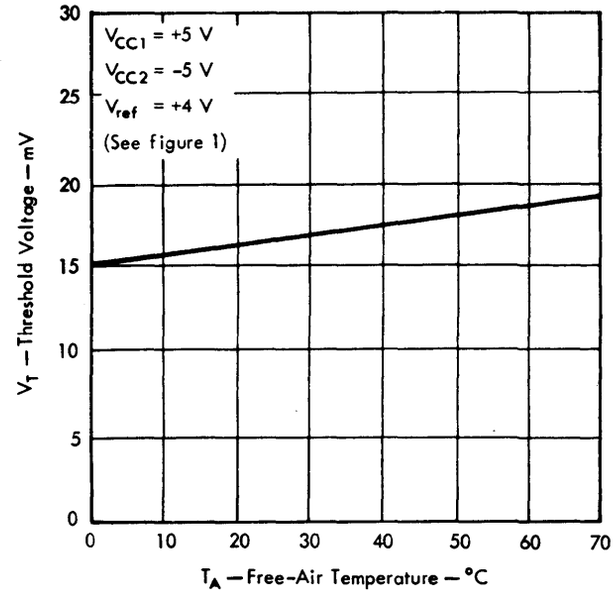
2. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
REFERENCE VOLTAGE

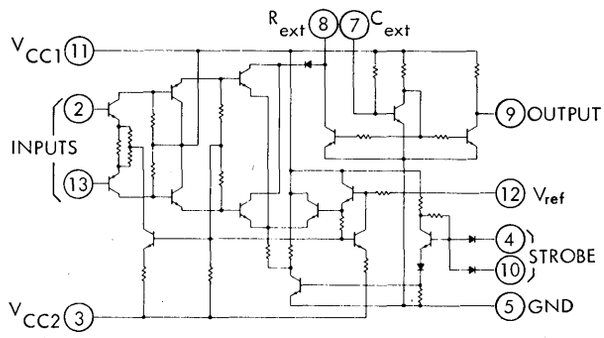


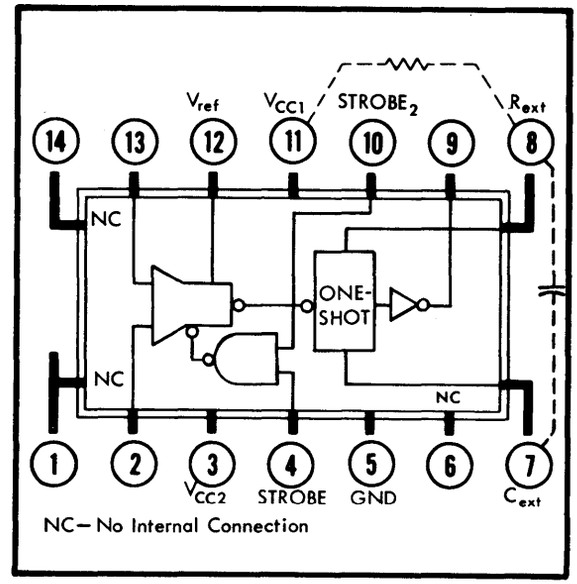
THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



TYPE SN7502
SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

schematic





recommended operating conditions

Supply Voltages:	V_{CC1}	+5 V
	V_{CC2}	−5 V
	V_{ref}	+4.3 V to +5 V
Strobe Input Voltages:	Logical 0 Level	0 to 0.8 V
	Logical 1 Level	+2 V to +5 V
Value of External Resistor and Capacitor:	R_{ext}	2 kΩ ±5%
	C_{ext}	47 pF minimum

electrical characteristics, V_{CC1} = + 5 V, V_{CC2} = −5 V (unless otherwise noted, T_A = 0°C to 70°C)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_T	Differential-input threshold voltage (see note 1)	1	C_{ext} = 47 pF, T_A = 0°C	14		24	mV
			C_{ext} = 47 pF, T_A = 25°C	17		24	mV
			C_{ext} = 47 pF, T_A = 70°C	17		27	mV
V_{CMF}	Common-mode input firing voltage (see note 2)		C_{ext} = 47 pF, T_A = 25°C *Strobe Input:* V_{inS} = 2.6 V *Common-Mode Input Pulse:* $t_r = t_f$ = 50 ns, t_p = 150 ns		2.5		V
$V_{out(1)}$	Logical 1 output voltage	2	I_{load} = −150 μA	2.6			V
$V_{out(0)}$	Logical 0 output voltage	3	I_{sink} = 15 mA			0.4	V
$I_{in(1)}$	Logical 1 level strobe input current	4	V_{in} = 5 V			5	μA
$I_{in(0)}$	Logical 0 level strobe input current	5	V_{inS} = 0		−1.1	−1.6	mA
z_{inD}	Differential-input impedance (see note 3)		f = 1 kHz		5		kΩ
I_{CC1}	V_{CC1} supply current	7			15		mA
I_{CC2}	V_{CC2} supply current	7			−8		mA
I_{ref}	V_{ref} supply current	7			2.5	3	mA

†V_{ref} = +4.5 V and R_{ext} = 2 kΩ

NOTES: 1. The differential-input threshold voltage (V_T) is defined as that pulse or d-c input voltage (V_{in}) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.

2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.

3. The differential-input impedance parameter is shown for reference only. This input impedance will not appreciably shunt a low-impedance sense-line termination.

switching characteristics, $V_{CC1} = +5$ V, $V_{CC2} = -5$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(0)D}$	Propagation delay time to logical 0 level (differential input-to-output)	8	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{sink} = 15$ mA		60	100	ns
$t_{pd(0)S}$	Propagation delay time to logical 0 level (strobe input-to-output)	9	$V_{inD} = 30$ mV, $C_L = 15$ pF, $I_{sink} = 15$ mA		50	100	ns
$t_{p(0)}$	Logical 0 output pulse width	8	$V_{inD} = 30$ mV, $I_{sink} = 15$ mA	150		300	ns
t_{orD}	Differential-input overload recovery time (see note 1)		*Differential Input Pulse:* $V_{inD} = 2$ V, $t_r = t_f = 20$ ns		20		ns
t_{orCM}	Common-mode input overload recovery time (see note 2)		*Common-Mode Input Pulse:* $V_{inCM} = \pm 2$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(min)}$	Minimum cycle time		$t_{pS} = 100$ ns		1.5		μs

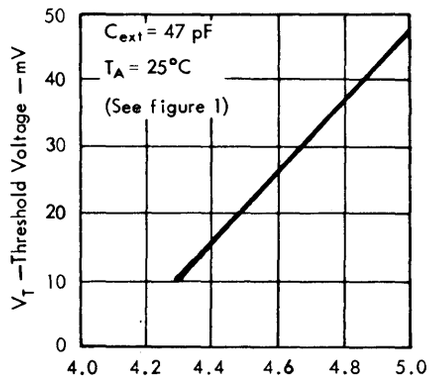
†$V_{ref} = +4.5$ V, $R_{ext} = 2$ kΩ and $C_{ext} = 47$ pF

NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

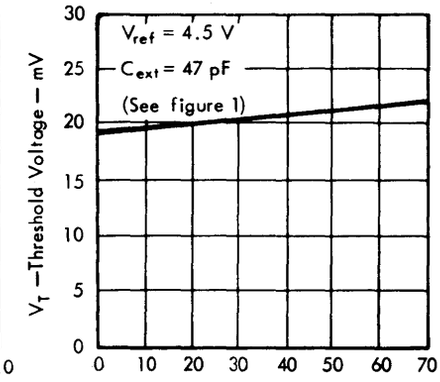
2. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input-overload signal prior to the strobe-enable signal.

TYPICAL CHARACTERISTICS§

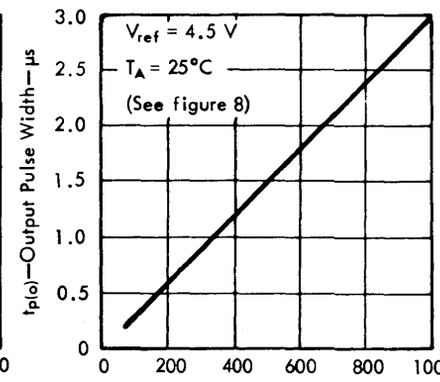
THRESHOLD VOLTAGE vs REFERENCE VOLTAGE



THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE



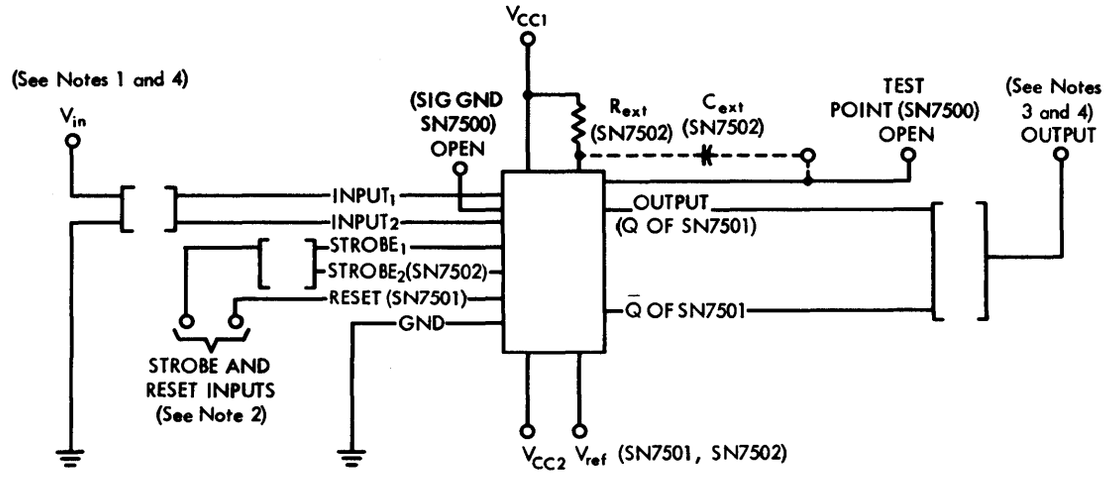
OUTPUT PULSE WIDTH vs EXTERNAL CAPACITOR VALUE



§$V_{CC1} = +5$ V, $V_{CC2} = -5$ V, and $R_{ext} = 2$ kΩ.

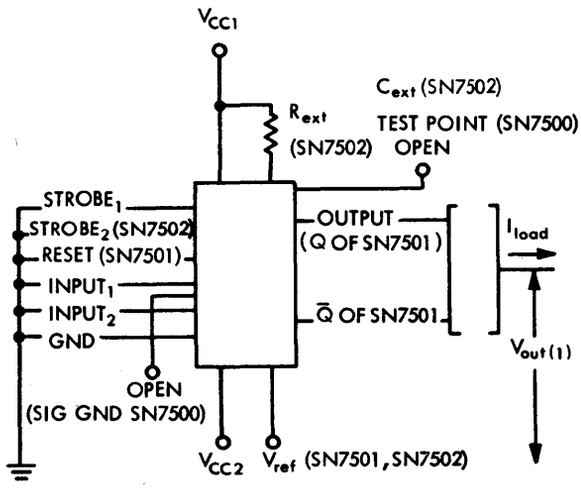
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



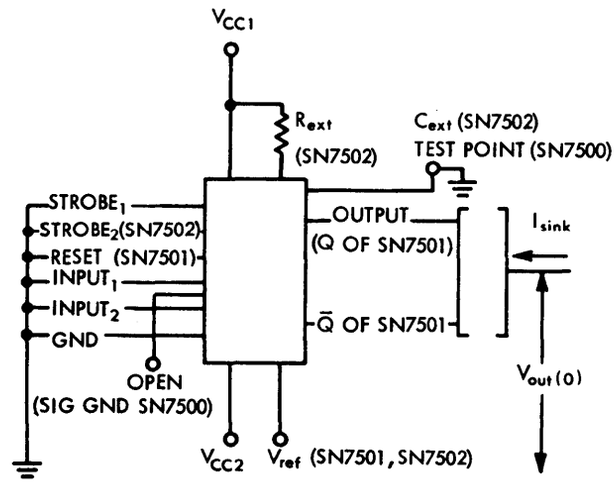
1. Both inputs are tested with voltages of the same polarity.
2. Strobe and reset input pulses are as shown in figure 8.
3. Both outputs are tested.
4. The differential-input threshold voltage (V_T) is defined as that pulse or d-c input voltage (V_{in}) just sufficient to cause the output (or outputs) to switch. For testing and correlation purposes a d-c input voltage is desirable.

FIGURE 1



1. When testing the SN7501, the output under test is set to logical 1 by applying a momentary ground to the opposite output.
2. Each output of the SN7501 is tested separately.

FIGURE 2



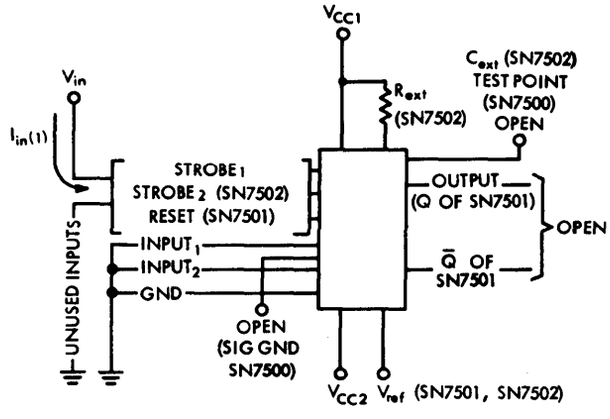
1. When testing the SN7501, the output under test is set to logical 0 by applying a momentary ground to the output to be tested.
2. Each output of the SN7501 is tested separately.

FIGURE 3

†Arrows indicate actual direction of current flow.

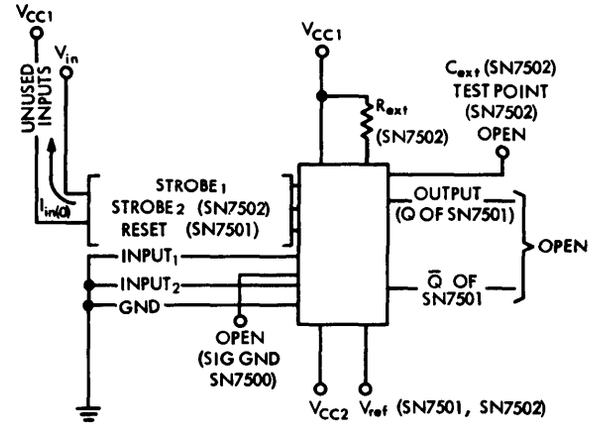
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each logic input is tested separately.

FIGURE 4



1. Each logic input is tested separately.

FIGURE 5

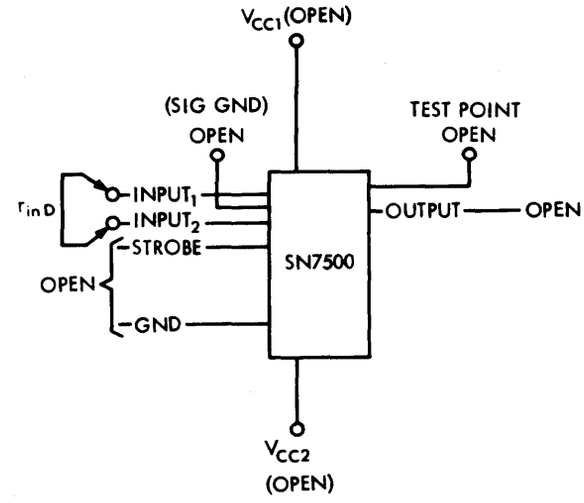


FIGURE 6

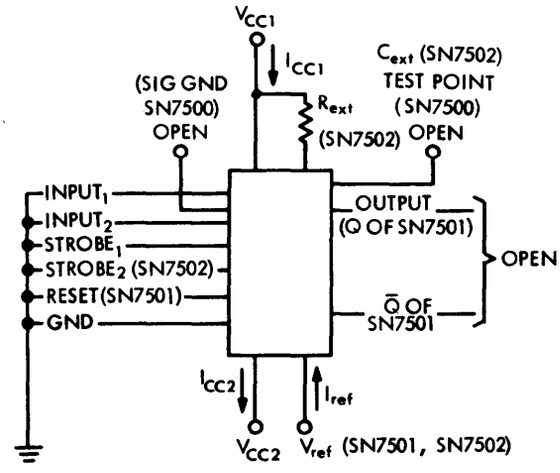
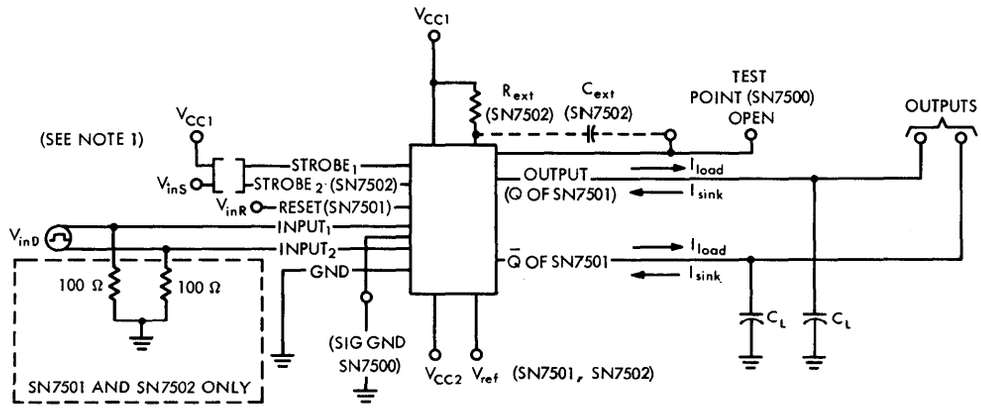


FIGURE 7

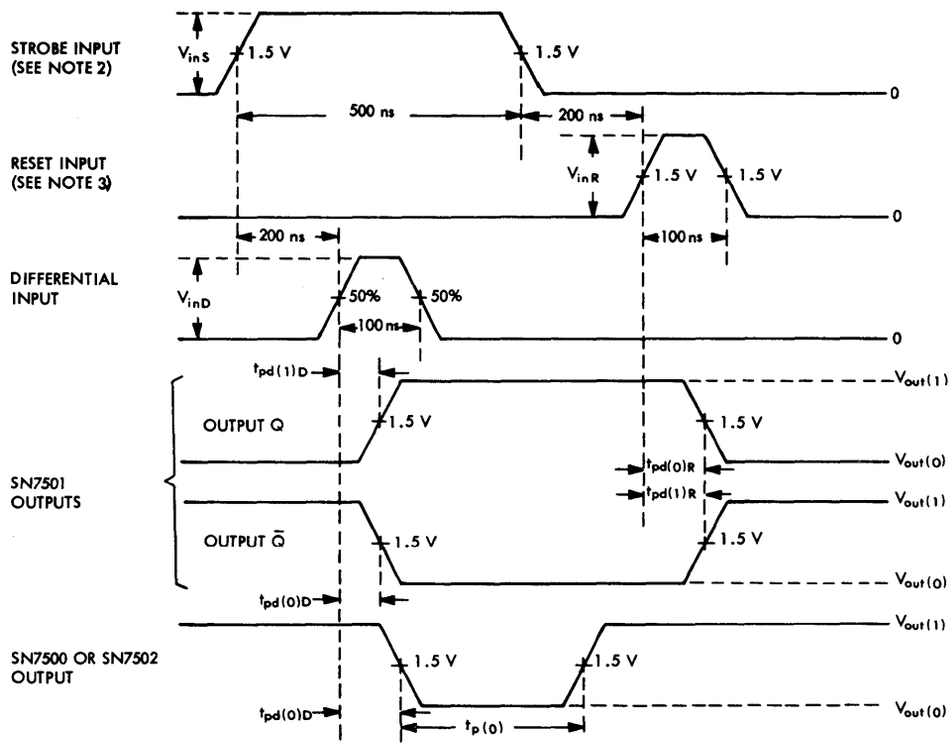
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

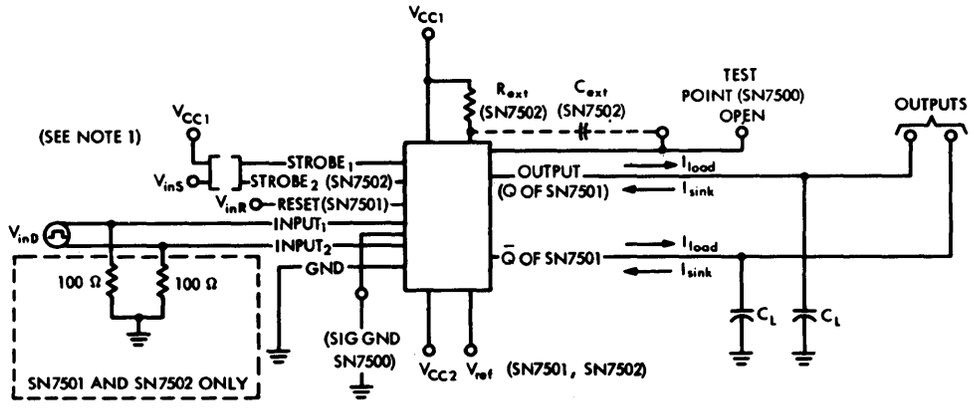
1. Each strobe input of the SN7502 is tested separately. The unused strobe input is connected to V_{CC1}.
2. Strobe input pulse characteristics: $V_{inS} = 3$ V, $t_r = t_f = 20$ ns.
3. Reset input pulse characteristics: $V_{inR} = 3$ V, $t_r = t_f = 20$ ns.
4. Differential-input pulse characteristics: $t_r = t_f = 20$ ns, PRR = 100 kHz, source impedance = 50 Ω.
5. All t_r and t_f specifications are from the 10% to 90% levels.

FIGURE 8 — DIFFERENTIAL AND RESET INPUT-TO-OUTPUT PROPAGATION DELAY TIME

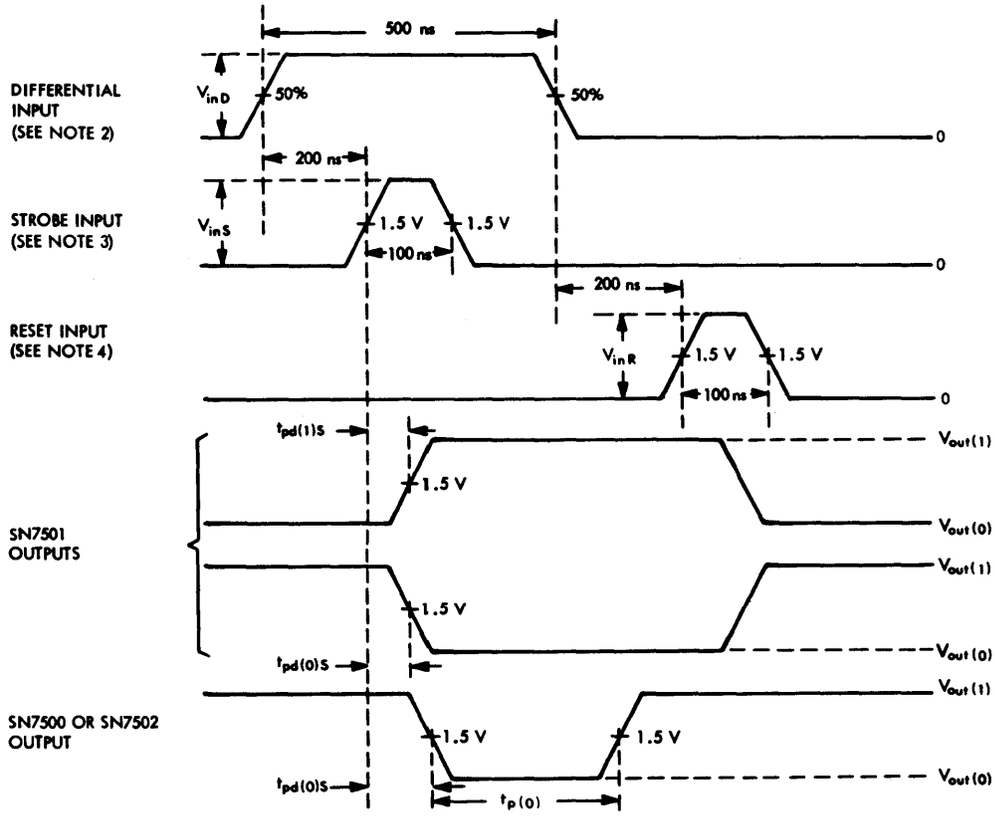
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics† (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Each strobe input of the SN7502 is tested separately. The unused strobe input is connected to V_{CC1}.
2. Differential-input pulse characteristics: $t_r = t_f = 20$ ns, PRR = 100 kHz, source impedance = 50 Ω.
3. Strobe-input pulse characteristics: $V_{inS} = 3$ V, $t_r = t_f = 20$ ns.
4. Reset-input pulse characteristics: $V_{inR} = 3$ V, $t_r = t_f = 20$ ns.
5. All t_r and t_f specifications are from the 10% to 90% levels.

FIGURE 9 — STROBE-INPUT-TO-OUTPUT PROPAGATION DELAY TIME

†Arrows indicate actual direction of current flow.

TYPICAL APPLICATION DATA

coincident-current memory application

This application fully utilizes the flexibility of the SN7501 in a typical coincident-current memory design. See figure 10.

One SN7501 sense amplifier is used to read-out the information from one plane (up to 4096 cores) of the memory, representing one bit in a stored word. A word is read-out by reading one bit from each plane in parallel. A location is selected by coincident currents in approriate x and y address lines. Cores in the "one" state switch to the "zero" state causing voltage pulses on their sense lines. Cores in the "zero" state do not switch but cause smaller amptitude voltage pulses on their sense lines. The sense amplifiers discriminate between these pulses representing stored logical "ones" and stored logical "zeros."

Since read-out is destructive, the information destroyed by read-out must be rewritten into the memory if it is to be retained for future use. A memory usually incorporates an inhibit register for this purpose. An important advantage of the SN7501 is that it contains a flip-flop that can be used as the inhibit register for its plane. "Ones" read from the memory "set" the flip-flops while "zeros" leave the flip-flops in their initial state. After read-out, therefore, the flip-flops of the SN7501's contain the information that was stored in the selected location. Since both outputs of the SN7501 flip-flops are brought out, both the selected word and its complement are available for use in the logic. The word thus stored in the SN7501's is available for use with the logic and for feedback to the inhibit drivers until a reset pulse clears the register prior to the next word read-out.

The variable-threshold capability of the SN7501 further extends its usefulness by allowing an optimum setting of the threshold level for a particular memory design. The threshold levels of the SN7501's in a memory may be adjusted either individually or in parallel.

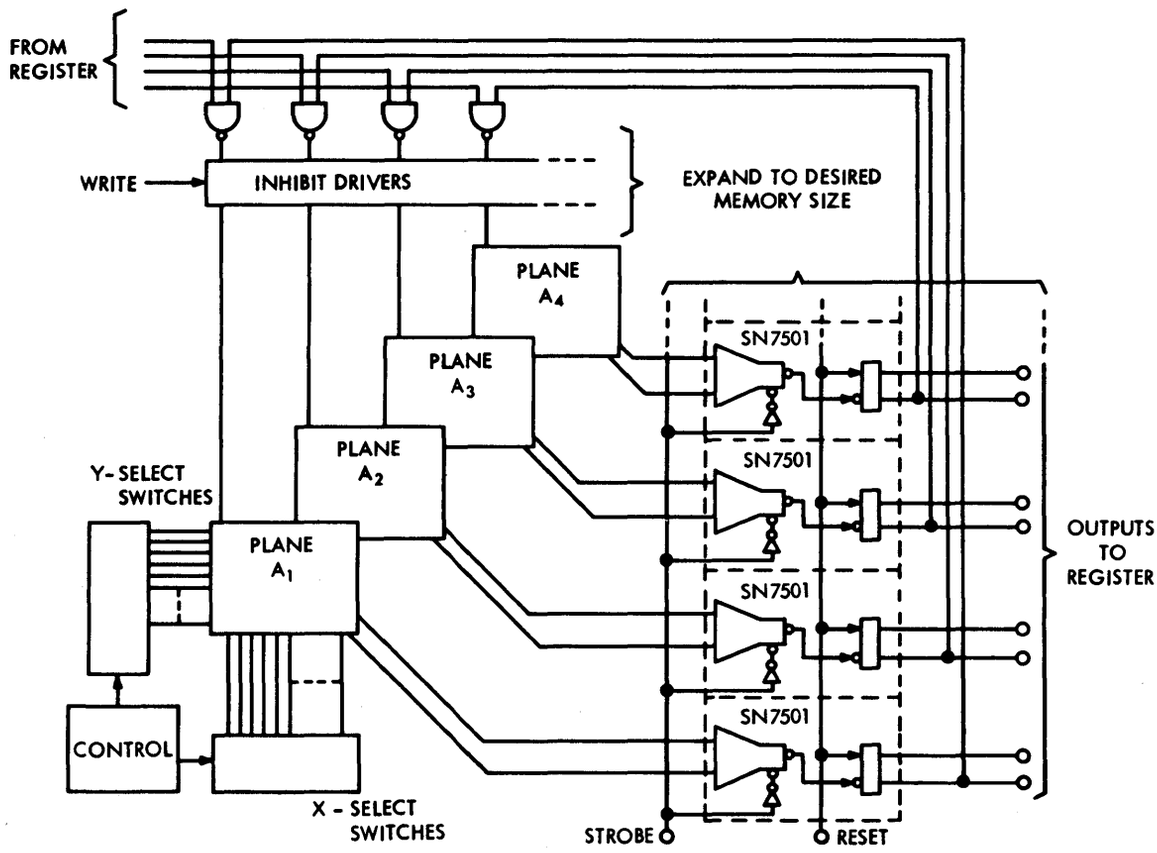


FIGURE 10 — COINCIDENT-CURRENT MEMORY USING SN7501 SENSE AMPLIFIERS

TYPICAL APPLICATIONS

variable threshold adjustment

The differential-input-threshold-voltage levels of the SN7501 or SN7502 may be adjusted for optimum memory performance by varying the amplitude of V_{ref}. V_{ref} should be derived from V_{CC1} or generated with respect to V_{CC1} rather than with respect to ground. (See figure 11) Any variations in V_{CC1} or V_{ref} will then cause minimal changes in the input-threshold-voltage level.

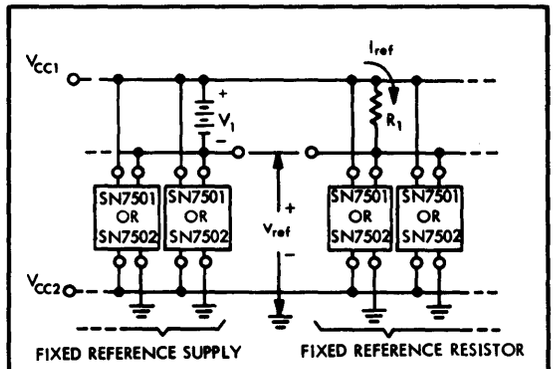


FIGURE 11 — INPUT THRESHOLD-VOLTAGE LEVEL GENERATION

Using one of these methods, adjust V_{ref} to obtain the desired threshold voltage. R_1 may be calculated as:

$$R_1 = \frac{V_{CC1} - V_{ref}}{I_{ref}}$$

This may apply for one sense amplifier or several sense amplifiers connected to the V_{ref} supply. V_1 can be measured and fixed. Some bypassing may be necessary at the V_{ref} terminal to eliminate noise problems where long leads are used.

SN7502 dot-OR capability

This application utilizes the output current sink capability of the SN7502 to perform the dot-OR function. The internal output load resistor of the SN7502 is approximately 7.5 kΩ. The output sink current is conservatively specified at 15 mA for a maximum $V_{out(0)}$ of 0.4 V. For this maximum $V_{out(0)}$ the nominal internal load current for the SN7502 is computed as follows:

$$\frac{V_{CC1} - V_{out(0)}}{R_L} = \frac{5 - 0.4\ V}{7.5\ k\Omega} = 0.61\ mA$$

To drive a worst-case DTL or TTL input requires a sink current capability of 1.6 mA. The remaining 13.4 mA may be used for sinking dot-OR-connected outputs. (See figure 12) Additional dot-OR connections may be made to utilize the remaining 13.4 mA of sink current up to a maximum number N of:

$$N = \frac{13.4}{0.61} = 22$$

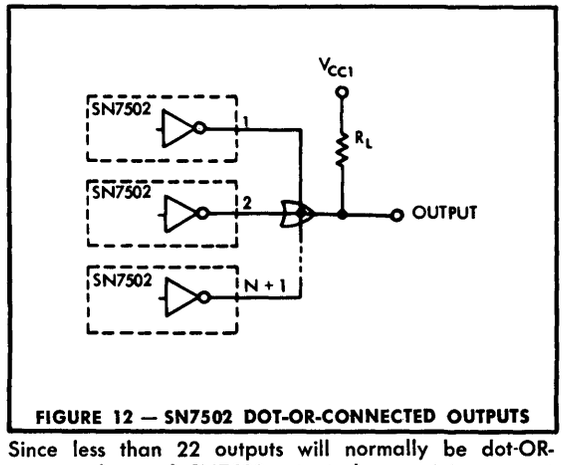


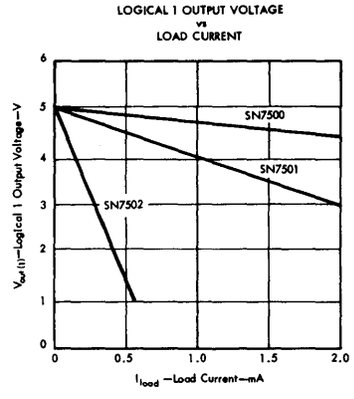
FIGURE 12 — SN7502 DOT-OR-CONNECTED OUTPUTS

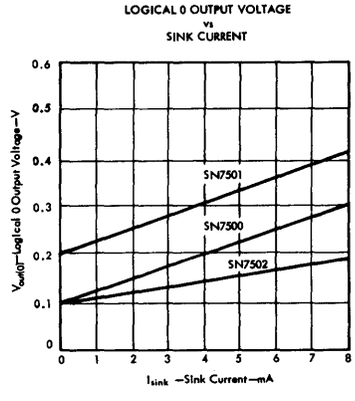
Since less than 22 outputs will normally be dot-OR-connected to each SN7502 output, the remaining current can be supplied from an external load resistor R_L. The load resistor reduces the output-voltage rise time to provide better capacitive-line driving capability. Value of the load resistor R_L may be calculated for a worst case (1.6 mA) DTL or TTL gate input load as follows:

$$R_L = \frac{4.6}{13.4 - n\ (0.61)} k\Omega$$

where n = one less than the number of SN7502 outputs connected to perform the dot-OR function.

TYPICAL CHARACTERISTICS§





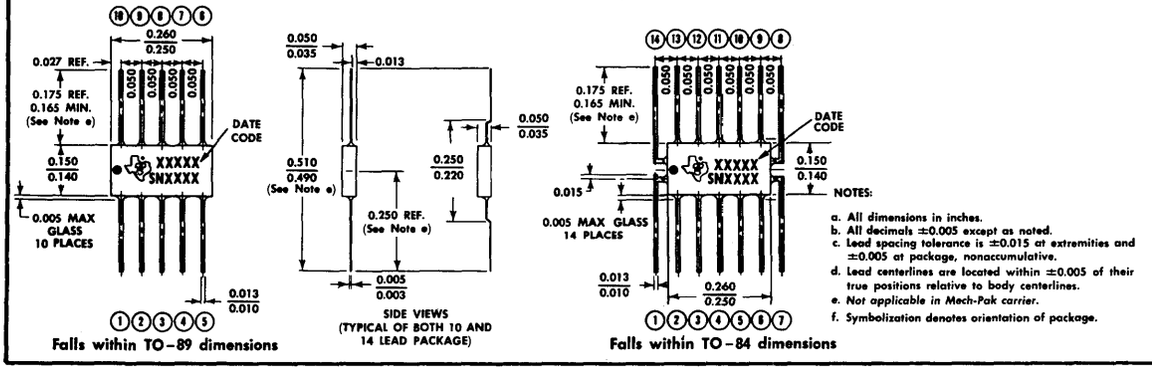
§V_{CC1} = 5 V, V_{CC2} = −5 V, and T_A = 25°C

MECHANICAL DATA

general

These three semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All three networks are available with formed leads, insulators attached, and/or mounted in Mech-Pak carriers.

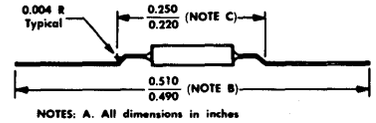
OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

FORMED LEADS



NOTES: A. All dimensions in inches
B. Not applicable in Mech-Pak Carrier
C. Measured from centerline of outside bends

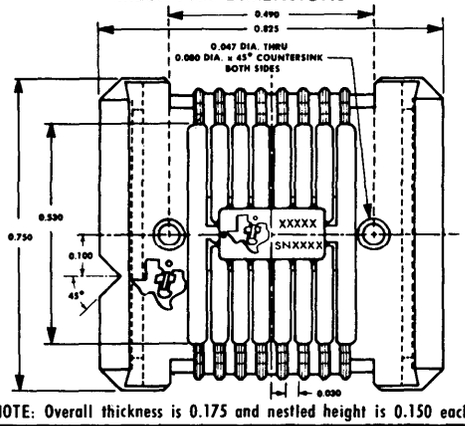
insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

MECH-PAK DIMENSIONS



NOTE: Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPE SNX1304
OPTOELECTRONIC PULSE AMPLIFIER

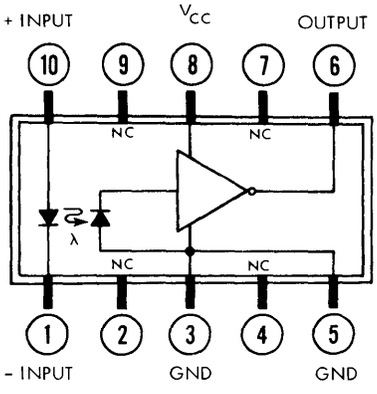
TYPE SNX1304
BULLETIN NO. DL-S 669811, NOVEMBER 1966
REPLACES BULLETIN NO. DL-S 657611, MAY 1965

SOLID CIRCUIT® SEMICONDUCTOR NETWORK†
AN EXPERIMENTAL OPTICALLY COUPLED DIGITAL INTEGRATED CIRCUIT

description

The SNX1304 is an experimental Optoelectronic Pulse Amplifier (OPA) for engineering evaluation. The OPA consists of a gallium arsenide p-n junction light emitter optically coupled to an integrated silicon photodetector feedback-amplifier circuit. The high input-output isolation of the optical coupling allows the OPA to function as a broad-band pulse transformer with response extending to zero frequency. The OPA is compatible for use with other digital integrated circuits. Applications include transmission of a-c or d-c signals across computer subsystem interfaces where circulating currents prevent interconnection of subsystem grounds, and rejection of common-mode noise at the end of a long data-transmission line.

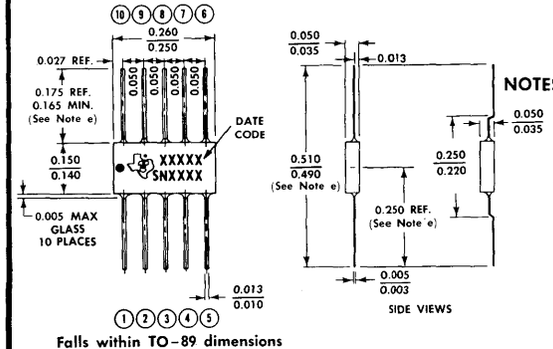
circuit symbol and pin identification



NOTES: 1. Forward input polarity is indicated.
2. NC — no internal connection.

mechanical data

The SNX1304 pulse amplifier is mounted in a glass-to-metal hermetically sealed, welded package. Package outline meets JEDEC TO-89. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit.



NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, nonaccumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

†Patented by Texas Instruments Incorporated

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input-to-Output Voltage	±100 V
Supply Voltage V_{CC}	+8 V
Reverse Input Voltage	3 V
Forward Input Current	.15 mA
D-C Fan-Out, N_{DC} (See Note 1)	15
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−55°C to 125°C

electrical characteristics

PARAMETER		TEST CONDITIONS			V_{CC} = 3V		V_{CC} = 6V		UNIT
					TYP	MAX	TYP	MAX	
$I_{in(th)}$	Forward Input Threshold Current	V_{out} = 0.5 V,		T_A = 125°C	5	10	5	10	mA
		V_{out} = 0.5 V,		T_A = −55°C	3		3		mA
V_F	Forward Input Voltage	I_{in} = 1.3 $I_{in(th)}$,		T_A = 125°C	1.1		1.1		V
		I_{in} = 1.3 $I_{in(th)}$,		T_A = −55°C	1.4		1.4		V
$V_{out(off)}$	"Off" Output Voltage	I_{in} = 0,	N_{DC} = 0,	T_A = 125°C	2.5		5.2		V
		I_{in} = 0,	N_{DC} = 15,	T_A = 125°C	2.3		5		V
		I_{in} = 0,	N_{DC} = 15,	T_A = −55°C	1.9		4.2		V
$V_{out(on)}$	"On" Output Voltage	I_{in} = 1.3 $I_{in(th)}$,		T_A = 125°C	0.2		0.25		V
		I_{in} = 1.3 $I_{in(th)}$,		T_A = −55°C	0.1		0.2		V
P_A	Amplifier Power Dissipation (See Note 2)	I_{in} = $I_{in(th)}$,	N_{DC} = 0,	T_A = 25°C	2.5		15		mW
		I_{in} = 0,	N_{DC} = 0,	T_A = 25°C	3		20		mW

switching characteristics

PARAMETER		TEST CONDITIONS	V_{CC} = 3V	V_{CC} = 6V	UNIT
			TYP	TYP	
t_d	Delay Time	I_{in} = 1.3 $I_{in(th)}$, N_{DC} = 1, T_A = 25°C, See Note 3	300	250	ns
t_r	Rise Time		200	150	ns
t_s	Storage Time		350	250	ns
t_f	Fall Time		250	200	ns

NOTES: 1. One d-c load (N_{DC} = 1) is defined by a circuit where C_s (see figure A) is selected so that the total capacitance of the test fixture, connectors, oscilloscope probe and C_s aggregates 50 pF. This rates fan-out in the same manner as Texas Instruments Series 51 networks.

2. This does not include the input power to the light-emitter diode.

3. The input pulse has the following characteristics: t_p = 5μs, $t_r \leq$ 10ns, $t_f \leq$ 10 ns, f = 40 kHz.

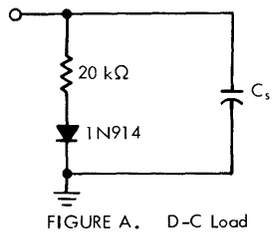
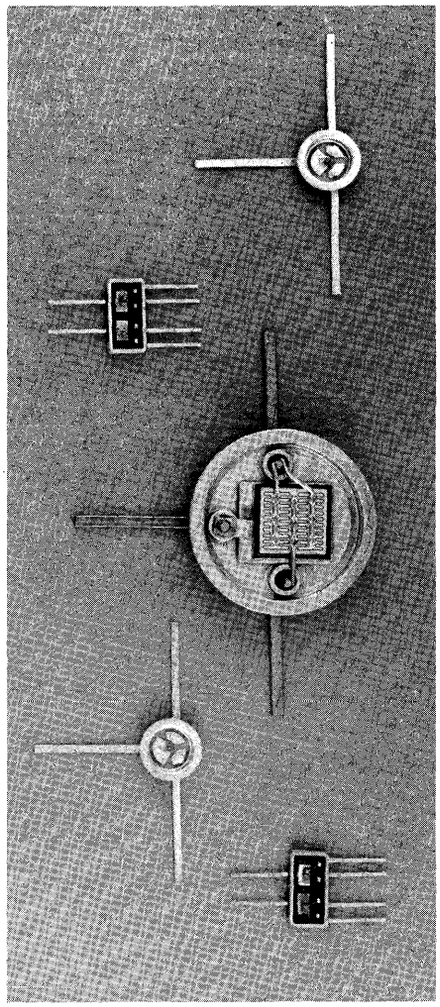


FIGURE A. D-C Load

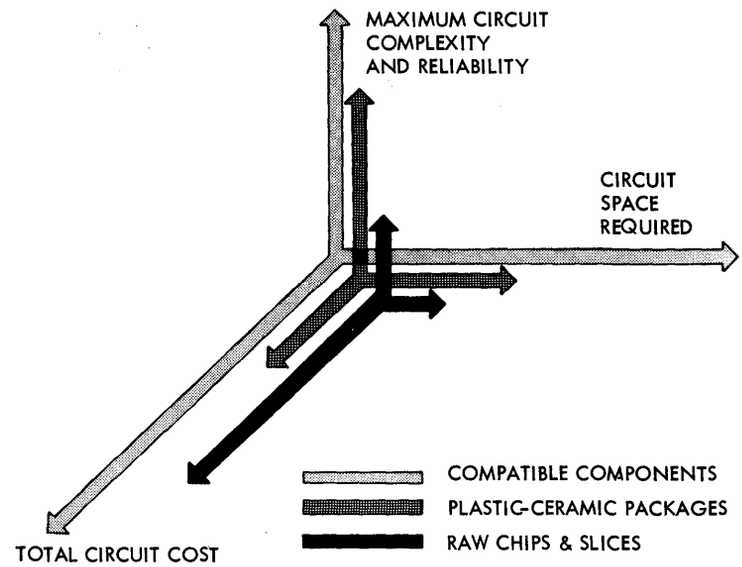
INTERFACE COMPONENTS



Texas Instruments line of *Interface Components* has been designed to meet the broad range of requirements for military, space, industrial, and consumer applications.

Interface Components are available in a variety of microminiature packages described on the following pages. These packages include the *Compatible Components: TO-50, Thin-Pac,* and *Flat-Pack;* and the plastic-ceramic packages: *Chip-Pak, Pellet-Pak,* and *Flip-Channel-Pak;* the components are also available as raw chips and slices.

More than 5000 different silicon small-signal planar device types can be fabricated into these standard packages. Selection of the package configuration can be made by considering the requirements for reliability, size, assembly in hybrid circuits, and cost.

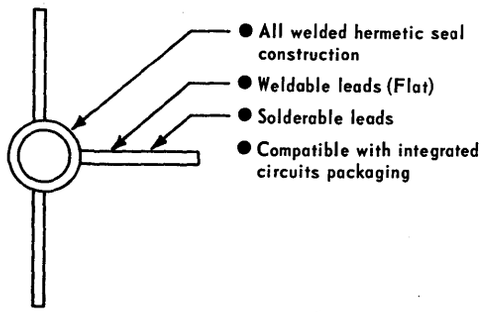


INTERFACE COMPONENT PACKAGE COMPARISON

WHAT ARE *COMPATIBLE COMPONENTS?*

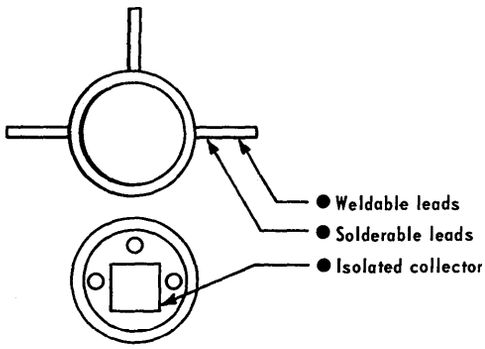
Discrete components which are electrically and mechanically compatible with integrated circuits. TI *Compatible Components* are used to perform functions supplementary to integrated circuits. At the same time, they can be handled, tested, and assembled with the same or essentially similar techniques and tools used for integrated circuits.

In addition, because of the form factors which are required to make components compatible with integrated circuits, most are also adaptable to circuit approaches requiring microminiature discrete components such as thin-film circuits.



TO-50

The **TO-50** hermetically sealed transistor package, introduced by Texas Instruments as the *μmesa** transistor package, is 0.210 inch in diameter and 0.050 inch thick.
*Trademark of Texas Instruments



THIN-PAC

The **THIN-PAC** power transistor package was developed by Texas Instruments to meet the power requirements of miniature circuits. It offers 40 watts dissipation at 100 degrees C case temperature in a package only 0.680 inch in diameter by 0.170 inch thick.

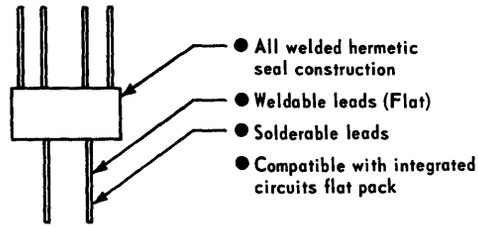
STANDARD *COMPATIBLE COMPONENT* DEVICE TYPES

There are now more than two dozen EIA registered small-signal *Compatible Components* available from TI, plus many custom devices. Two types of compatible power transistors and a large number of diode types in miniature packages are also available.

NEAREST STANDARD*	DESCRIPTION	COMPATIBLE COMPONENT		
2N929/2N2639	NPN Diff. Amp 10% Match	2N3046	*Flat Pack*	Dual
2N929/2N2640	NPN Diff. Amp 20% Match	2N3047	*Flat Pack*	Dual
2N929/2N2641	NPN Unmatched	2N3048	*Flat Pack*	Dual
2N930/2N2642	NPN Diff. Amp. 10% Match	2N3043	*Flat Pack*	Dual
2N930/2N2643	NPN Diff. Amp 20% Match	2N3044	*Flat Pack*	Dual
2N930/2N2644	NPN Unmatched	2N3045	*Flat Pack*	Dual
2N2412/2N2805	PNP Diff. Amp 10% Match	2N3049	*Flat Pack*	Dual
2N2412/2N2806	PNP Diff. Amp 20% Match	2N3050	*Flat Pack*	Dual
2N2412/2N2807	PNP Unmatched	2N3051	*Flat Pack*	Dual
2N914	NPN Driver	2N3052	*Flat Pack*	Dual
2N2497 FET	P-Channel FET Diff. Amp 5% Match	2N3333	*Flat Pack*	Dual
2N2497 FET	P-Channel FET Dual Unmatched	2N3336	*Flat Pack*	Dual
2N2222/2N2907	Complementary Pair	2N3838	*Flat Pack*	Dual
2N706A	NPN Switch	2N849	*TO-50*	
2N753	NPN Switch	2N850	*TO-50*	
2N743	NPN Switch	2N851	*TO-50*	
2N744	NPN Switch	2N852	*TO-50*	

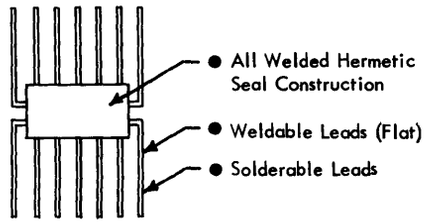
NEAREST STANDARD*	DESCRIPTION	COMPATIBLE COMPONENT	
2N929	NPN High-Gain Amp	2N2387	*TO-50*
2N930	NPN High-Gain Amp	2N2388	*TO-50*
2N696	NPN General Purpose	2N2395	*TO-50*
2N697	NPN General Purpose	2N2396	*TO-50*
2N1613	NPN General Purpose	2N2389	*TO-50*
2N1711	NPN General Purpose	2N2390	*TO-50*
2N2243	NPN General Purpose	2N3037	*TO-50*
2N1890	NPN General Purpose	2N3038	*TO-50*
2N1131	PNP General Purpose	2N2393	*TO-50*
2N1132	PNP General Purpose	2N2394	*TO-50*
2N2904	PNP General Purpose	2N3040	*TO-50*
New Product	NPN 10-Amp Power Switch (60 v)	2N3551	*Thin-Pac*
New Product	NPN 10-Amp Power Switch (80 v)	2N3553	*Thin-Pac*

*Single or dual where applicable



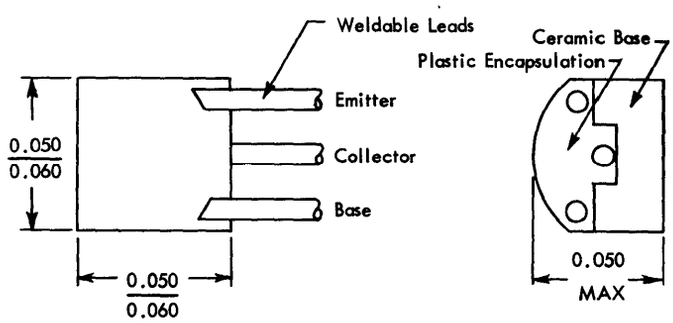
FLAT PACK

The dual SCN hermetically sealed **FLAT PACK** offers component miniaturization with no compromise in electrical or mechanical characteristics. The package measures 0.250 by 0.150 by 0.050 inch.



CUSTOM FLAT PACK

CUSTOM FLAT PACK configurations are also available for *Compatible Components*. Custom devices may be supplied in the 6-, 10-, or 14-lead hermetically sealed package. Four discrete planar transistors can be supplied in one **FLAT PACK** with all leads isolated. Five to six transistors in one package are possible with certain interconnections. Custom configurations are the same size as the dual SCN **FLAT PACK.**



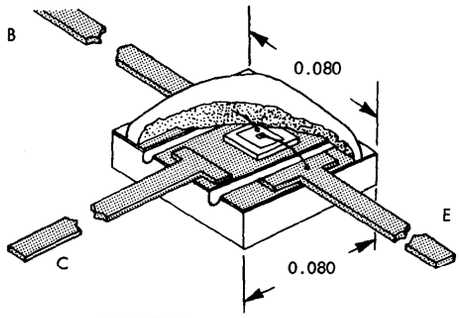
CHIP-PAC

The **CHIP-PAC** is the ultimate in discrete transistor miniaturization. Transistor chips are alloyed to a metalized ceramic base and are plastic encapsulated. The package provides a relatively high degree of environmental protection. The gold-plated leads are weldable and solderable. Standard **CHIP-PAC** devices include:

Nearest Standard	Description	CHIP-PAC
2N929	NPN Diff. Amp.	TIS22
2N930	NPN Diff. Amp.	TIS23
2N2484	NPN Diff. Amp.	TIS24

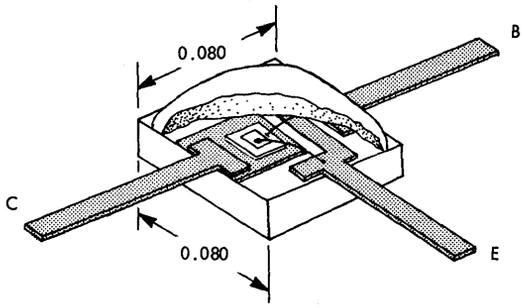
HOW RELIABLE ARE *COMPATIBLE COMPONENTS?*

More than five thousand TI *Compatible Components* have been subjected to high-level step-stress tests as a part of the extensive quality and reliability testing requirements of the Component Quality Assurance Program (CQAP) for the Minuteman II Program. The program has as its goal component use-condition failure rates in the order of ten-thousandths of a percent (.000X%) per thousand hours. The program is keyed to constant product improvement, using destructive testing techniques to determine potential failure mechanisms. At TI this means that the active chips themselves, as well as the package in which the chips are contained, are undergoing constant process improvement. Tests results are analyzed, and even subtle and very obscure failure mechanisms are isolated and attacked systematically through the process improvement feedback loop. Extensive reliability data is available. Contact your TI Field Sales Engineer.



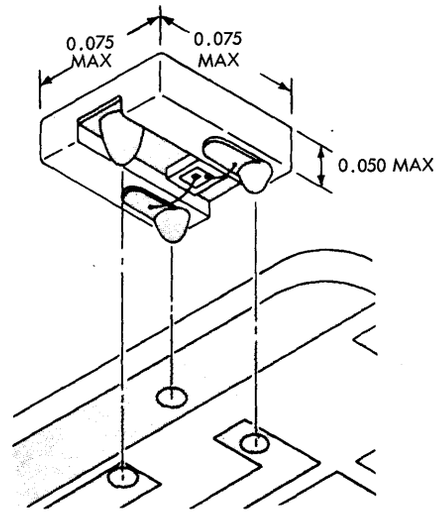
PELLET-PAK

PELLET-PAK devices are low-cost fully tested microminiature packages available with both solderable and weldable leads designed for automated assembly. They feature a plastic sealed ceramic header and low thermal resistance. High-frequency models with low lead inductance are also available. Their environmental capabilities match those of canned transistors.



HIGH-FREQUENCY PELLET-PAK

The **FLIP-CHANNEL-PAK** is specially designed for leadless automated thermal or ultrasonic bonding to film substrates. It retains all other features of the **PELLET-PAK** configuration.



FLIP-CHANNEL-PAK

RAW CHIPS AND SLICES

Silicon transistors in raw chip and slice form have the lowest initial cost and smallest possible size. Although relatively sophisticated bonding and alloying technologies are required, substantial savings may be achieved in non-critical operations. Texas Instruments can supply any device from its broad line of silicon planar transistors in either chip or slice form.

WHERE ARE *INTERFACE COMPONENTS* USED?

In any application requiring a high-quality miniature semiconductor. Here are some applications where TI *Interface Components* are being used today:

• Digital and analog interface circuits, for integrated circuits • Driver circuits • Sense amplifiers • Thin-film circuits • Critical differential amplifiers • High-impedance amplifiers • Special analog circuits • D-c amplifiers • Diode matrixes • Complementary (NPN/PNP) circuits • Power switching to 5 amps

Functionally, the devices fall into the following categories:

• Differential amplifiers (dual elements), NPN and PNP • Low-level, low-noise amplifiers (dual elements), NPN and PNP • Low-level switching (dual elements), NPN and PNP • Dual drivers, NPN • High-current driver and power switches, NPN • Drivers (single), NPN and PNP • High-speed switches (single) NPN • Multiple diodes in most common configurations